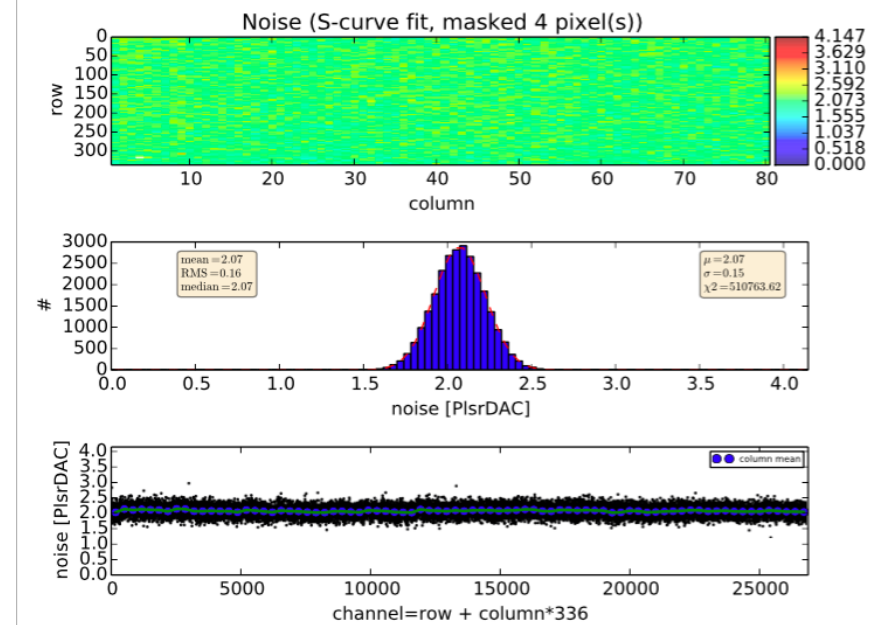
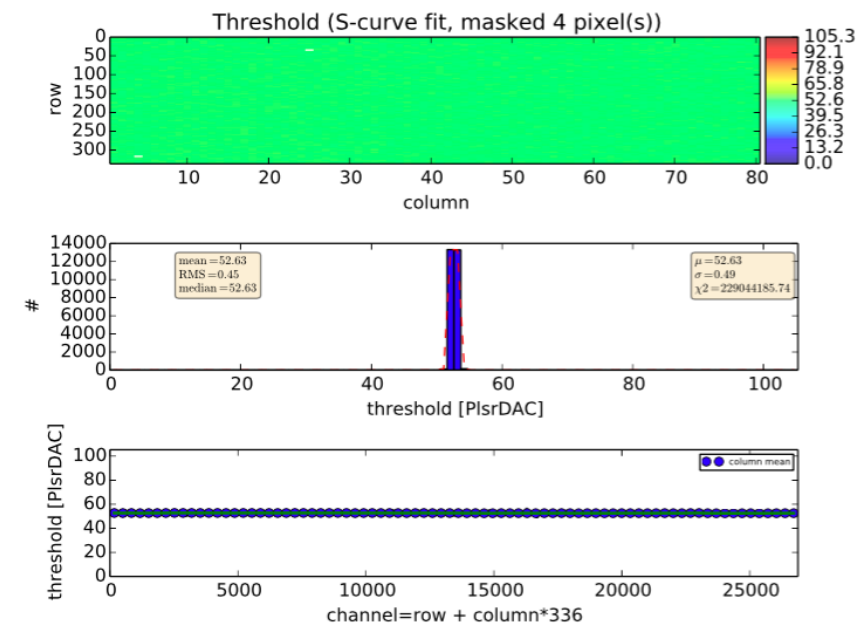
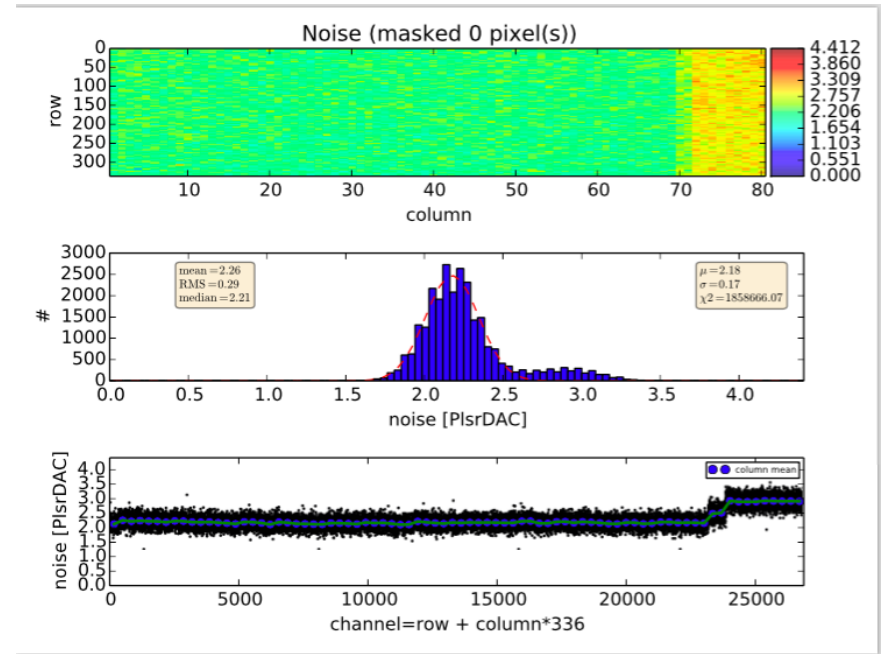
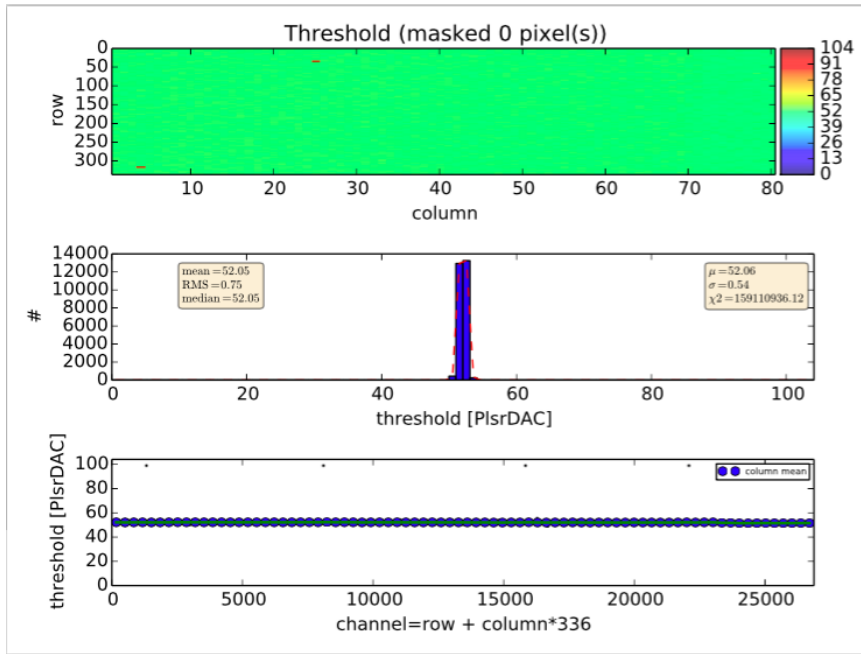


# Chip Scan and Board Quality Test Results

ILSOO SEONG

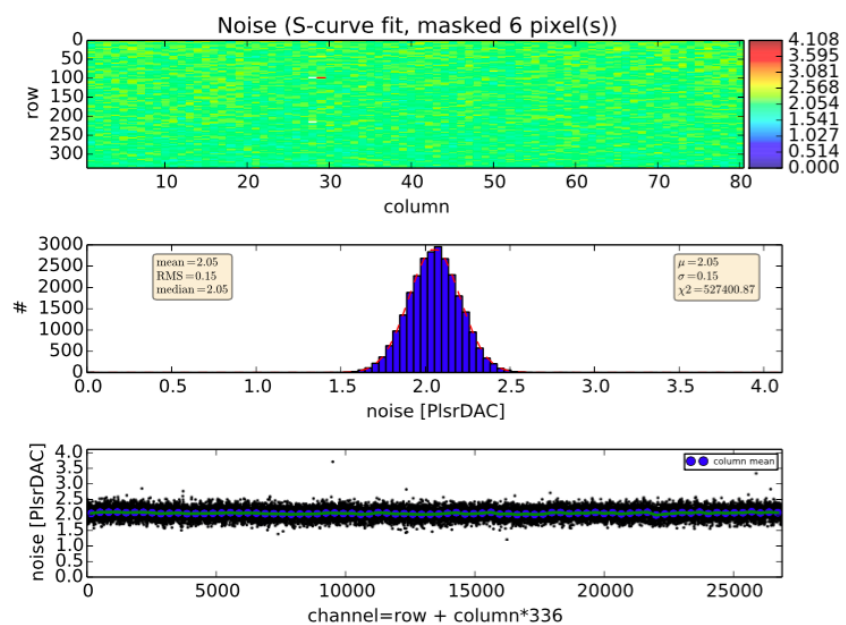
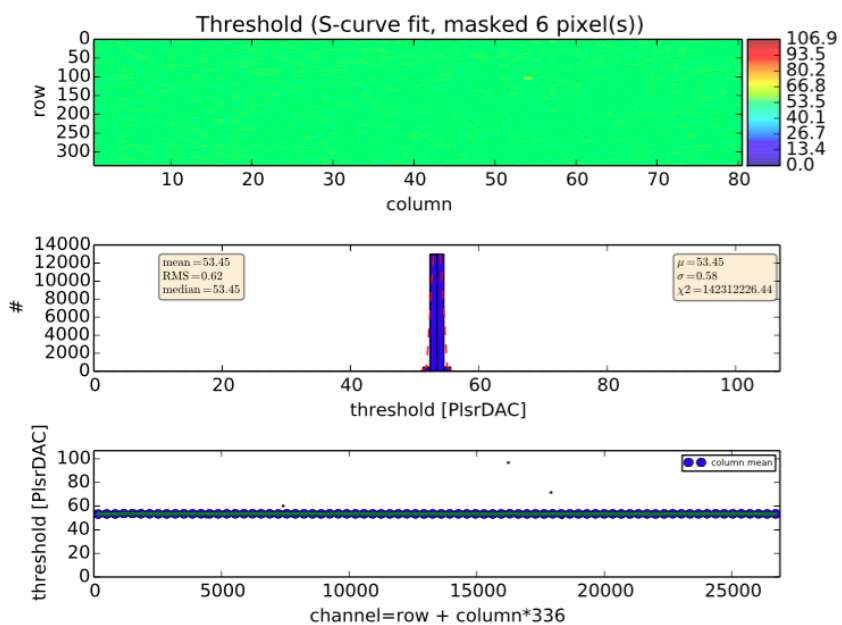
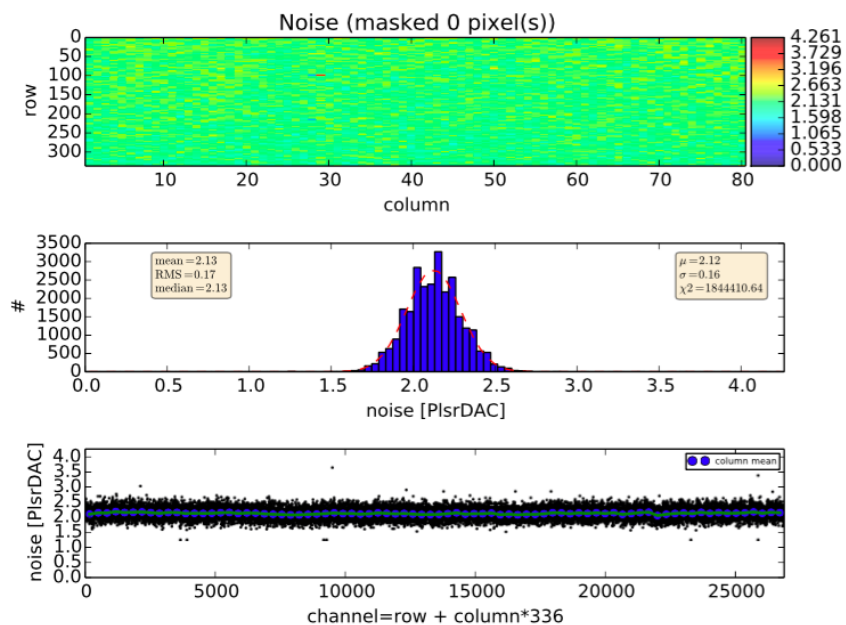
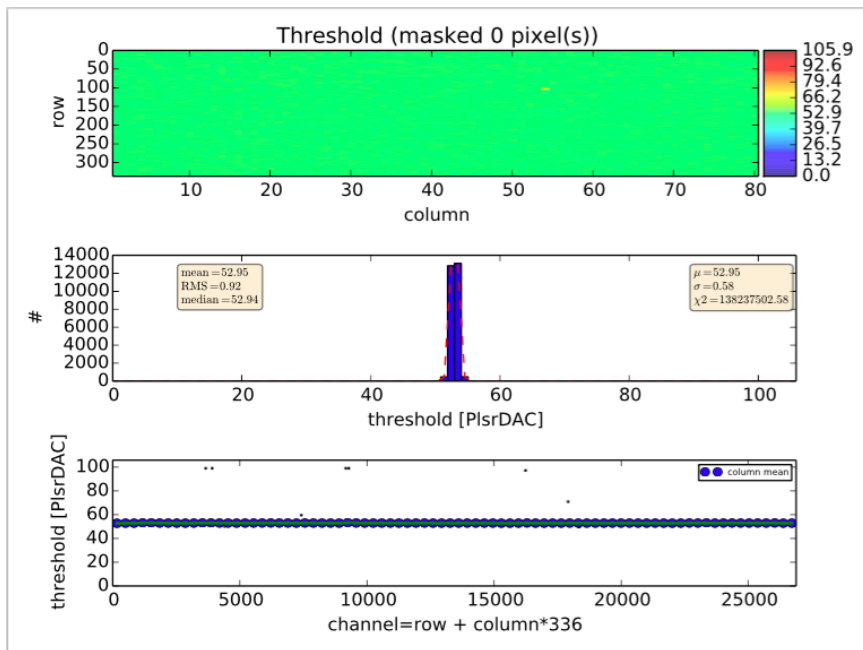
May 13, 2015

# Board #1 (Target Threshold = 52 = $\sim 3000$ e, 2.0 plsrDAC = $\sim 114$ e)



# Board #2 (Target Threshold = 52 = ~3000 e, 2.0 plsrDAC = ~114 e)

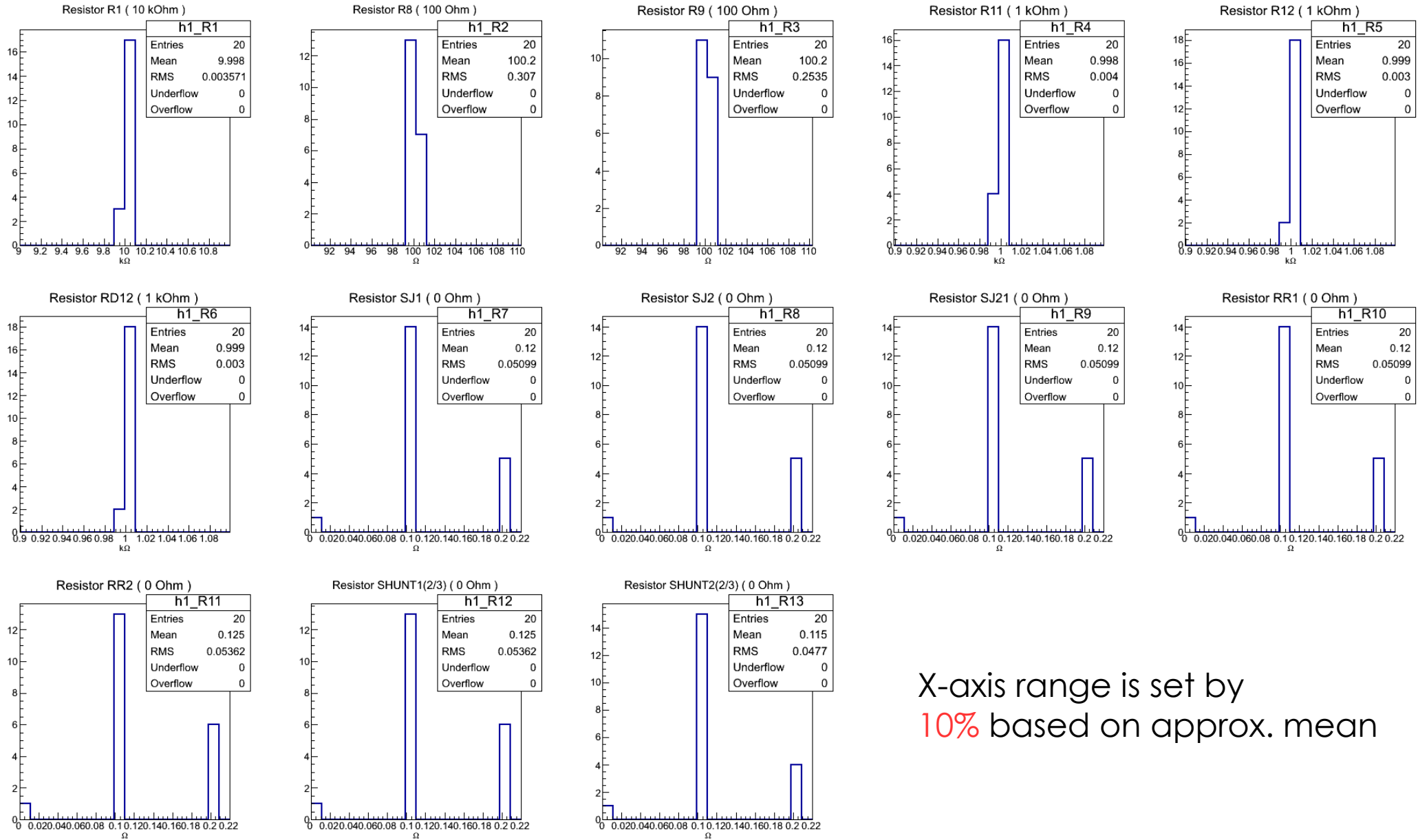
Found tiny hair(?) on the chip: I didn't remove it



## Summary of Testing Quality for Board

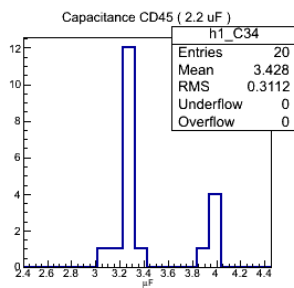
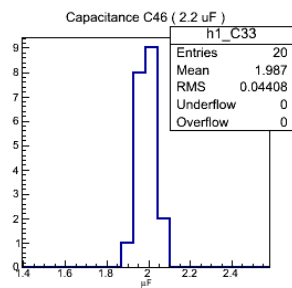
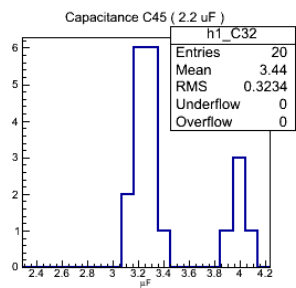
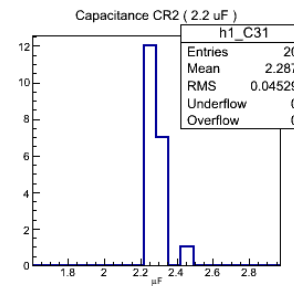
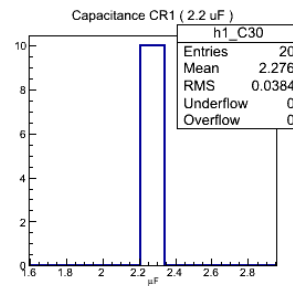
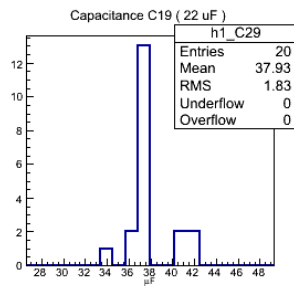
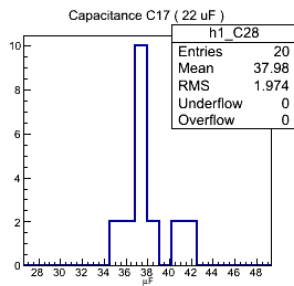
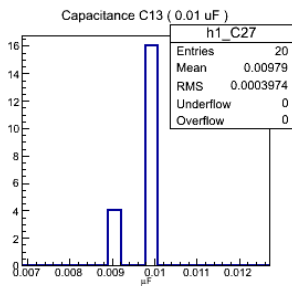
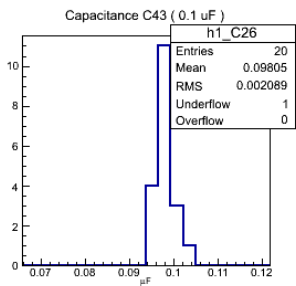
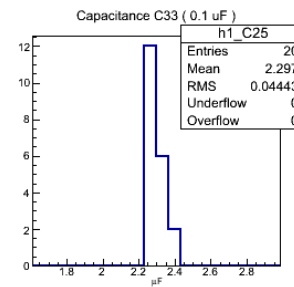
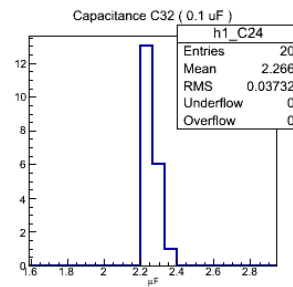
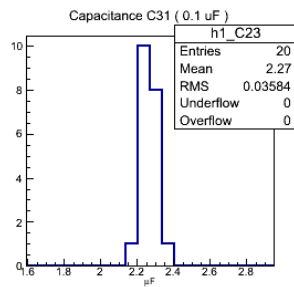
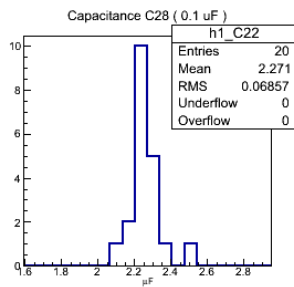
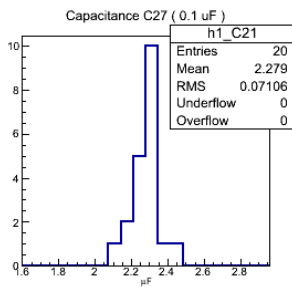
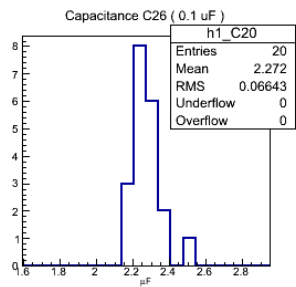
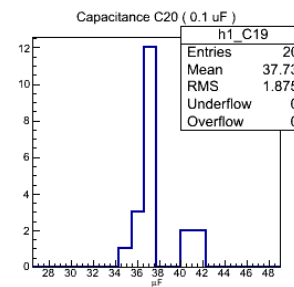
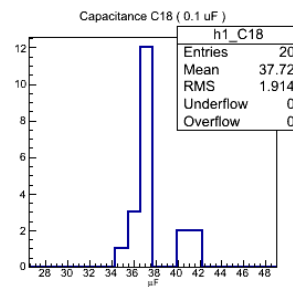
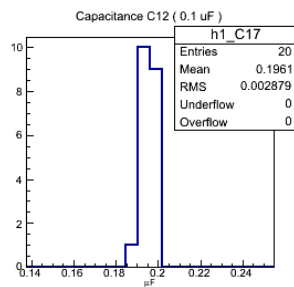
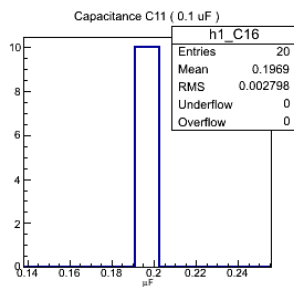
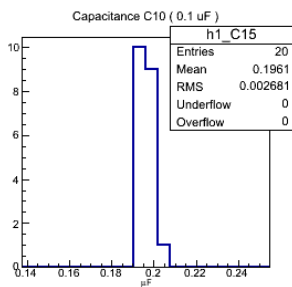
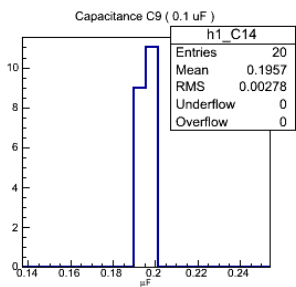
- Most them are very clean. I saw a stain(?) on the two boards only.
- No missing Components except first one I reported before.
- Resistor values are all within 10% of actual component's value.
- Capacitor values are very sensitive depending on how I measure  
Most of them (except 5 boards) within 10% from mean of measured value.  
The multimeter which I used before is broken(?) for capacitor measurement
  - I used different multimeter and different probe
  - It caused offset(?).

# Measured Distribution of Resistors



X-axis range is set by  
**10%** based on approx. mean

# Measured Distribution of Capacitors



X-axis range is set by  
**30%** based on approx. mean

## Next Plan

- Support Plates of the chip are already ready.
- Send all board to Maurice.
  - Question is do we also ask installation of wire-bond bridge?

## Testing Chip Process

- Need to Tune each chip.
- Process: Tune → Digital Scan → Threshold Scan
  - Q: Anything Else? e.g. TOT Calibration?
- Tune and threshold scan takes around 20~30 minutes per chip:
  - Do we need to use clean-room?