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RFpix1 Feasibility Study

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Introduction

- RFpix1 will be used in future upgrade of Bell
- It will be positioned very closed to the beam line
- It will calculate the position of event
  - By receiving the TEM waves formed due to redistribution of charges between the layers of conductor and dielectric that will travel (going in both direction from the event) in transmission lines placed on a dielectric substrate
- ILC vertex detector and future use as XFEL detector

Requirements

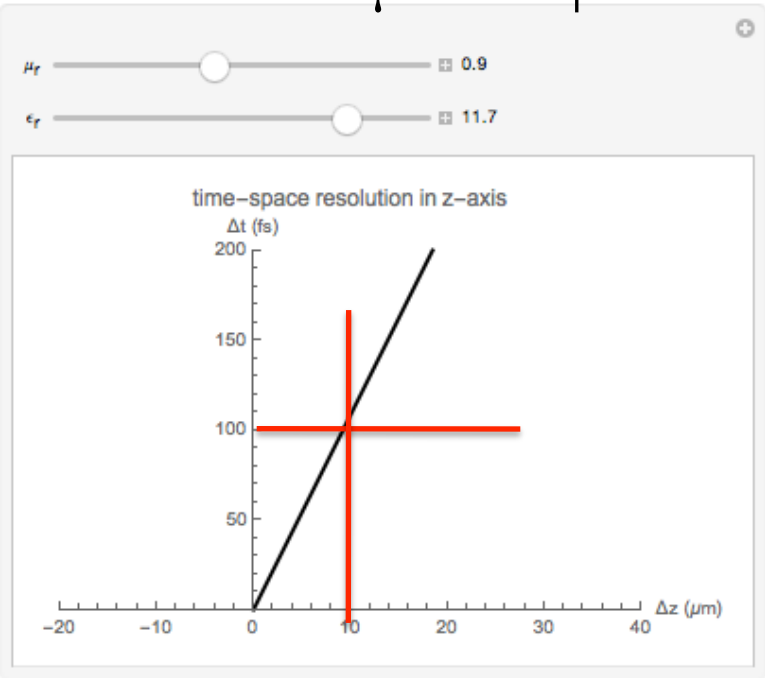
-Sampling at high sampling rate and high bandwidth

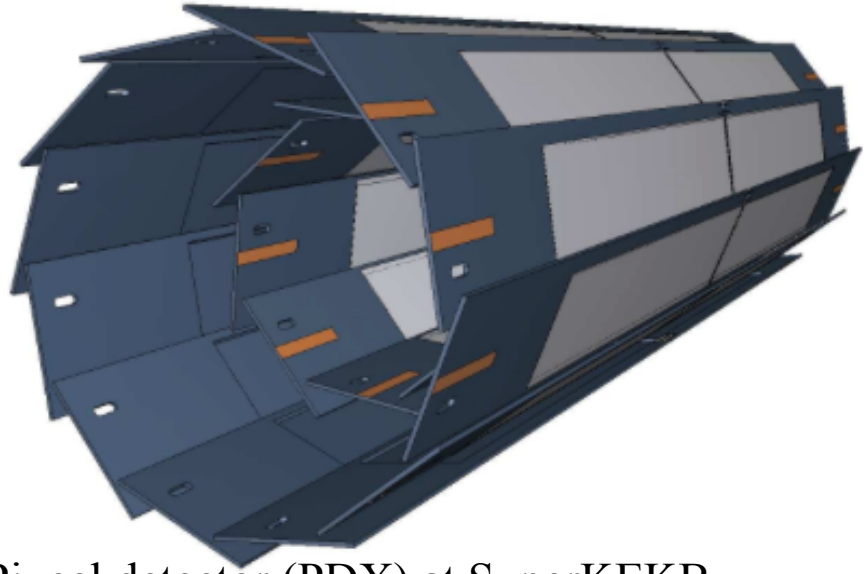
-Resolve small distances

Current Goals: Spatial resolution of 10μm in z and 20μm in rφ

In Silicon 10μm in z corresponds to timing resolution of about 100fs

20μm in rφ will depend on the Signal to Noise Ratio

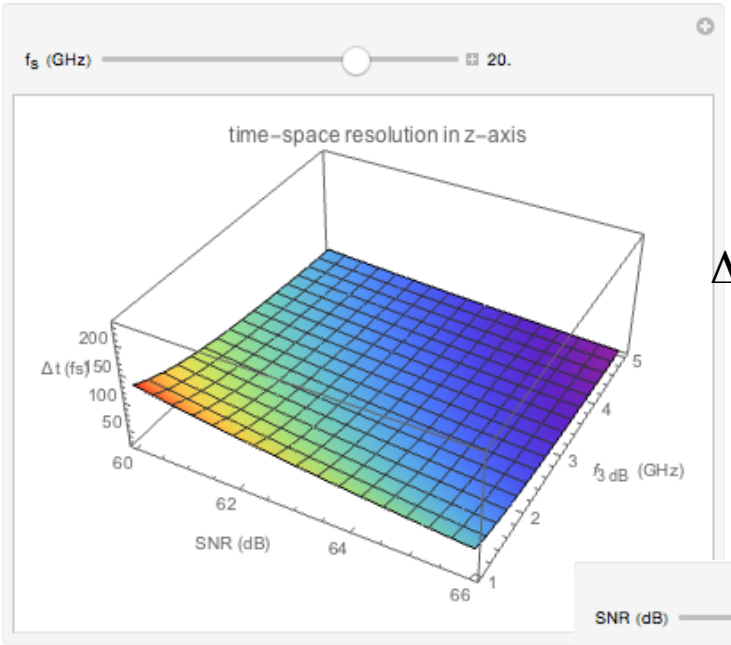




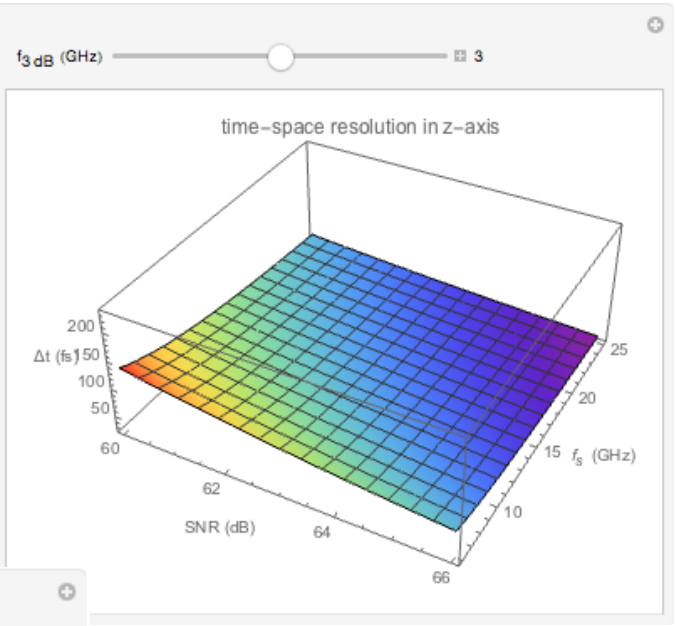
Pixcel detector (PDX) at SuperKEKB

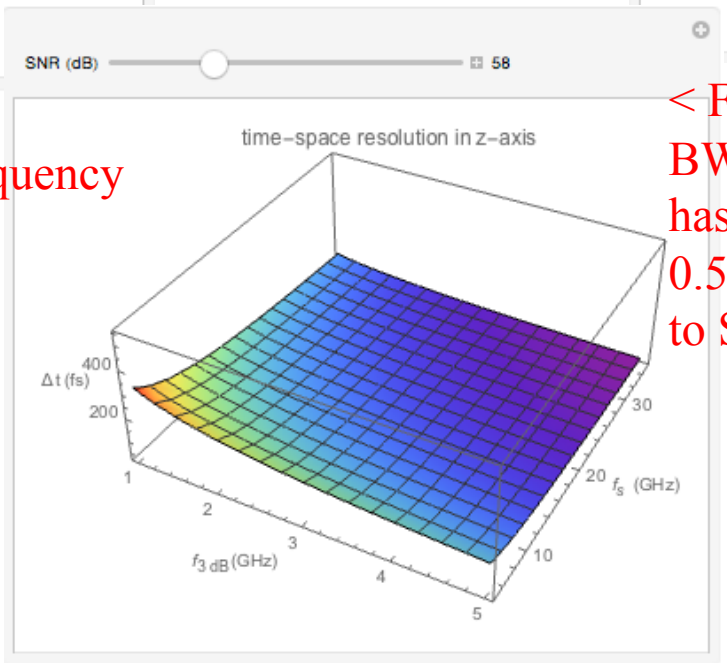
Image from http://arxiv.org/ftp/arxiv/papers/1011/1011.0352.pdf

Plots of parameter sweep for time resolution in z



$$\Delta t = \frac{\Delta U}{U}\frac{1}{\sqrt{0.34 * BW * f_s}}$$





^ Need to hold sampling frequency at least at 20 GHz so we can have timing resolution in 100fs range

< For the above sampling freq and BW integrated noise amplitude has to be in the range or less than 0.5mV to 0.6mV corresponding to SNR~58dB (V_{pp}=1volts)

SNR~58dB corresponds to 9.4 bit for 20μm resolution in rφ (Ideal ADC)

Requirements (cont.)

Parameter	Minimum desired value
Sampling frequency (ASIC)	20 GHz
Bandwidth (Detector and ASIC)	3 GHz
Signal to Noise Ratio (Detector and ASIC)	58dB (V_{pp}=1 volts)
Velocity of Propagation (Transmission Line/ strip line)	0.35c
Number of Bit (ADC)	9 bit

Basic Structure

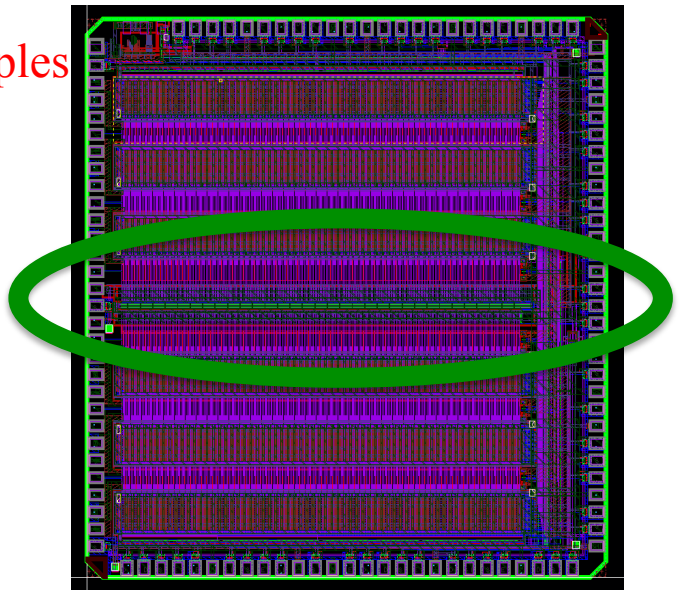
- Using a switched capacitor array (SCA) for track and hold
- Followed by a buffered storage capacitor array
- Using fast Wilkinson ADC clock for digitization

PSEC4: Analysis for Sampling Stage

Utilizing PSEC4's SCA for our analysis

-Adjustable Sampling rate between 4-15Gigasamples

-1.5 GHz bandwidth



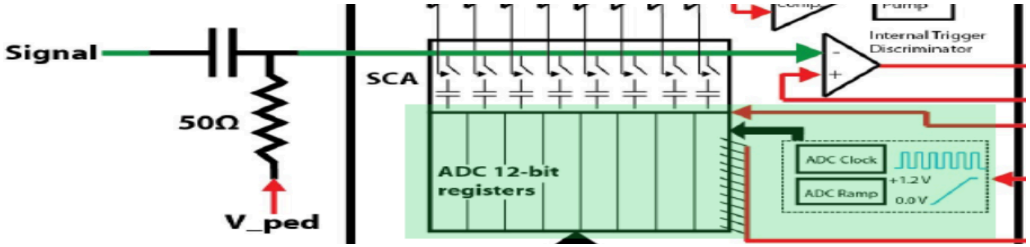
also

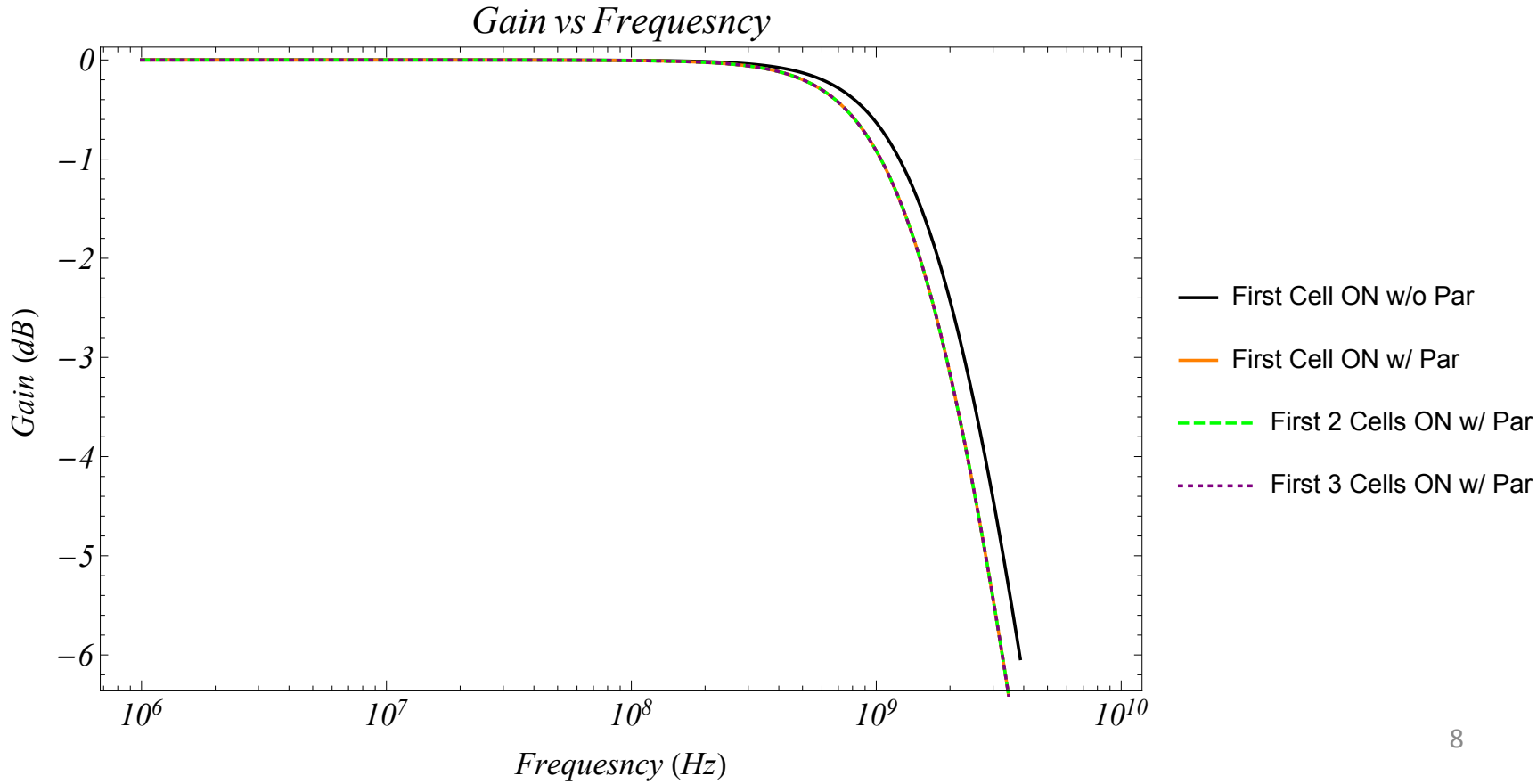
-0.13µm CMOS (IBM-8RF)

-10.5 bit DC dynamics

Equivalent Circuit

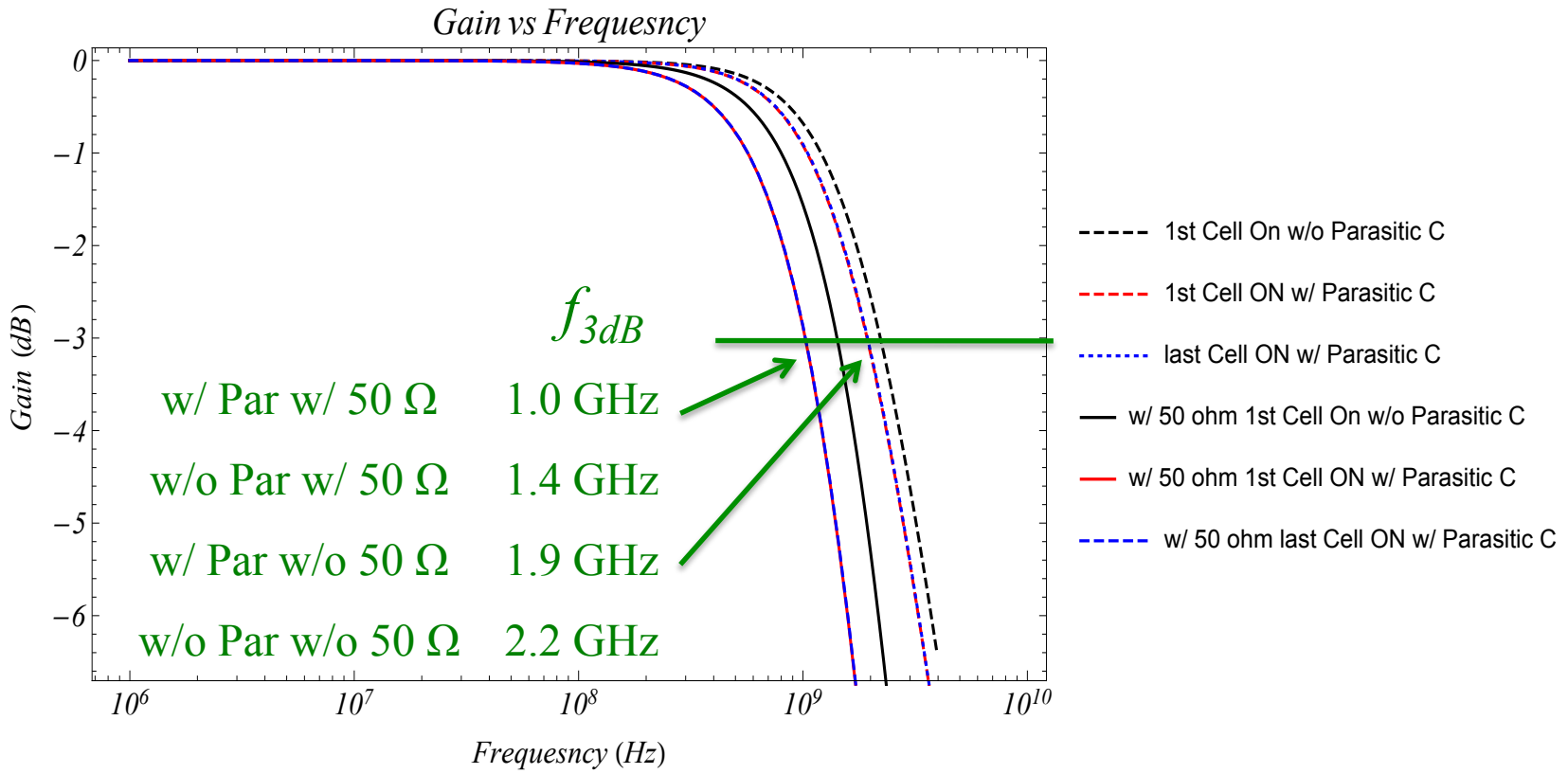
Multichannel sampling array





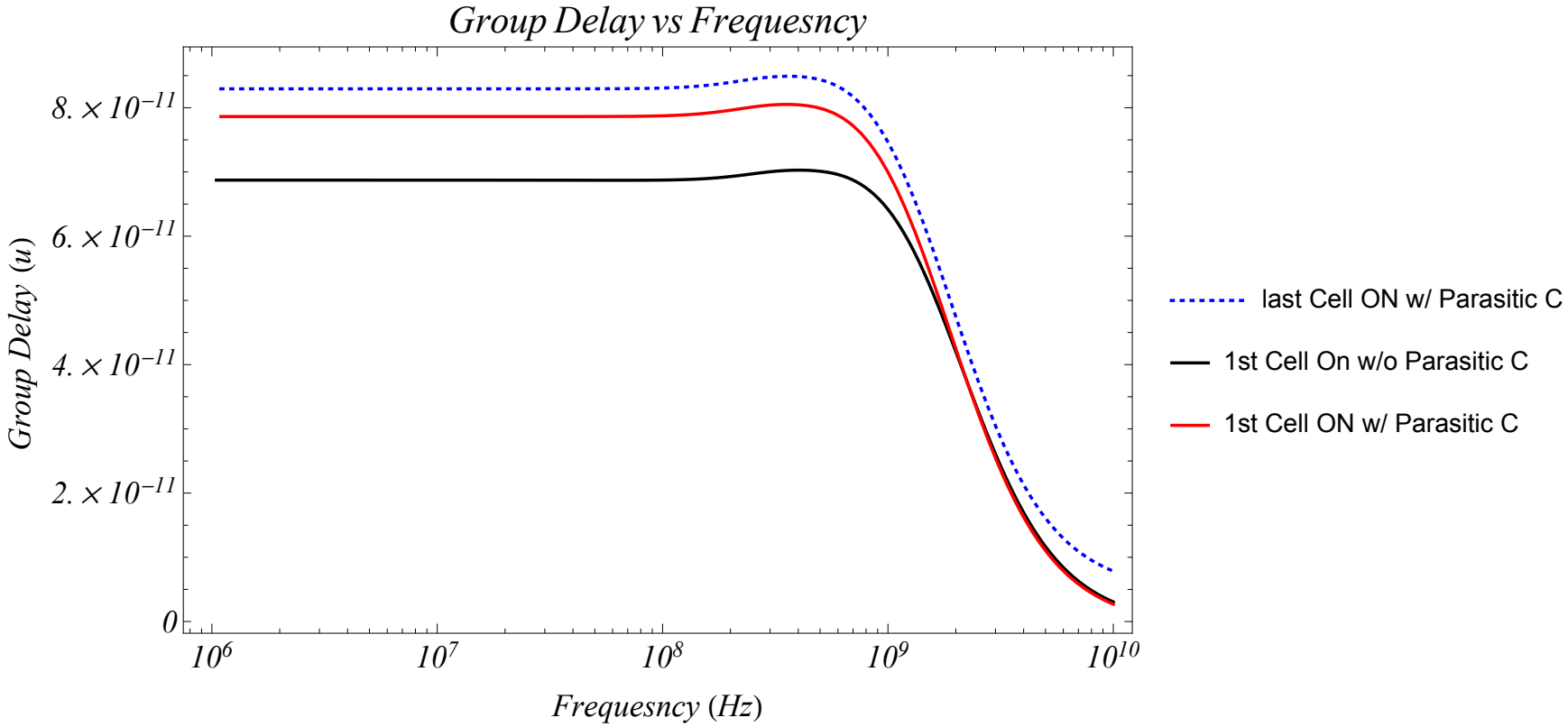
Simulation Results: Bandwidth for worst case operating bias point

Whether the 1st switch is on or the last, Gain is the same



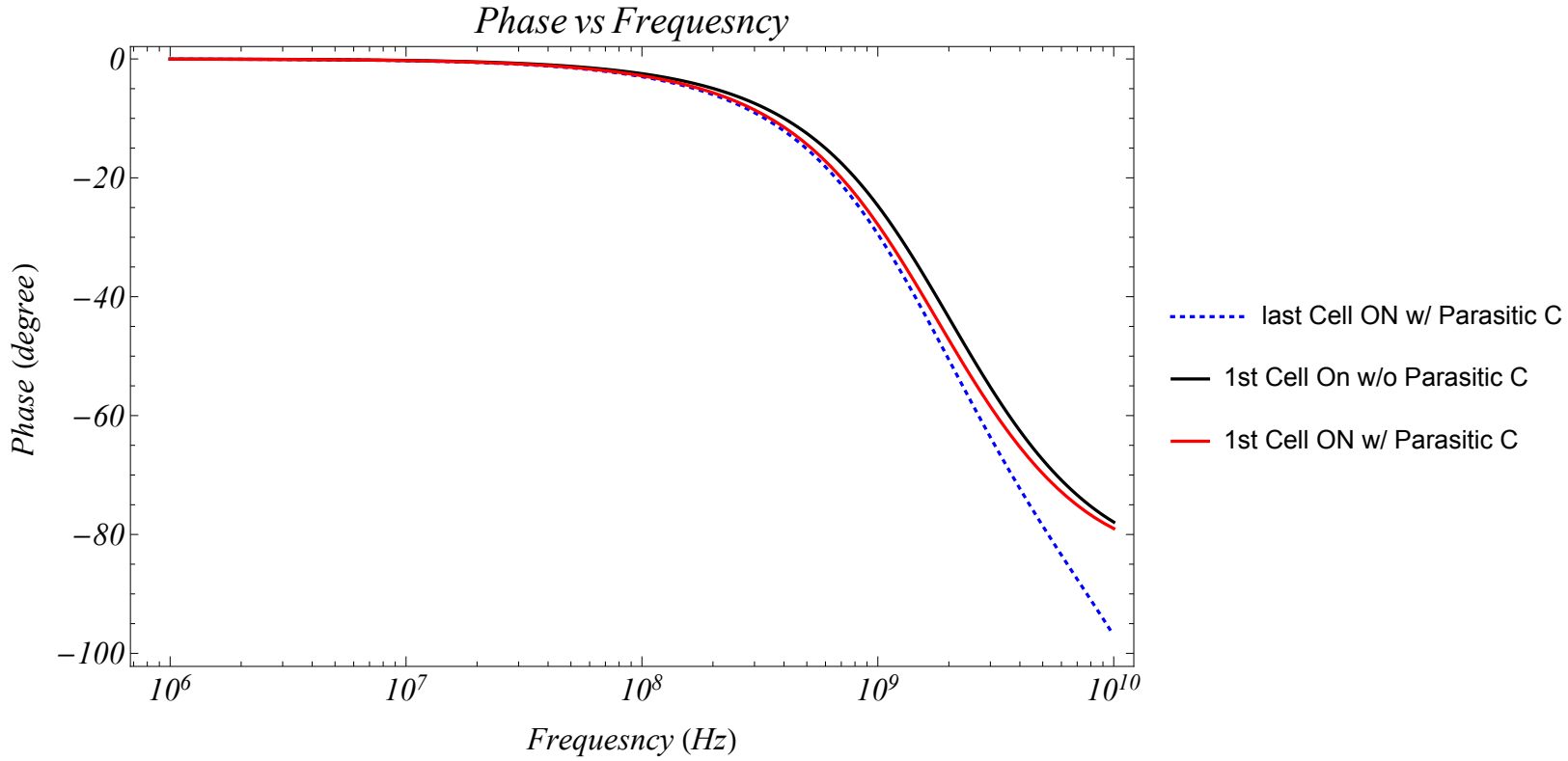
Simulation Results: Group Delay

Group Delay does vary depending which switch is on by ~25ps which puts a constraint on sampling time window



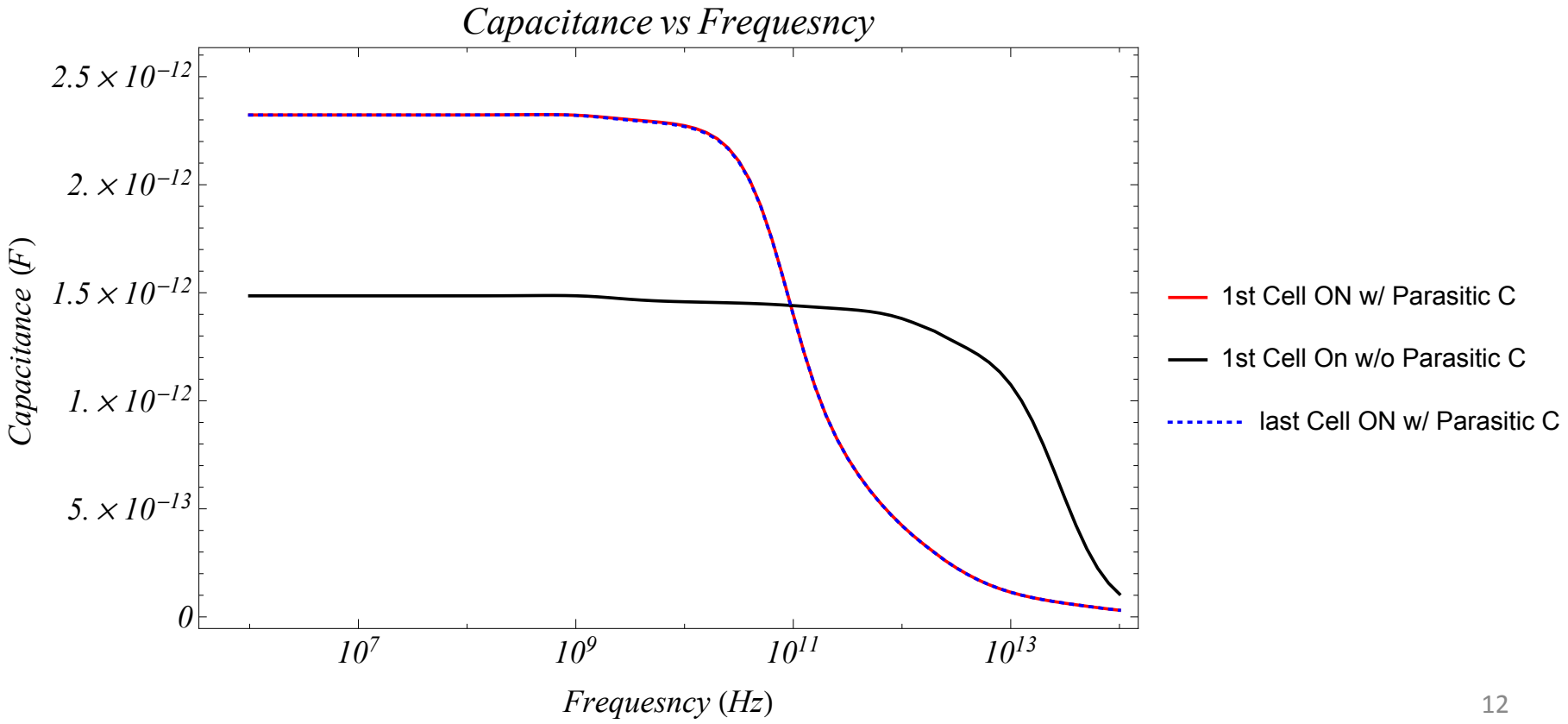
Simulation Results: Phase

- At higher frequencies Phase vs freq behavior is also different and depends on which switch is on



Simulation Results: Capacitance

Capacitance is at 2.2 pF and not dependent on witch switch is on



Future Plans

- Investigate Group Delay and Phase more
- Model and study Parasitic capacitance of the Transmission Line

Next

Study of single sampling cell (of PSEC4)
by Peter Orel

And summary comparison of measured parameters with requirements