PHYS476 Electronics for Physicist

RFpix1 Feasibility Study, part 2

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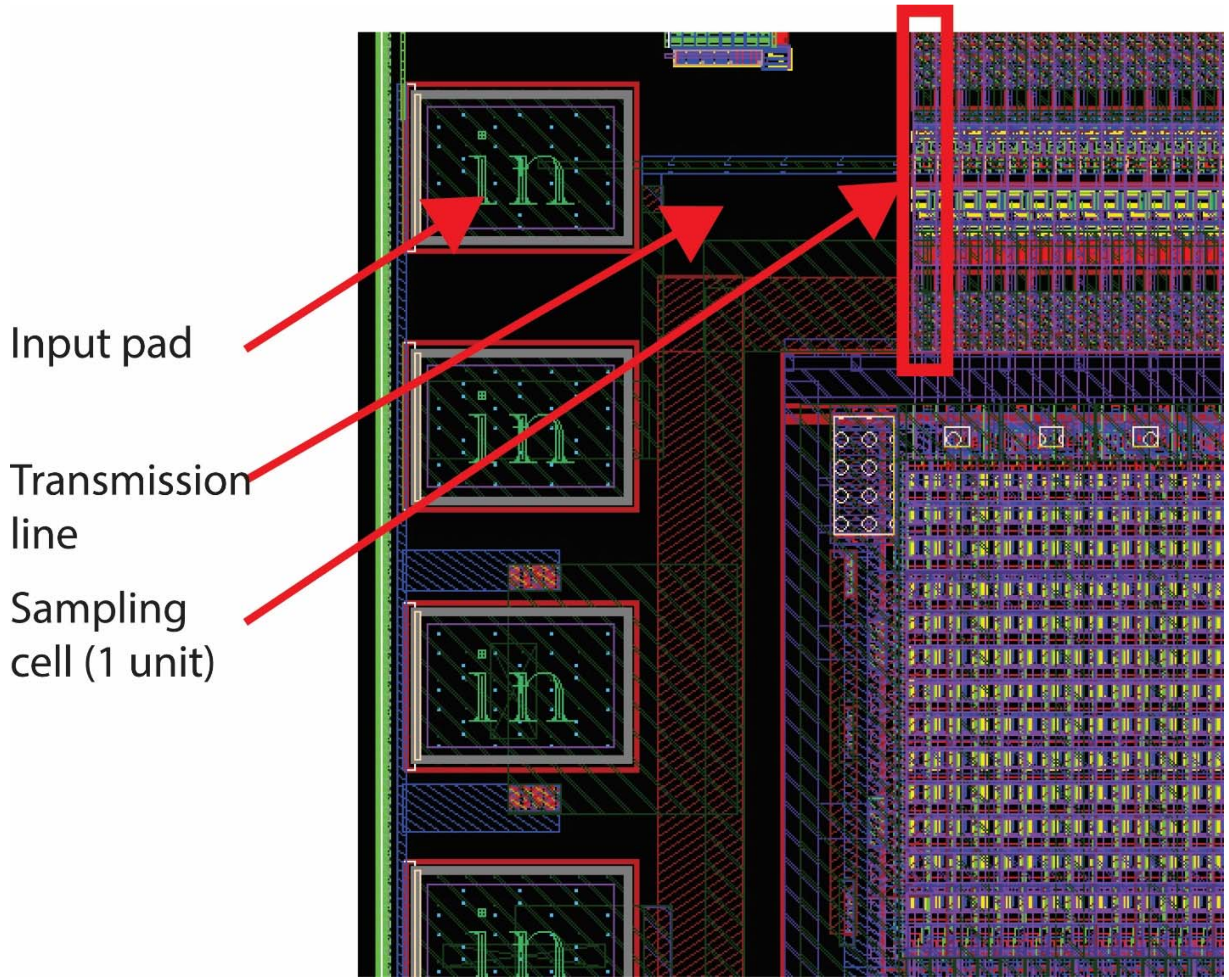
CONTENT:

- Performance evaluation of the PSEC4 single cell
- Summary of the results and comparison with the requirements

PSEC4 Analysis: Single Sampling Cell

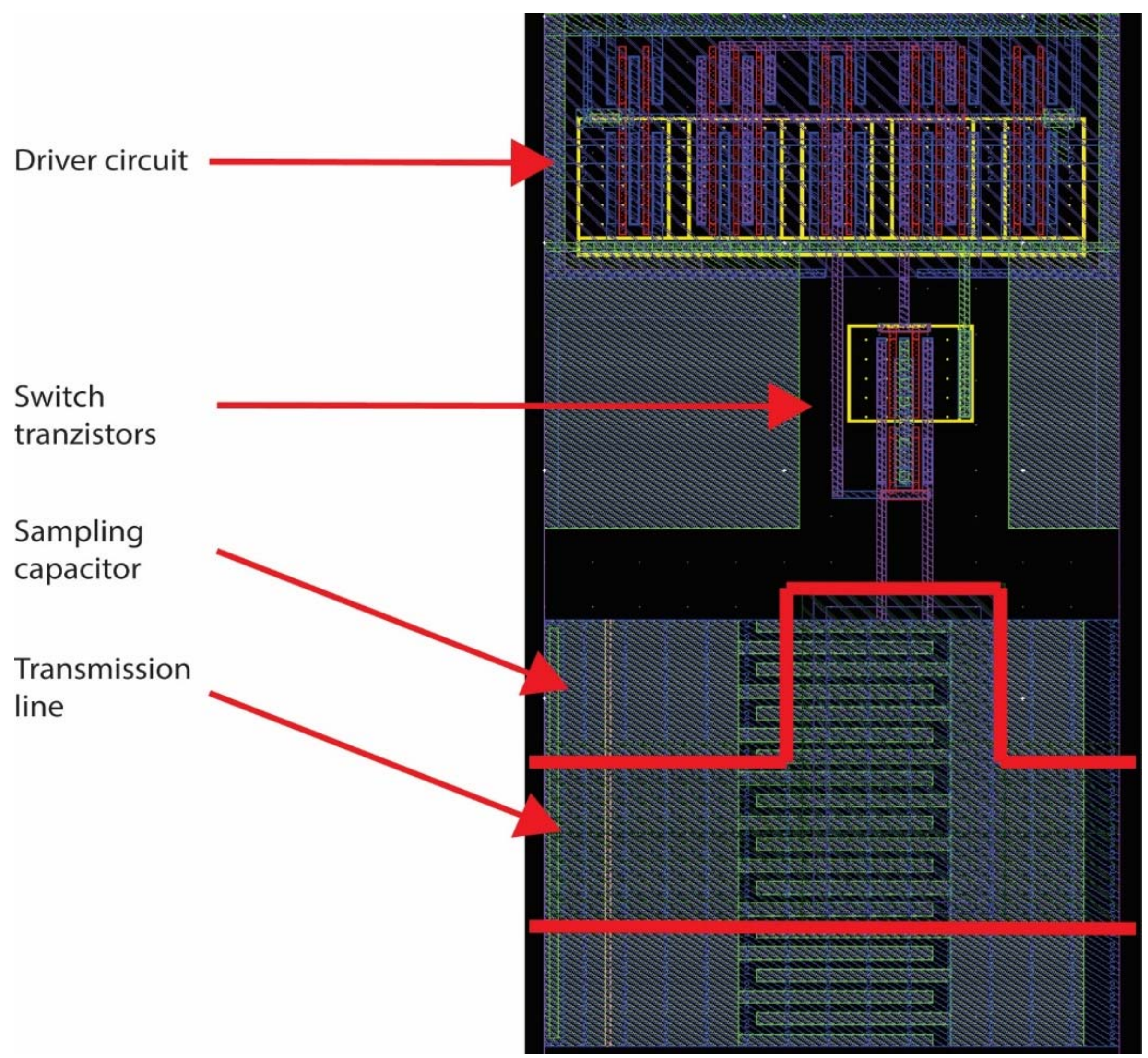
Structure & Layout, part 2



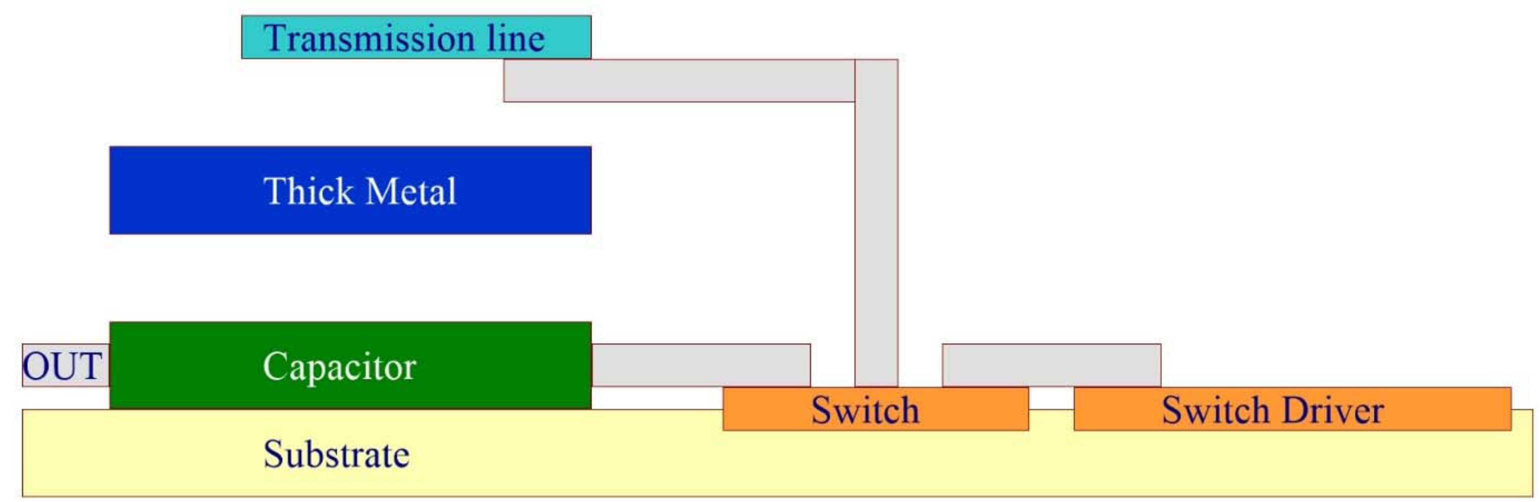
PSEC4 Analysis: Single Sampling Cell

Structure & Layout, part 2

Top view



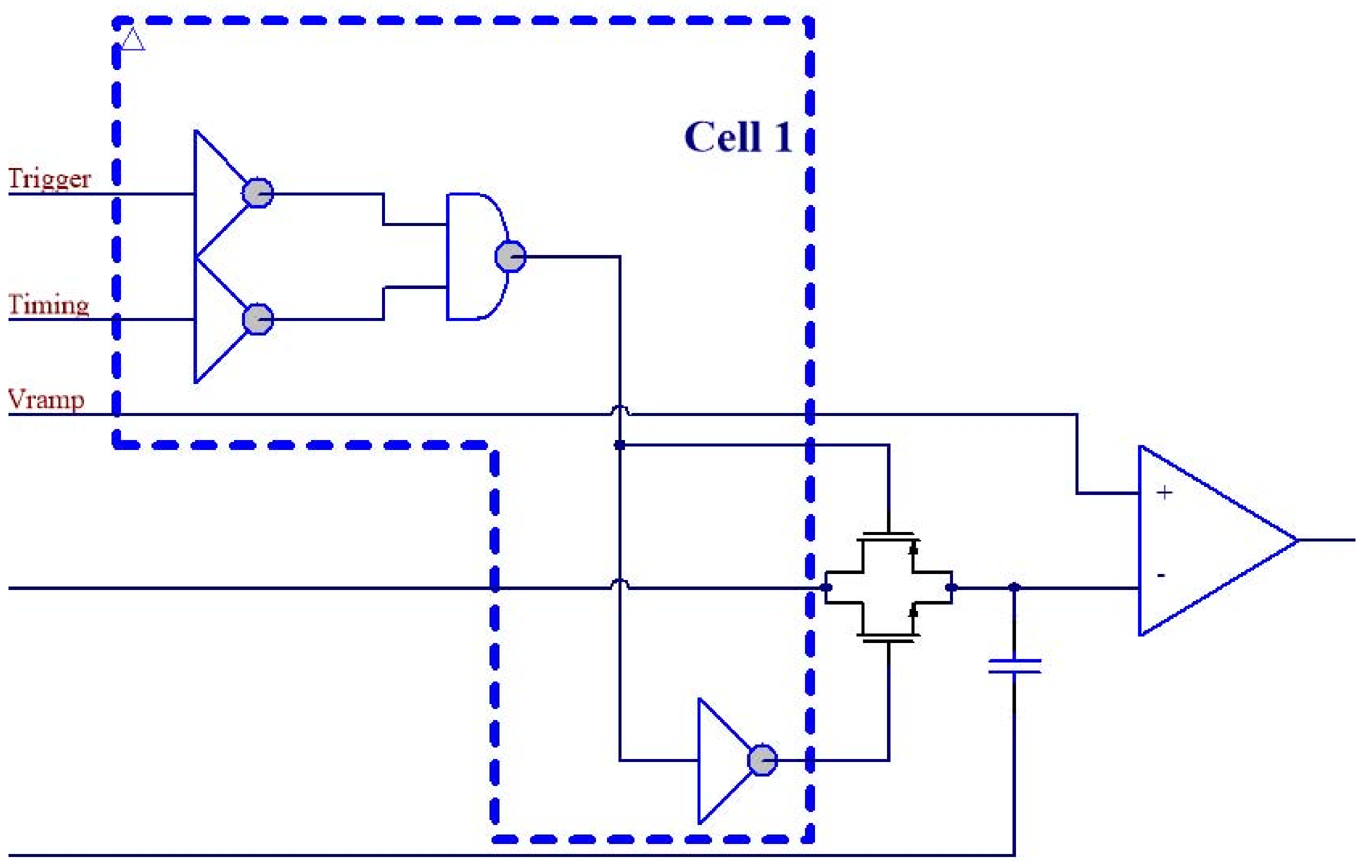
Side view



PSEC4 Analysis: Single Sampling Cell

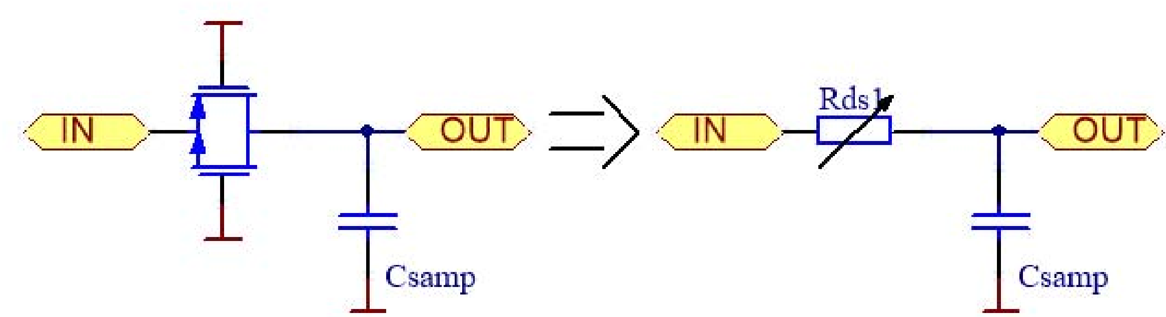
Structure & Layout, part 3

Simplified Schematic



- Driver circuit
- Switch with n-p FET pair
- Sampling capacitor
- Comparator as load

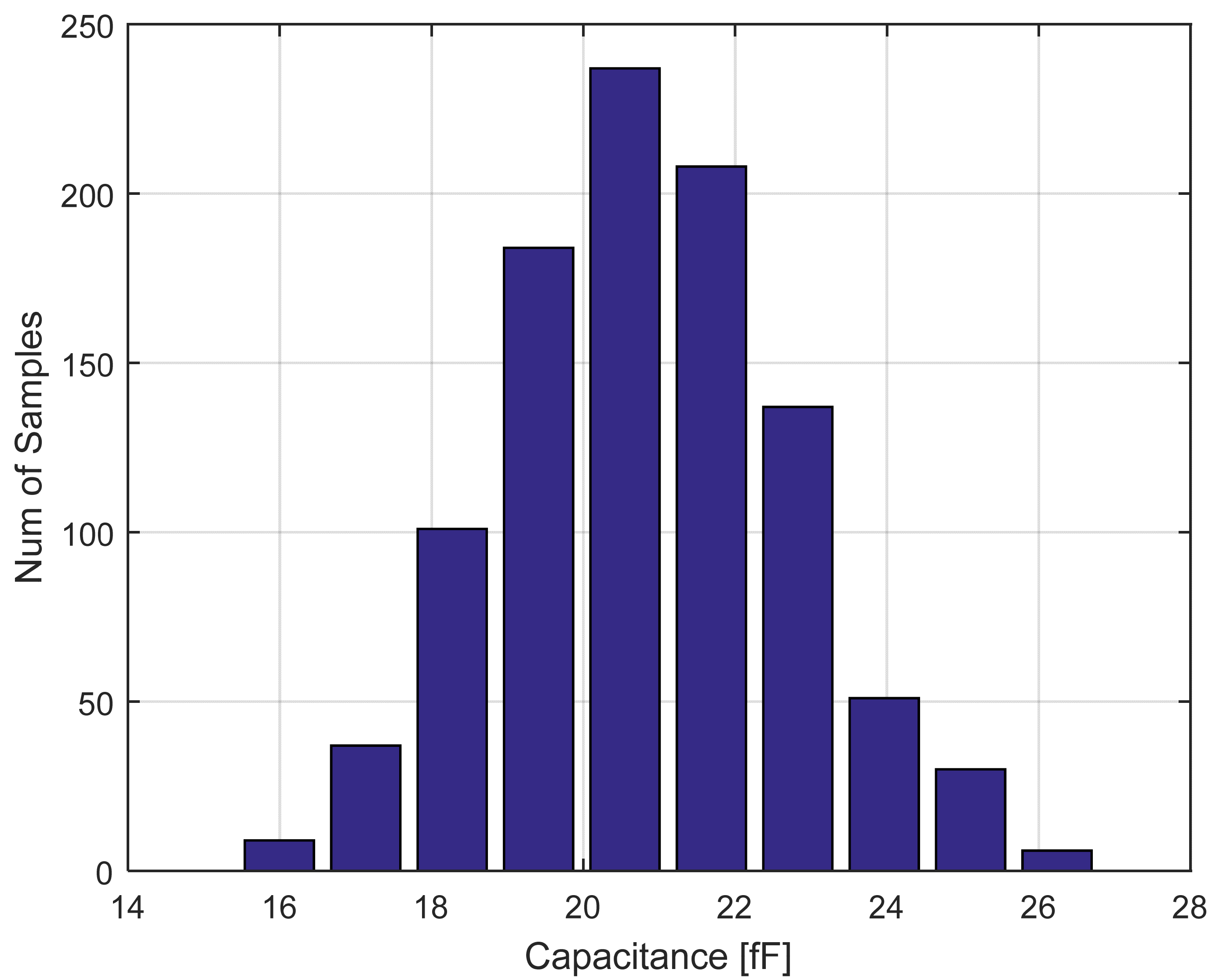
Switch & Sampling Capacitor Equivalent Circuit



- Check Csampling capacitance
- Identify Ron and Roff

PSEC4 Analysis: Single Sampling Cell

Sampling Capacitor



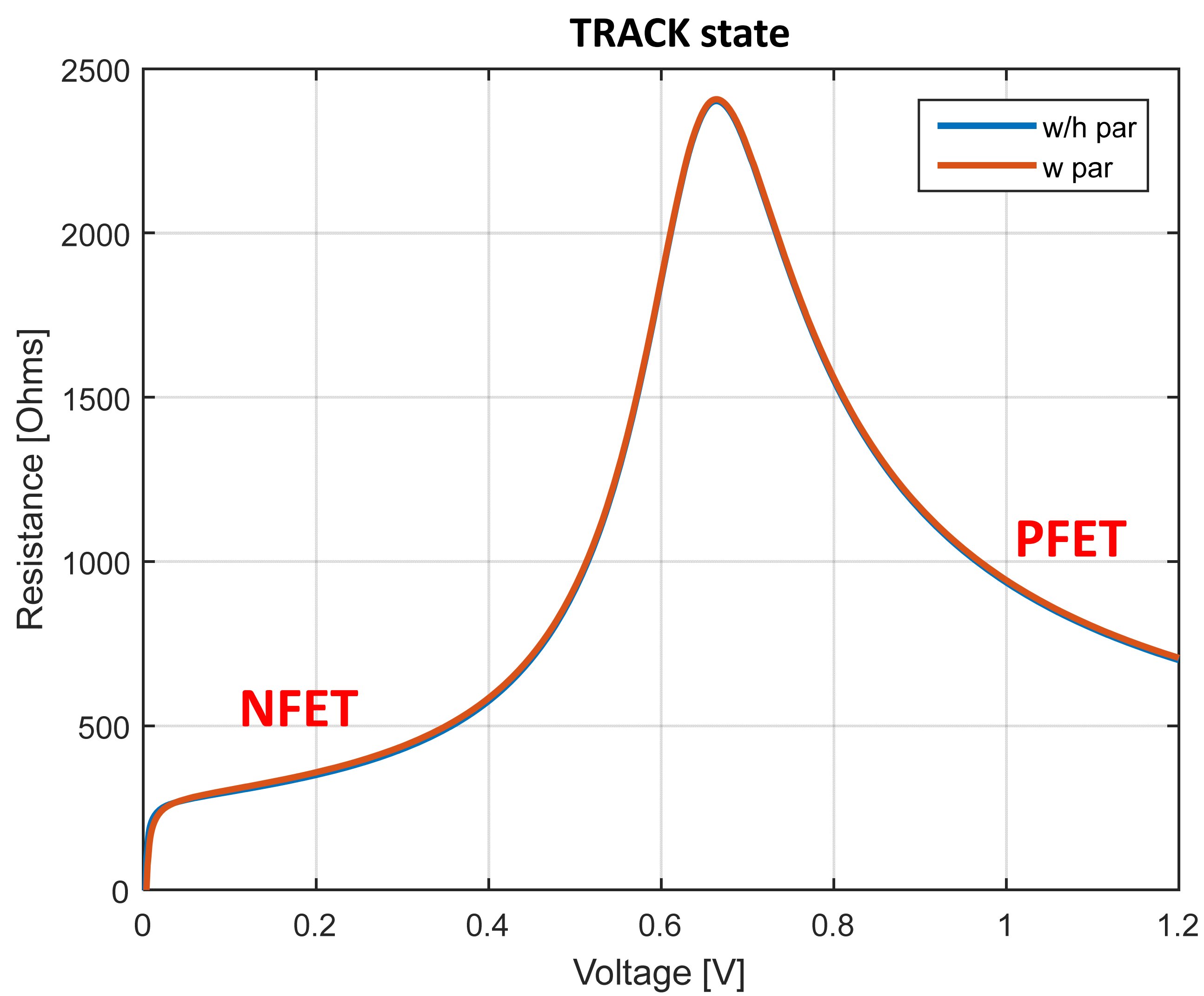
Montecarlo with process variation and mismatches shows a discrepancy between Csampling Schematic (13.5 fF) and Measured mean (20.27 fF).

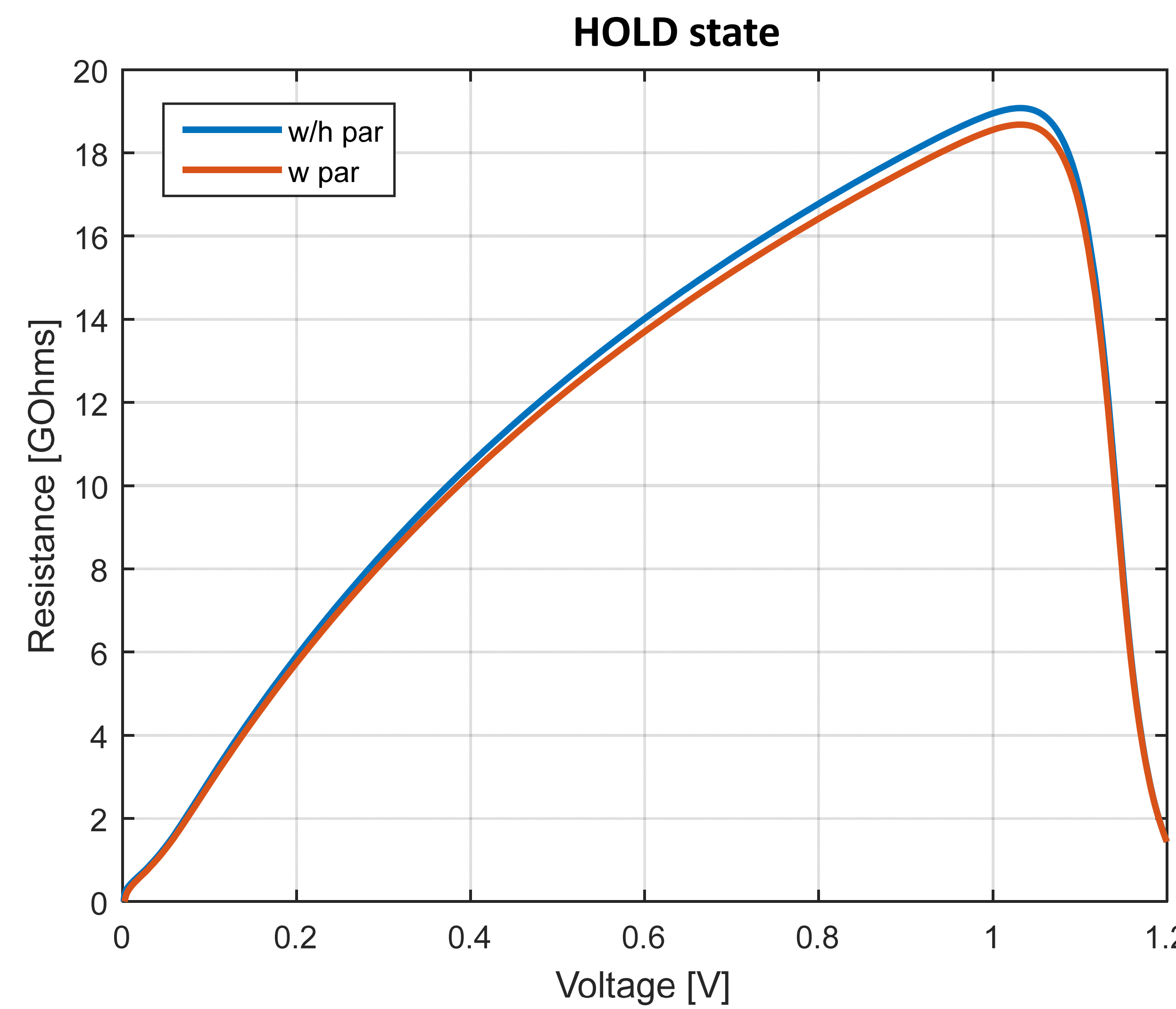
The Spread is about 1.9fF which makes the Capacitor tolerance at about 9.3%

Num. of Samp.	MEAN	STD	MIN	MAX
1000	20.27 fF	1.89 fF	14.86 fF	26.24 fF

PSEC4 Analysis: Single Sampling Cell

Switch resistance



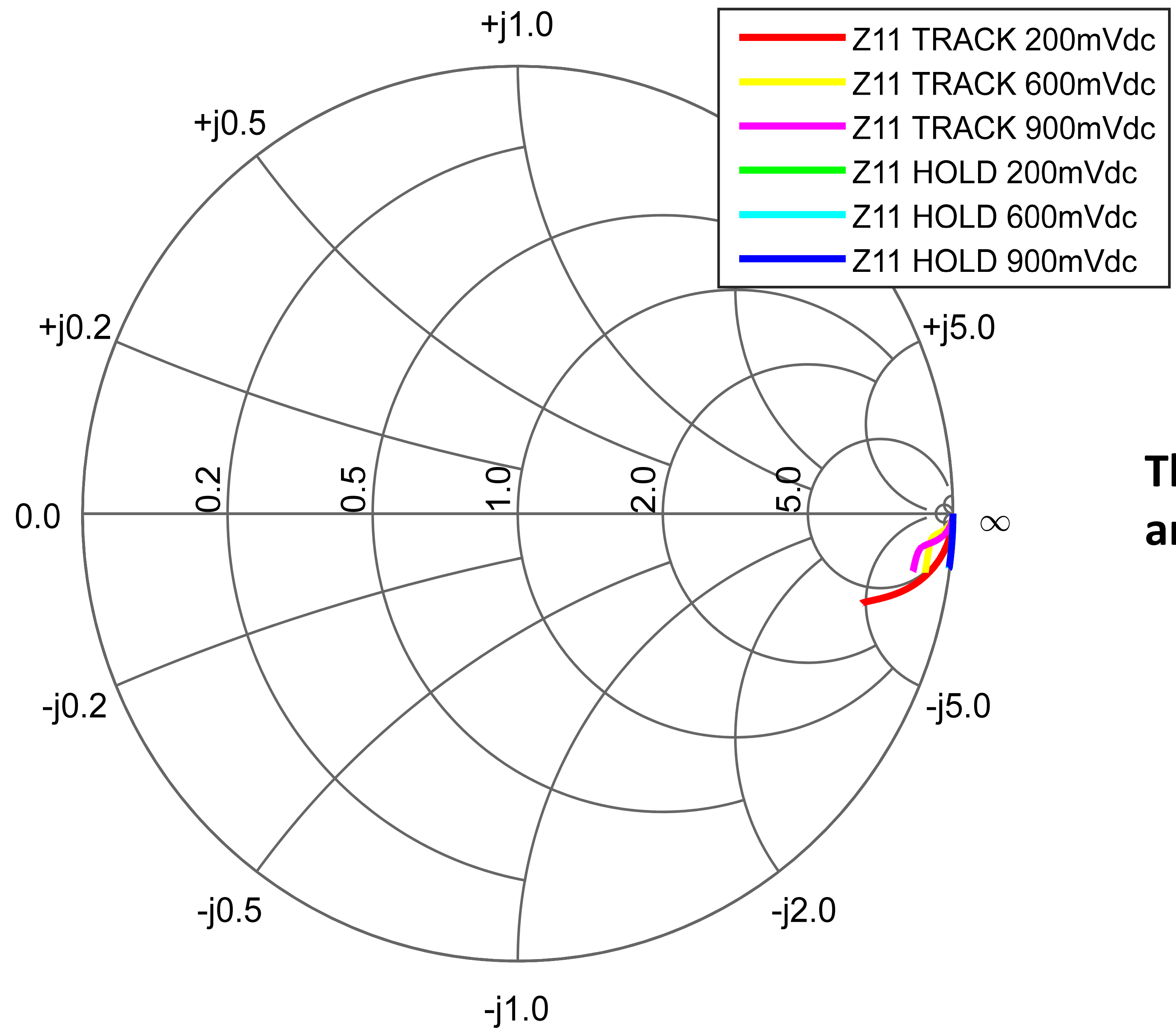


- **Ron=2.4k @665mVdc**
- **Roff is in GΩ**

- The PFET and NFET are not matched and Ron varies considerably

PSEC4 Analysis: Single Sampling Cell

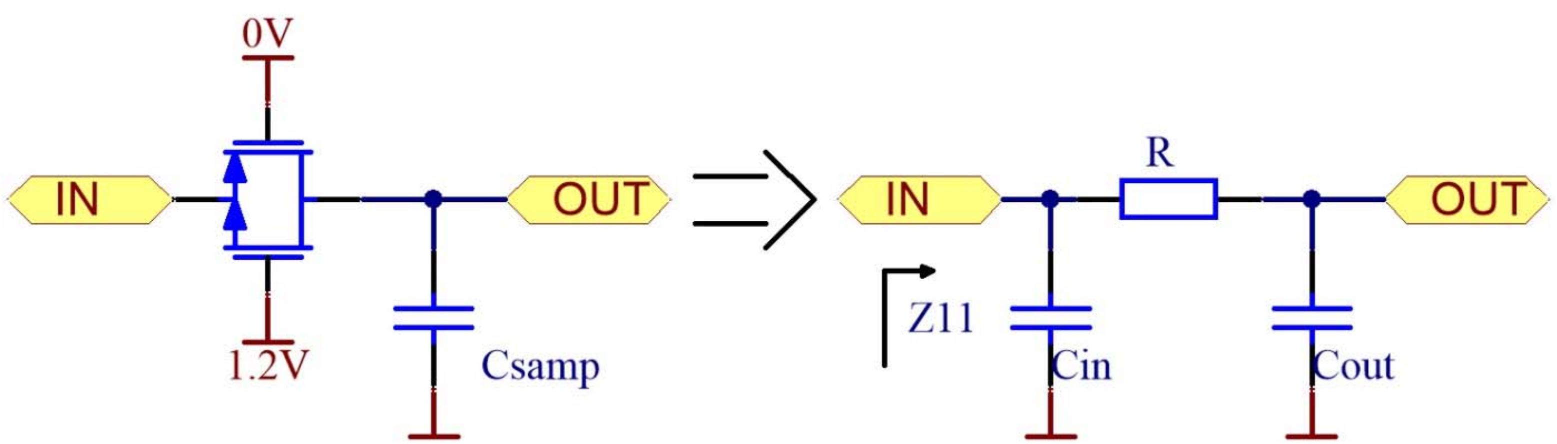
Performance: S(Z)-parameter



The input impedance is high and it is capacitive.

PSEC4 Analysis: Single Sampling Cell

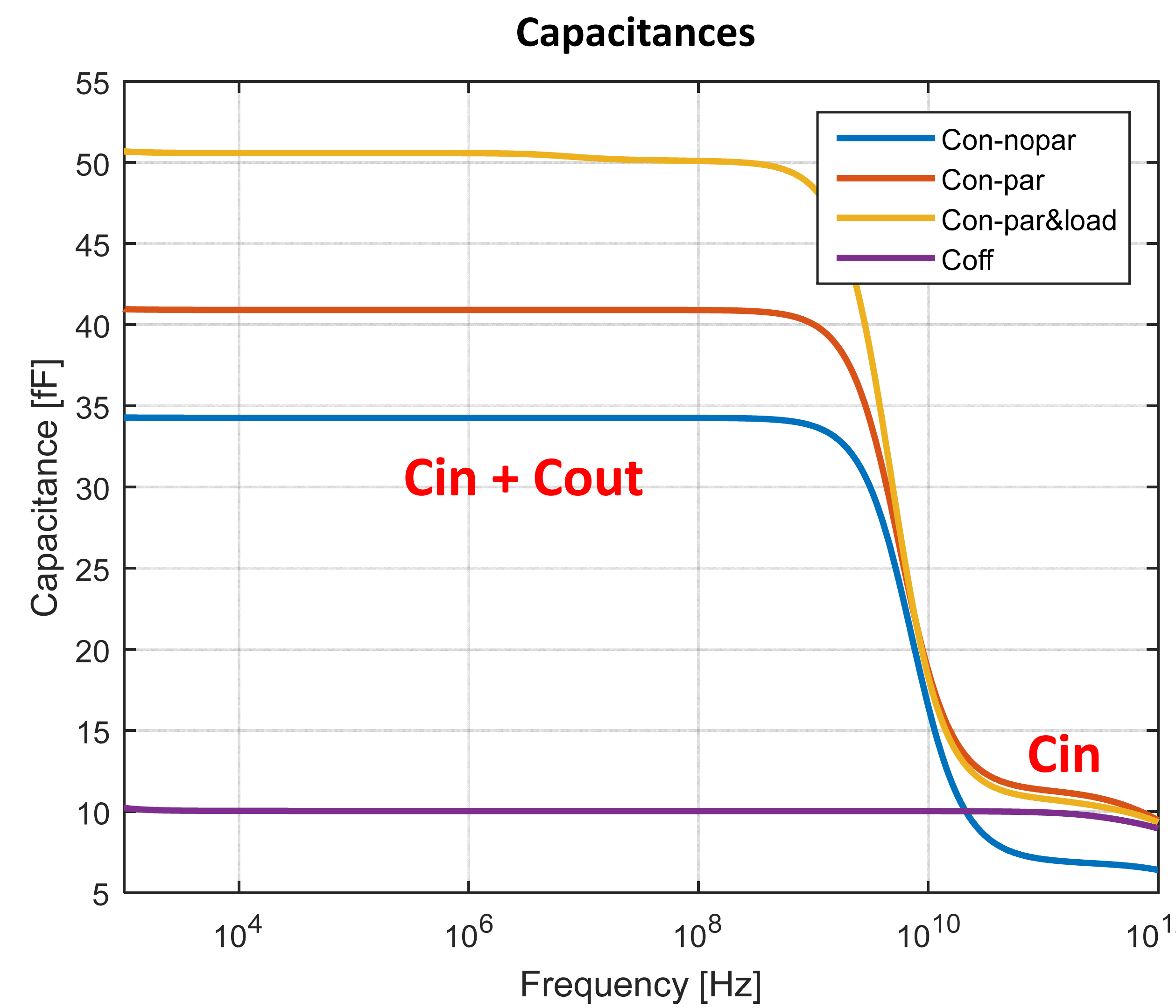
Transfer function & Parasitic Capacitances



$$Z_{11} = \frac{1 + sC_{OUT}R}{s^2 C_{IN} C_{OUT} R + s(C_{IN} + C_{OUT})}$$

The transfer function parts:

- input parasitic capacitance of the transistor plus capacitance of the transmission line section.
- Series resistance of the transistor channel (Rds)
- Output capacitance which is formed of the parasitic capacitance of the transistor, sampling capacitor and load capacitance

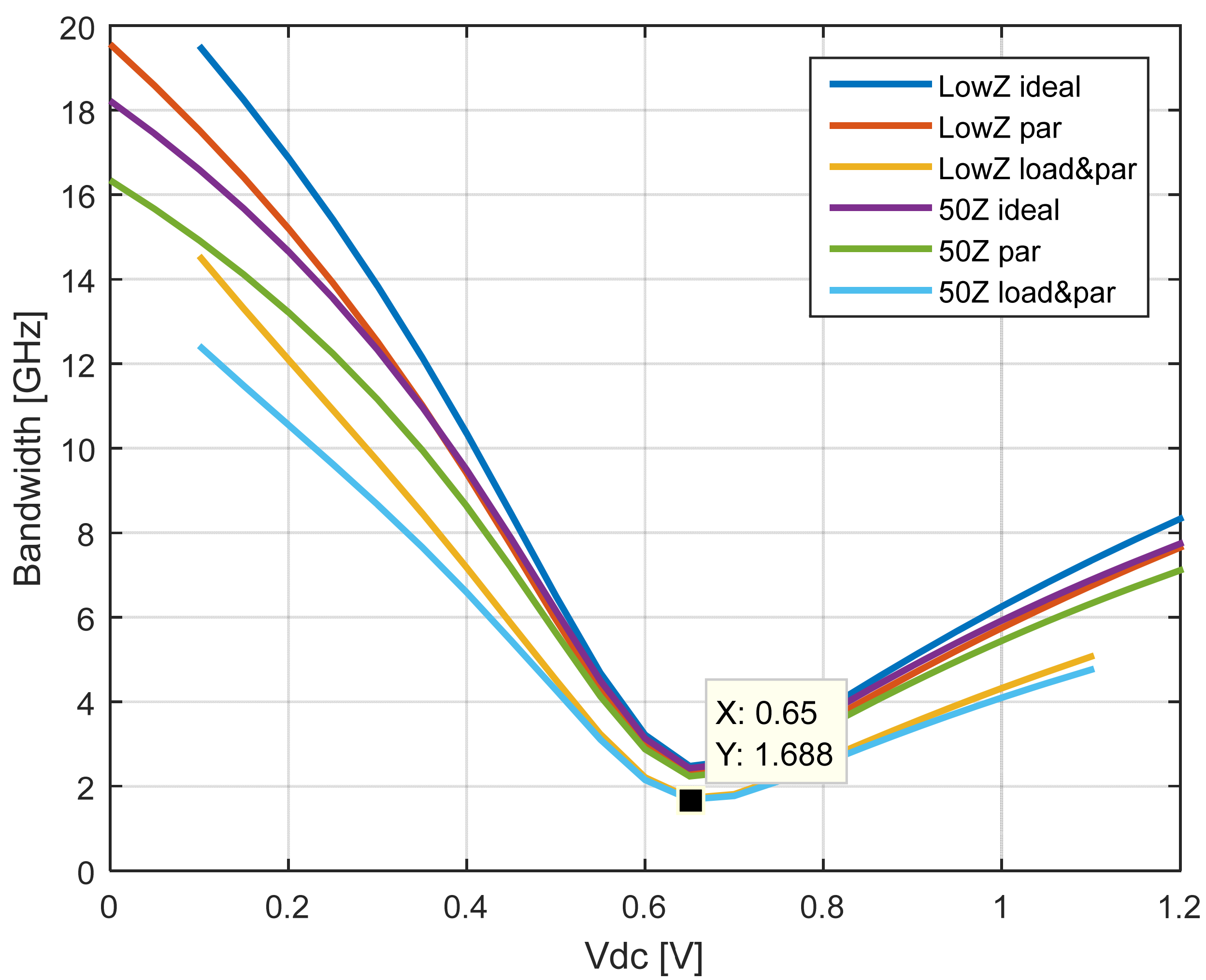


Capacitance	Value [fF]
Cin_open	8fF
Csw_out	10fF
Csamp	20.3fF
Cload	13fF

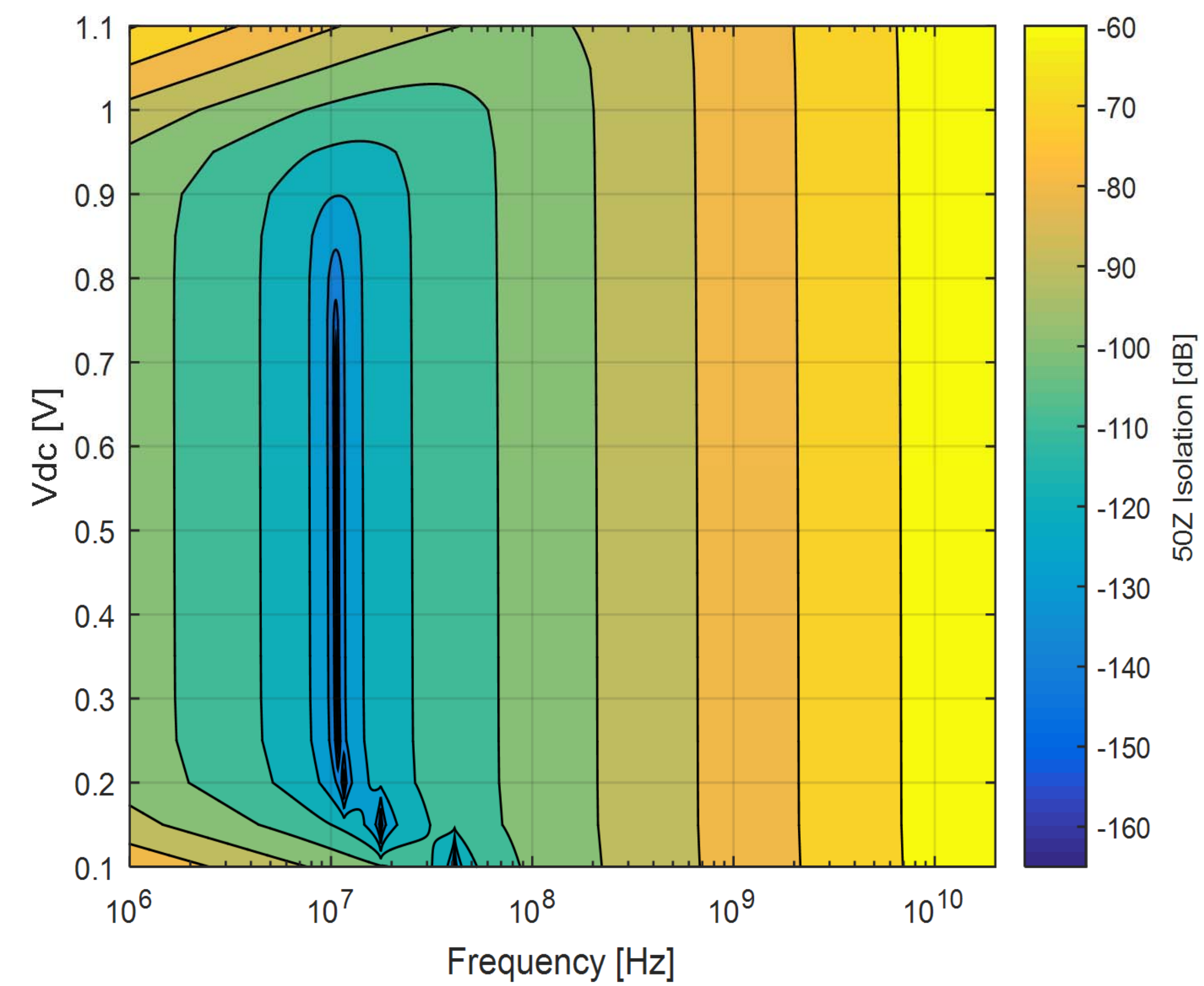
PSEC4 Analysis: Single Sampling Cell

Performance: Small Signal Frequency response, part1

Bandwidth



Isolation

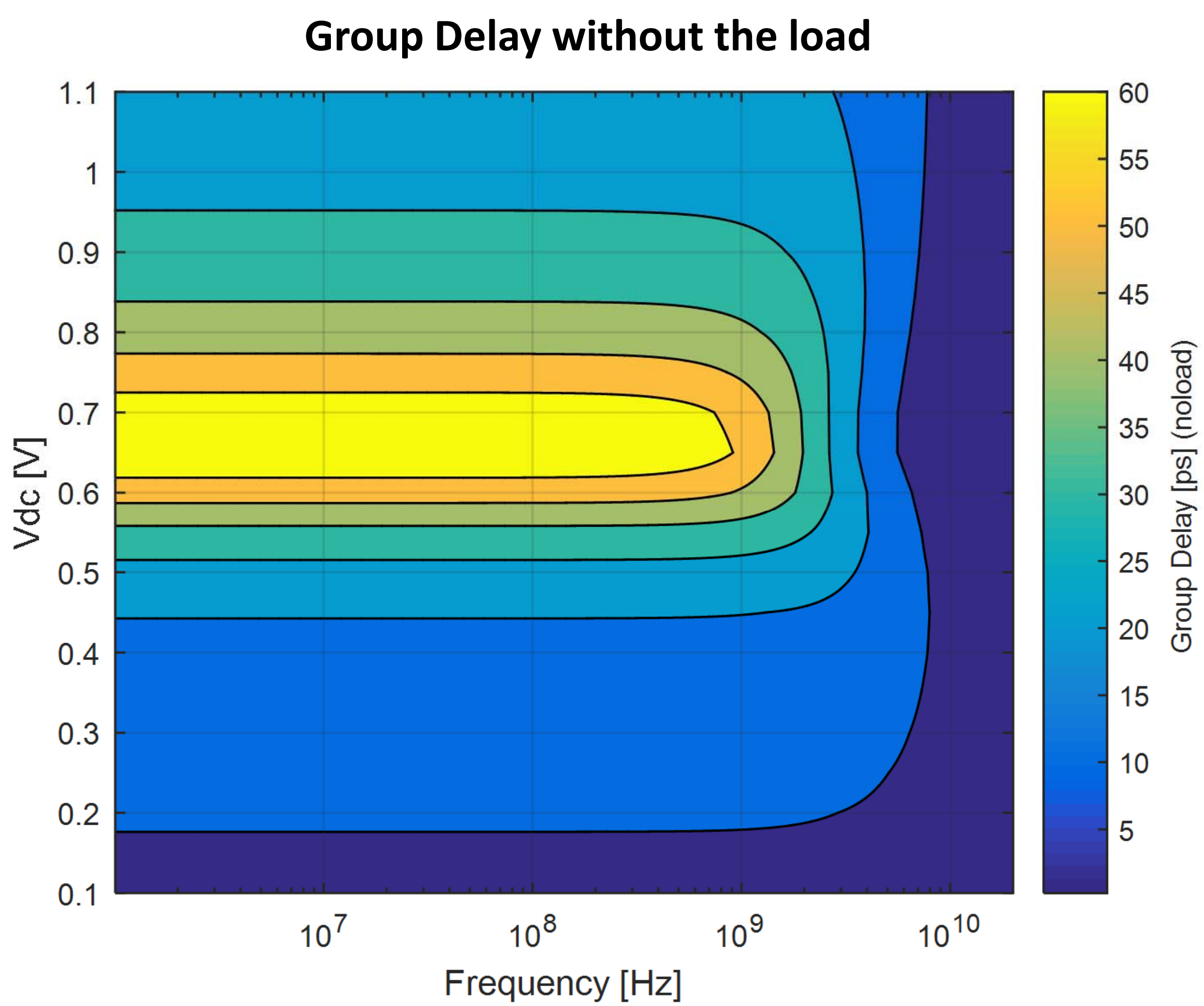


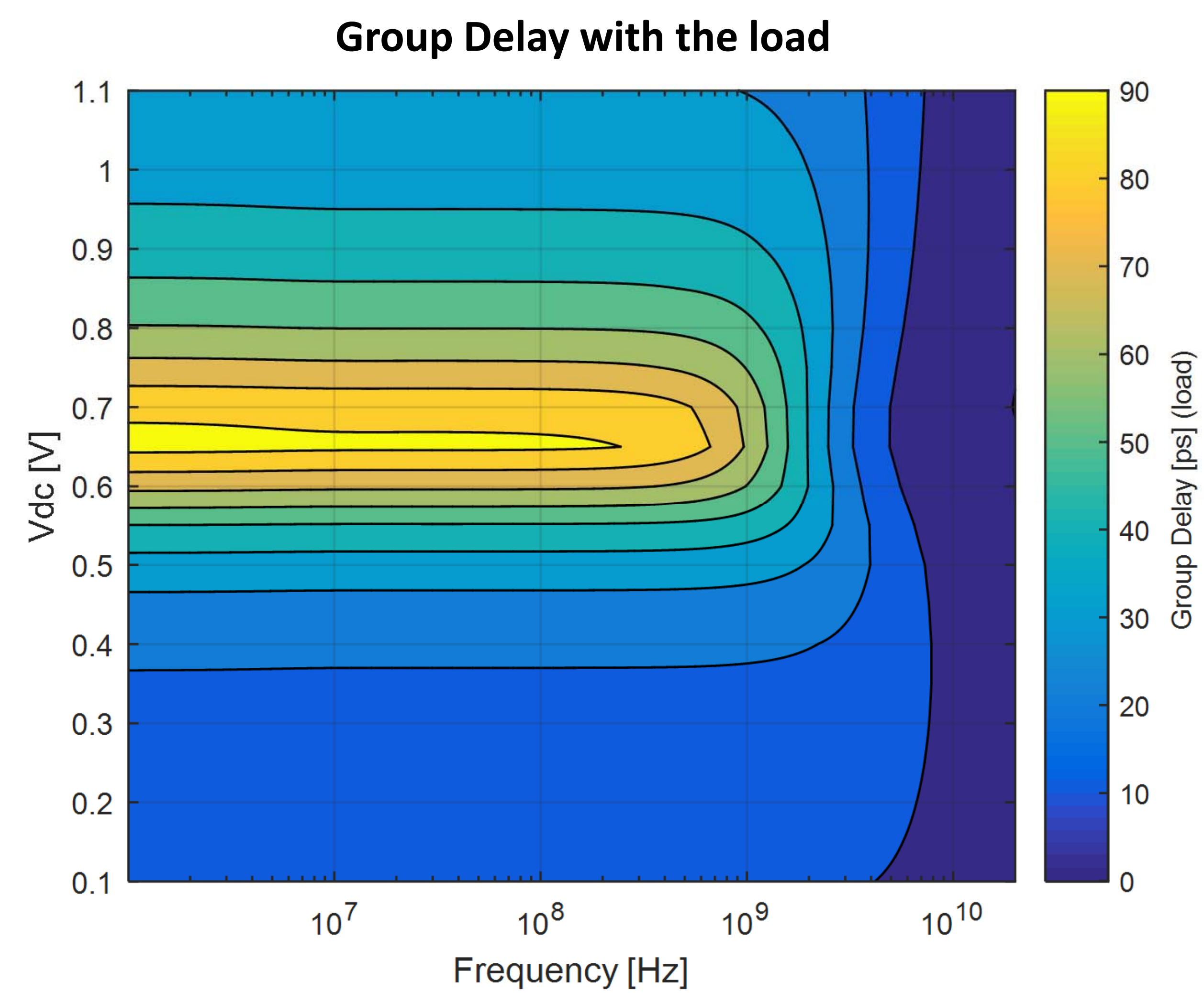
- **BWworst≈2.3GHz @665mVdc @LowZ drive**
- **BWworst≈1.7GHz @665mVdc @50Ω drive**

- **Isolation is over 60dB over all range**

PSEC4 Analysis: Single Sampling Cell

Performance: Small Signal Frequency response, part 2



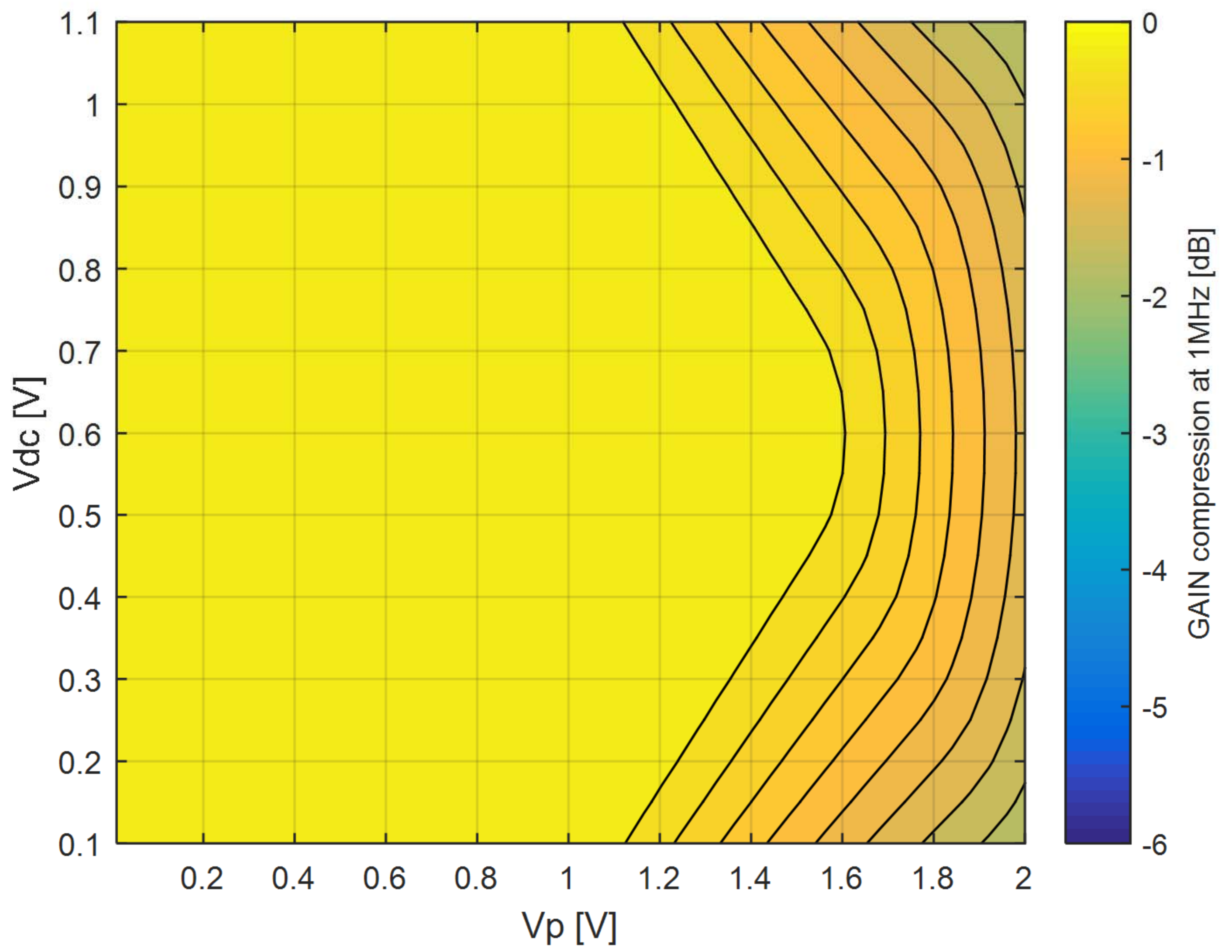


- **High Group delay variation which points to high distortion**

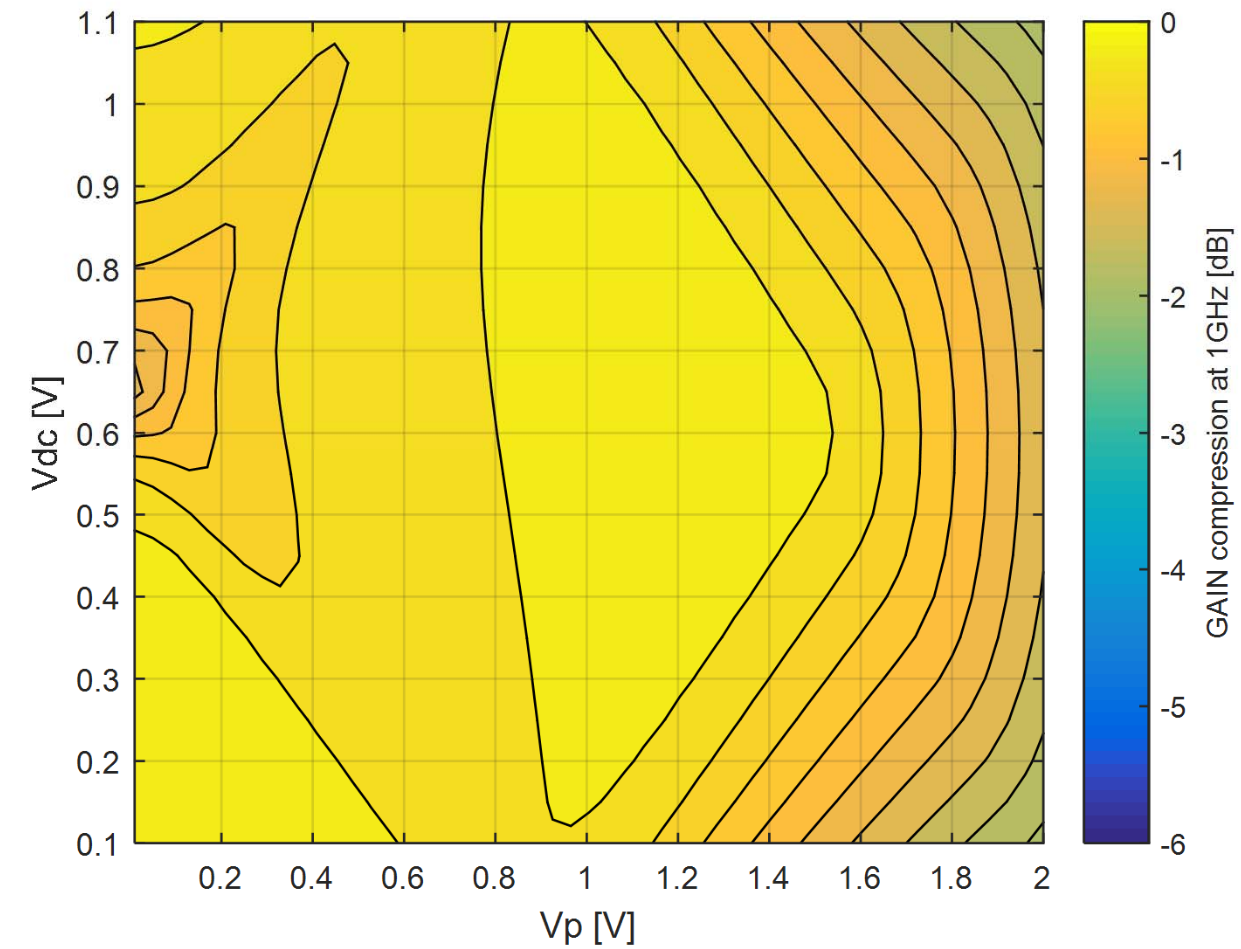
PSEC4 Analysis: Single Sampling Cell

Performance: Large Signal response, part 1

Low frequency gain compression



High frequency gain compression

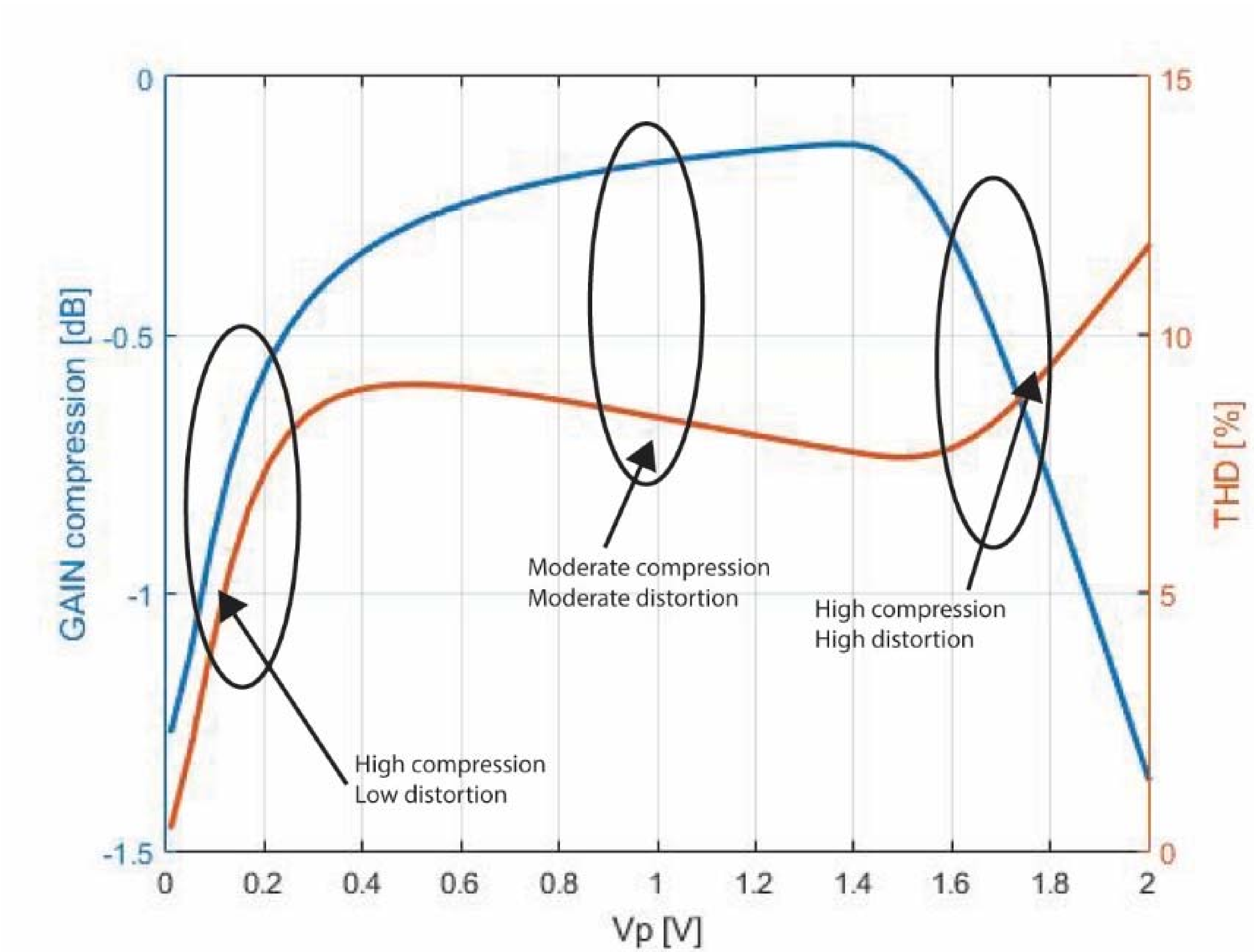


- **Full dynamic range at low frequency, compression appears when reaching the voltage threshold of the PN junctions at the drain/substrate barrier.**
- **Gain compression at lower and higher amplitudes**

PSEC4 Analysis: Single Sampling Cell

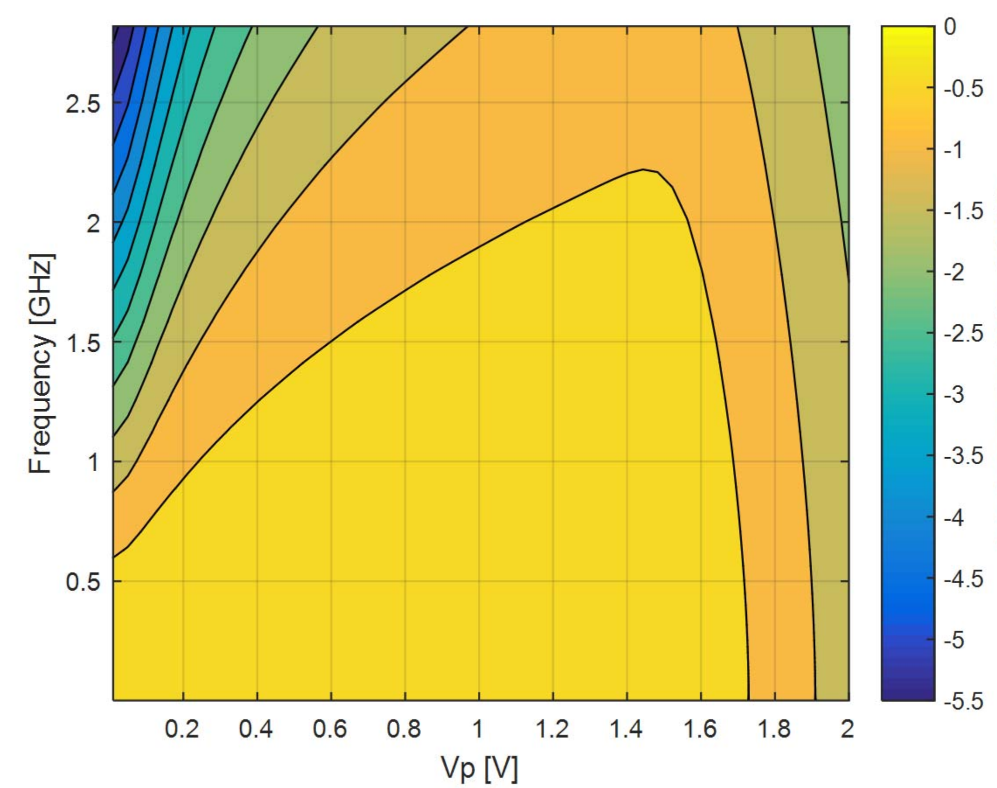
Performance: Large Signal response, part 2

High frequency gain compression & distortion



Three region of operation:

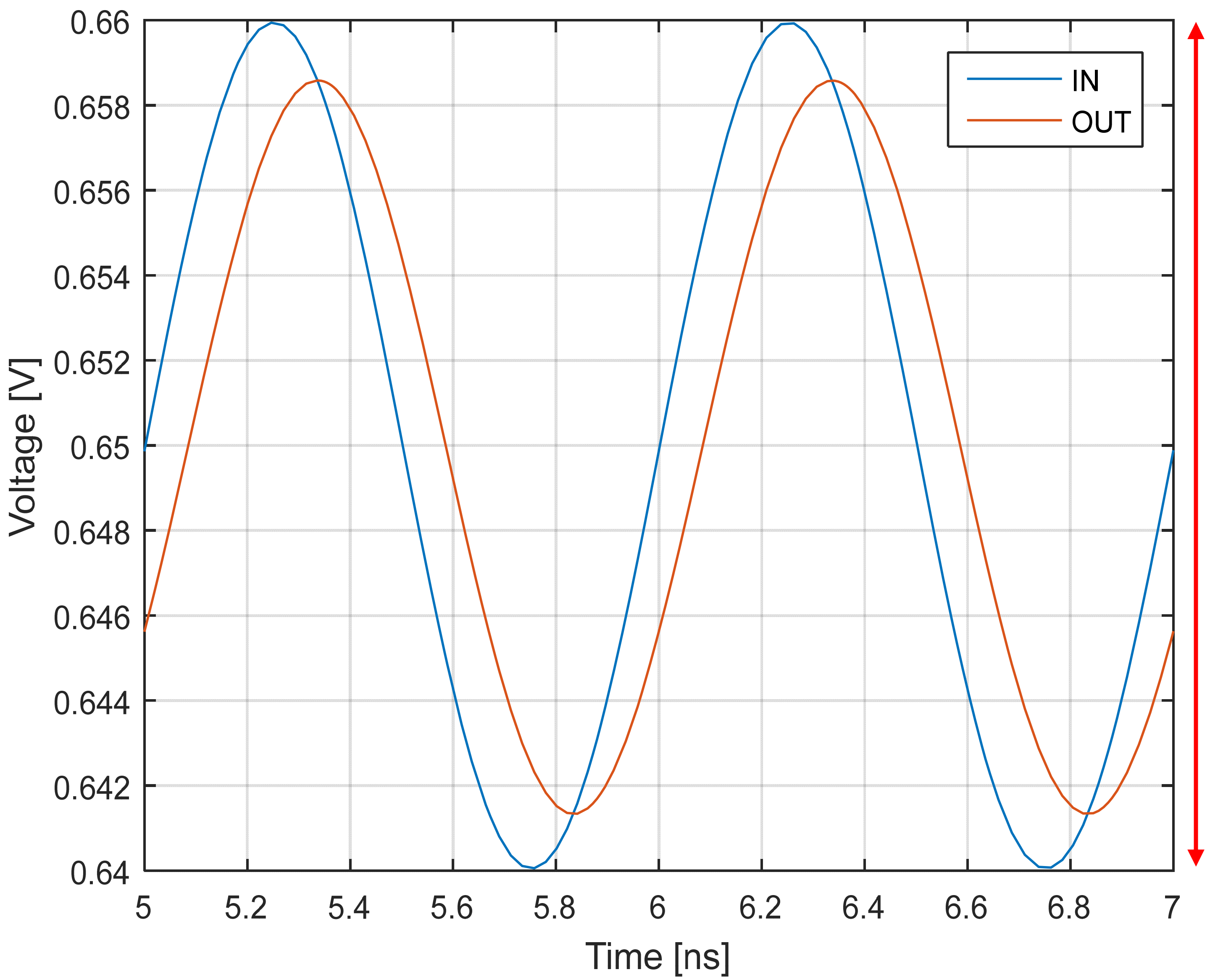
- **Low distortion & High compression**
- **Moderate distortion & Moderate compression**
- **High distortion & High compression**



PSEC4 Analysis: Single Sampling Cell

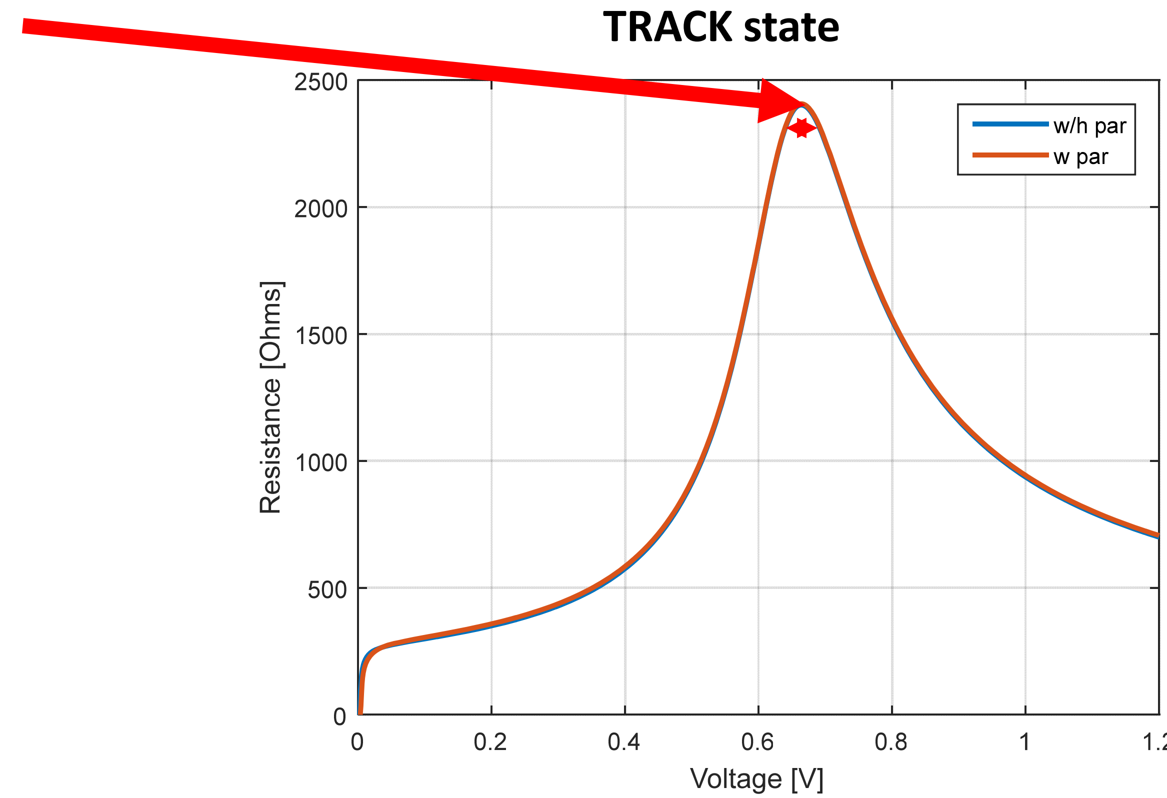
Performance: Large Signal response, part 3

Low distortion & High compression



- **Resistance of the channel does not vary much -> Low distortion**
- **At high resistance the bandwidth is limited -> lowering of the gain (compression)**

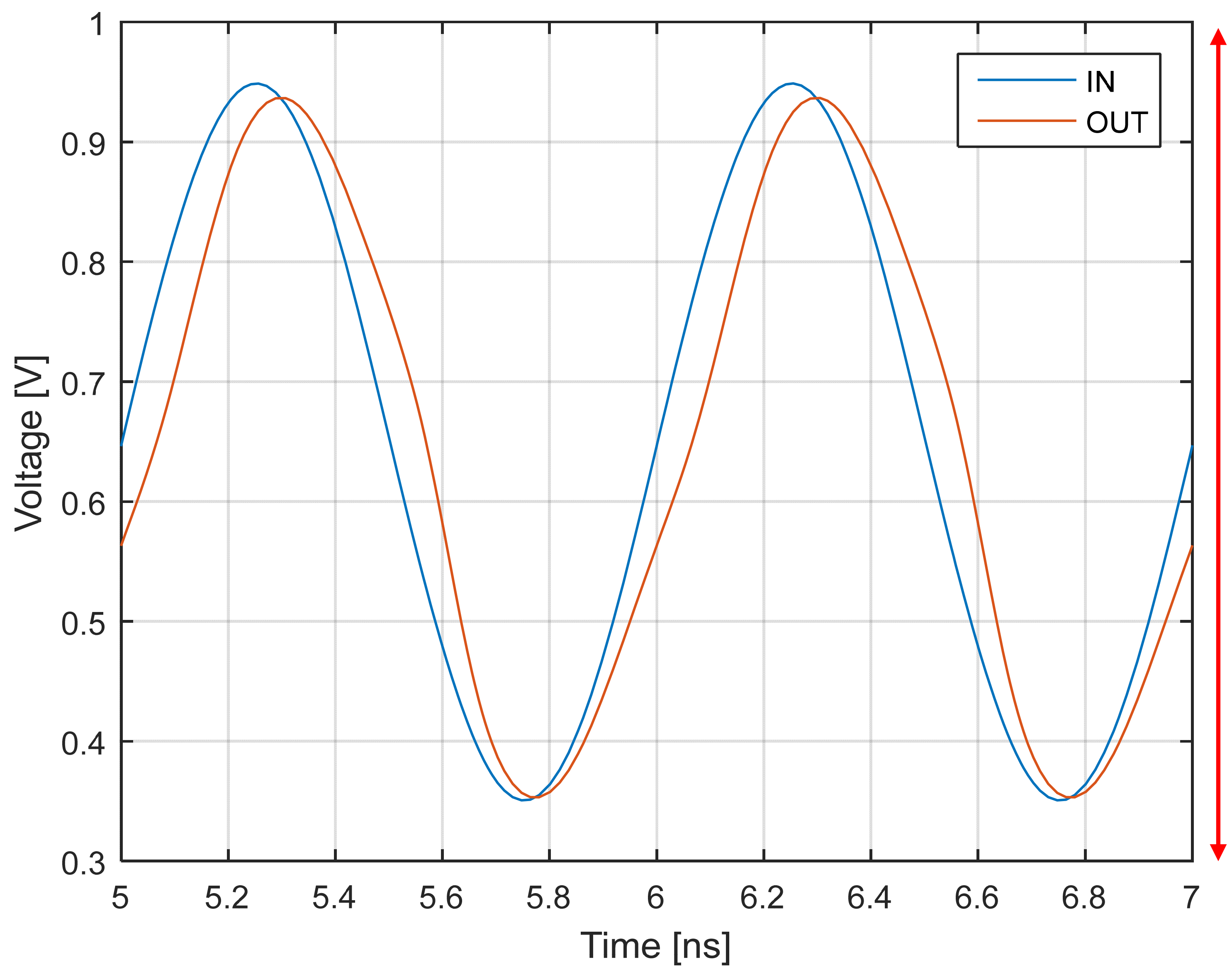
TRACK state



PSEC4 Analysis: Single Sampling Cell

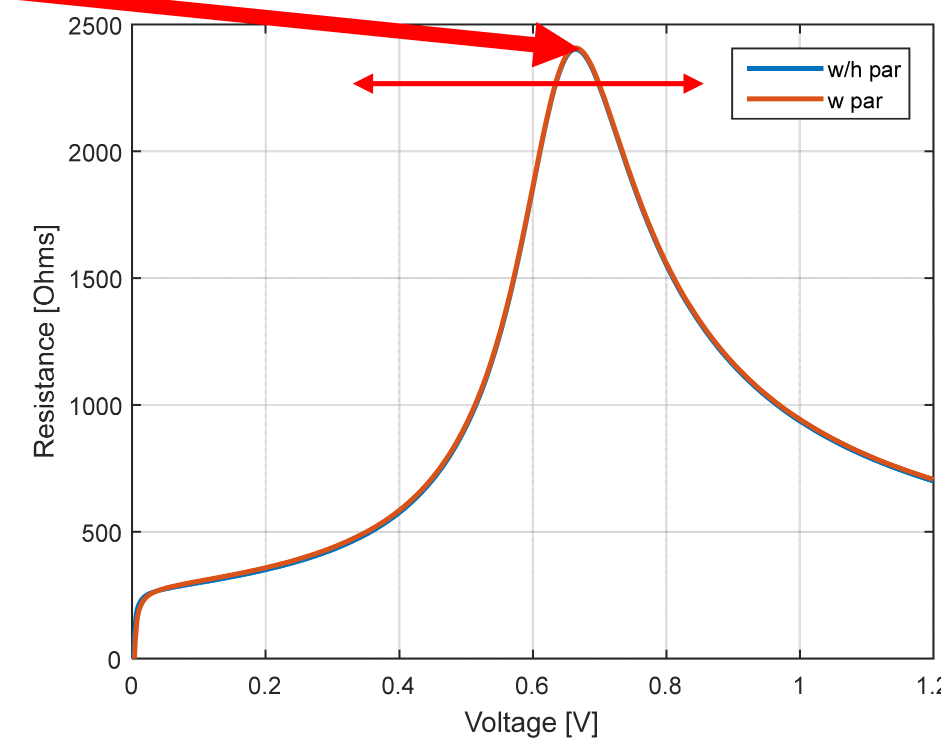
Performance: Large Signal response, part 3

Moderate distortion & Moderate compression



- **Resistance of the channel is varying**
  -> The bandwidth at instantaneous values of the incident voltage waveform is different
  - **-> In frequency domain this gives rise to higher harmonics which interfere constructively hence increasing the overall signal amplitude but also increasing distortion**

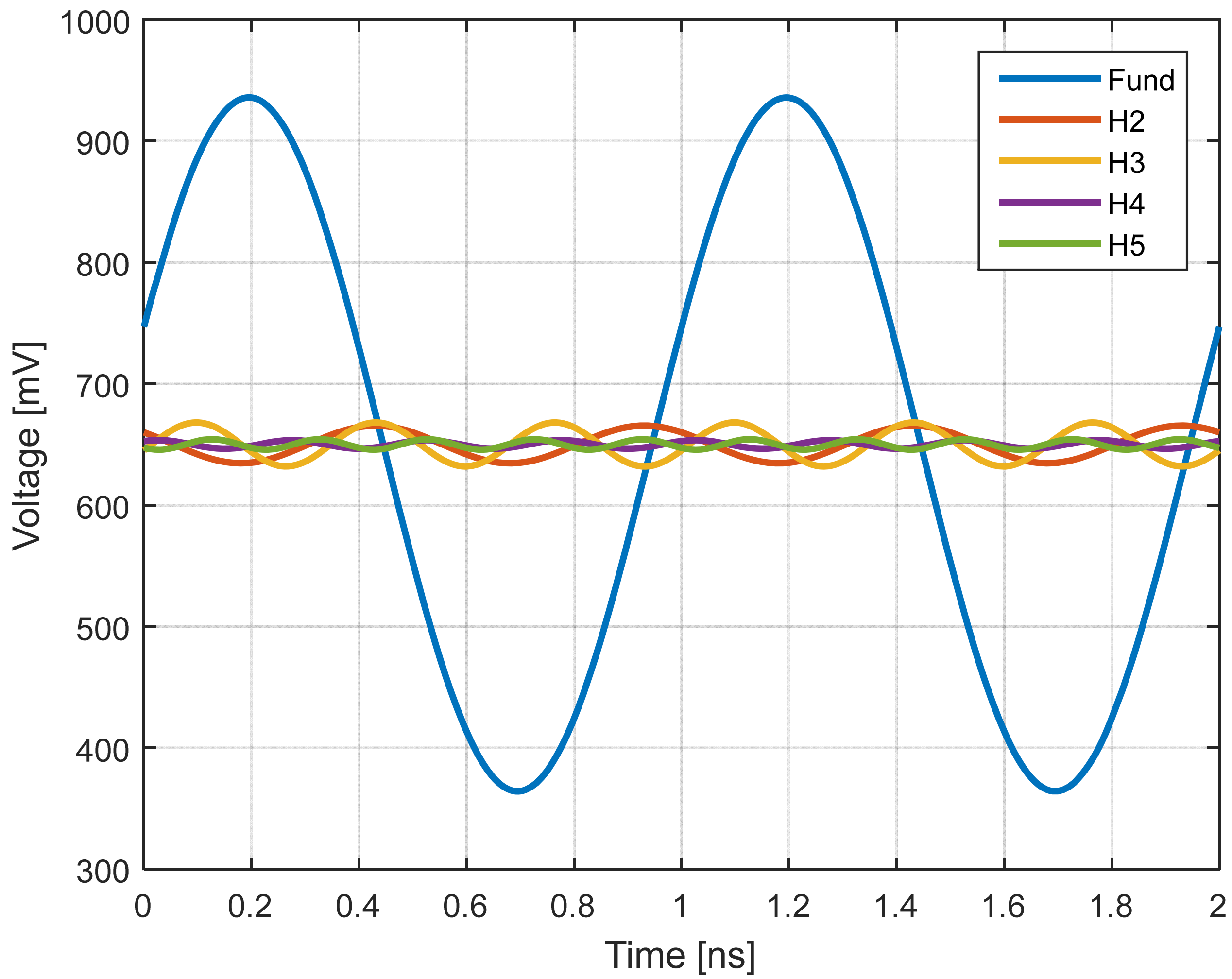
TRACK state



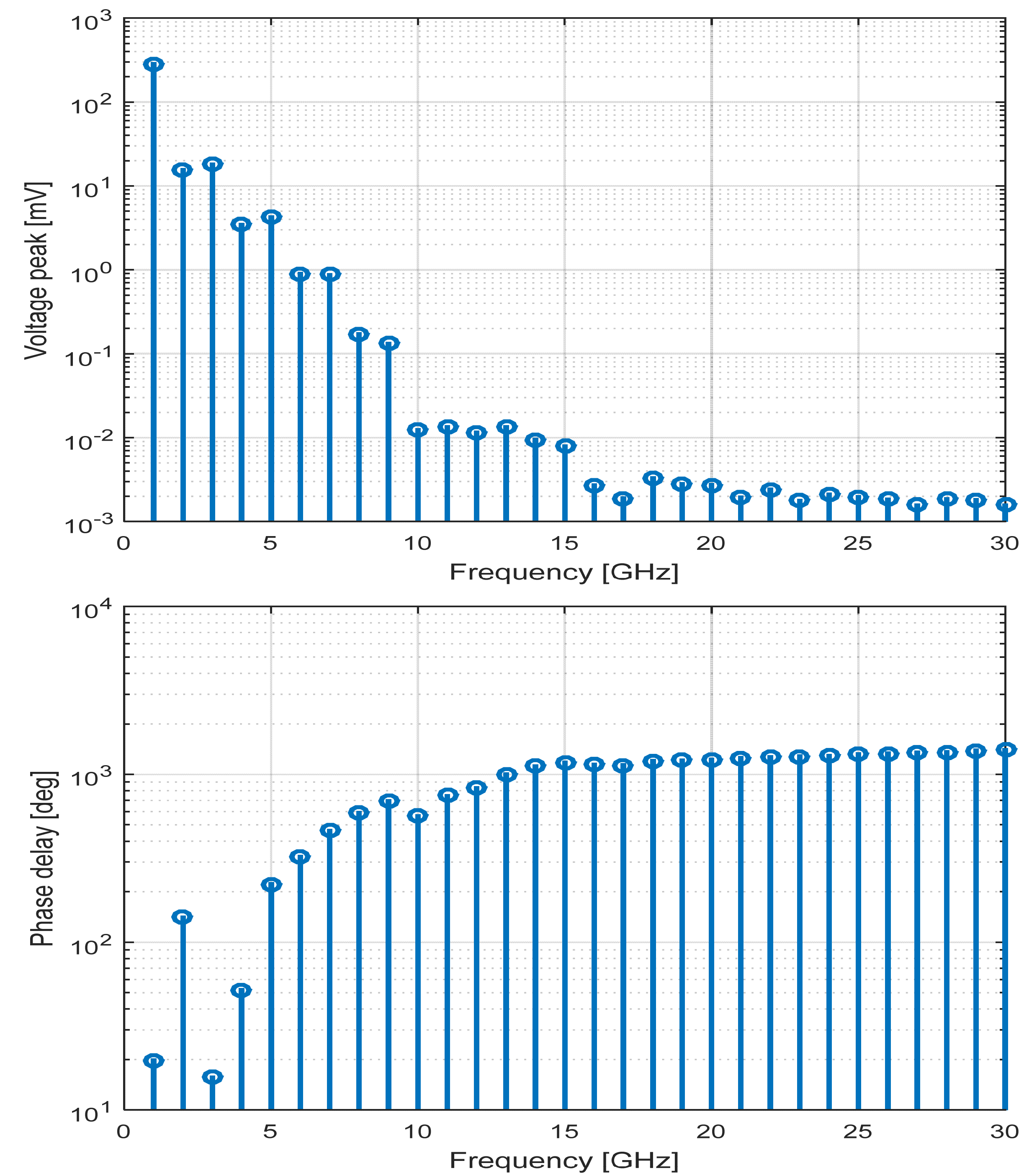
PSEC4 Analysis: Single Sampling Cell

Performance: Large Signal response, part 4

Time domain decomposition



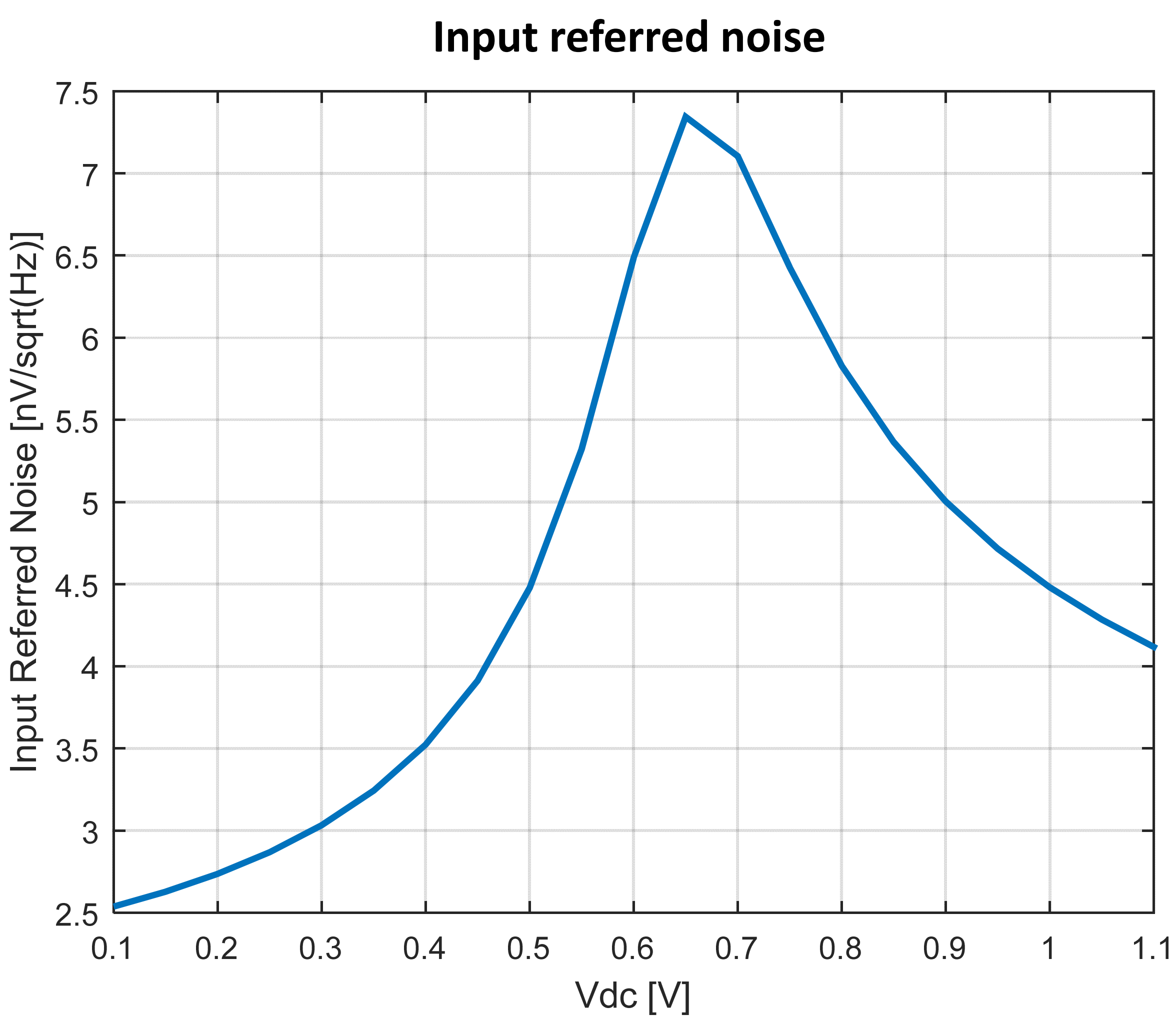
Frequency domain decomposition

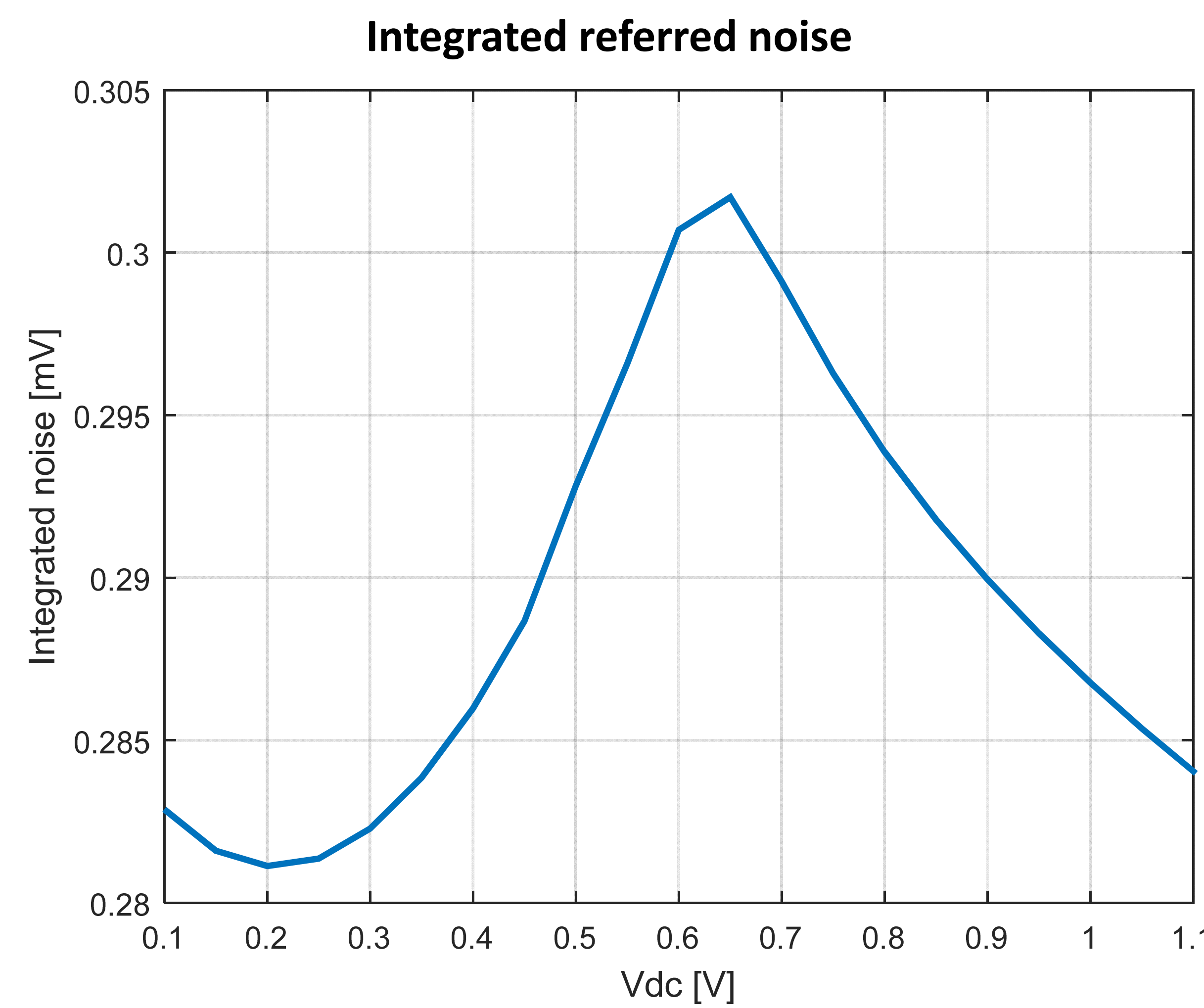


- **Constructive interference of odd harmonics and destructive interference of even harmonics at the peaks**
- **Constructive interference of second and third harmonic at zero crossing**

PSEC4 Analysis: Single Sampling Cell

Performance: Noise & Distortion, part 1

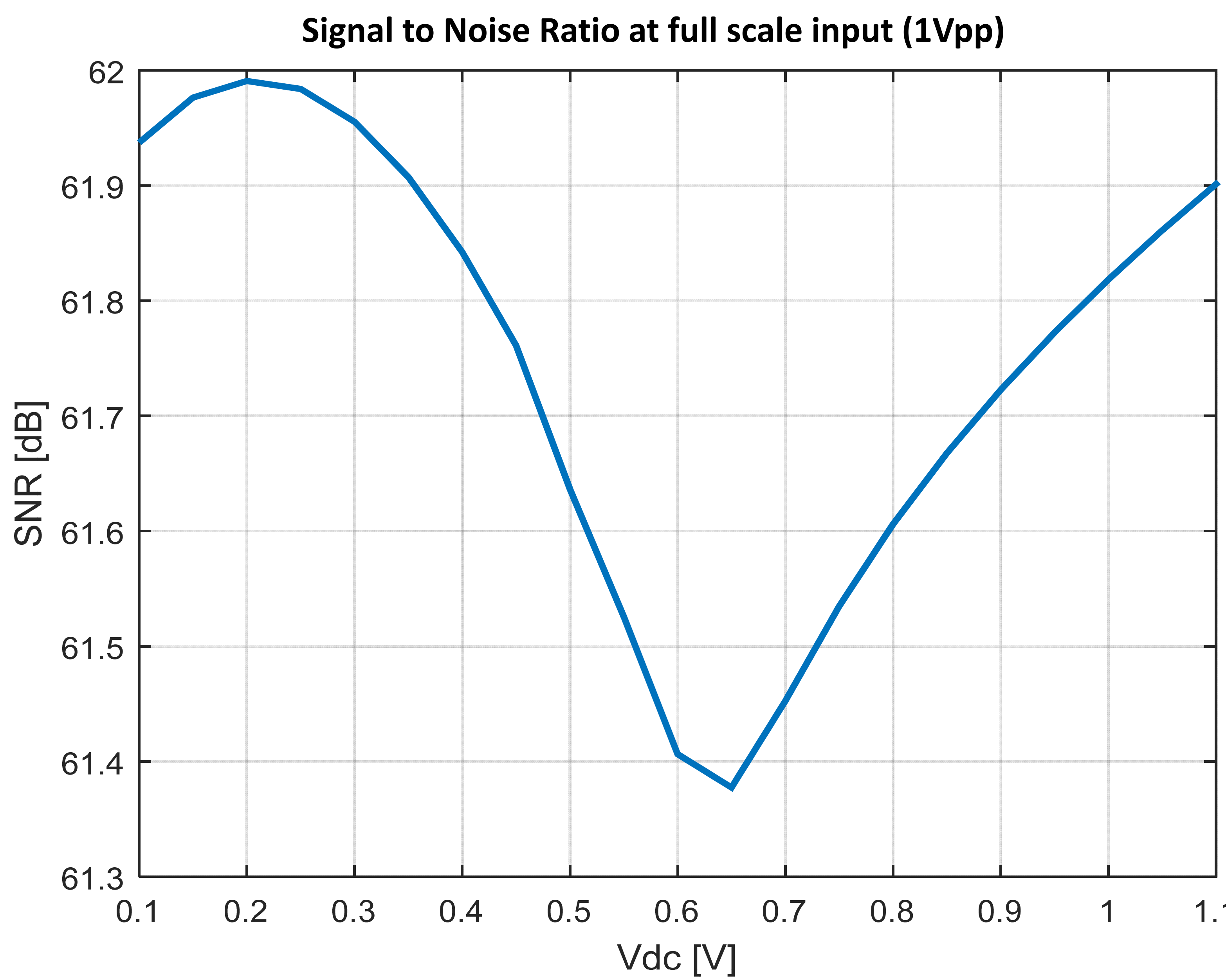




- **Noise dominated by the ON resistance of the channel**
- **Total noise is around 0.29mV ± 0.01 mV**

PSEC4 Analysis: Single Sampling Cell

Performance: Noise & Distortion, part 2

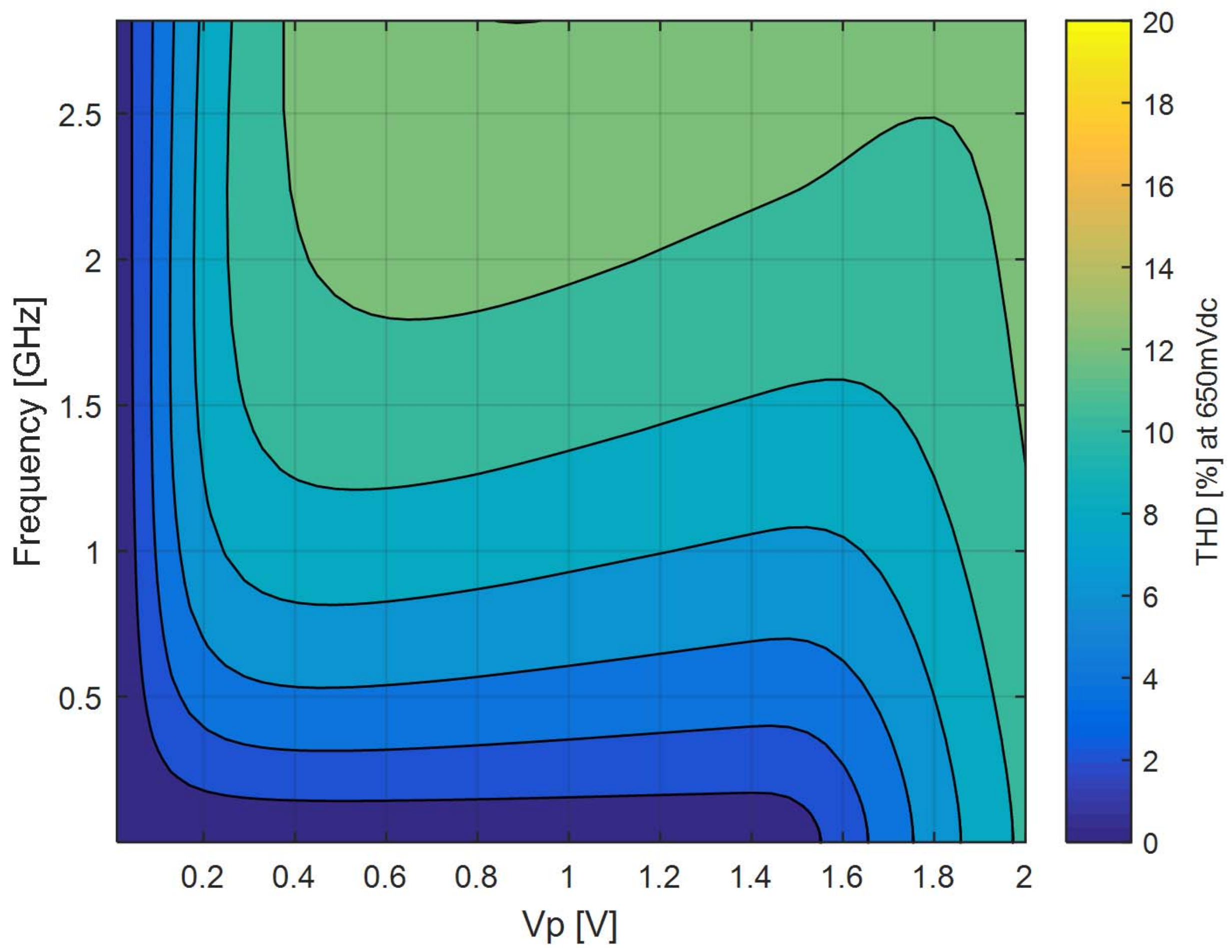


- **SNR is around 61.7dB ± 0.3 dB**

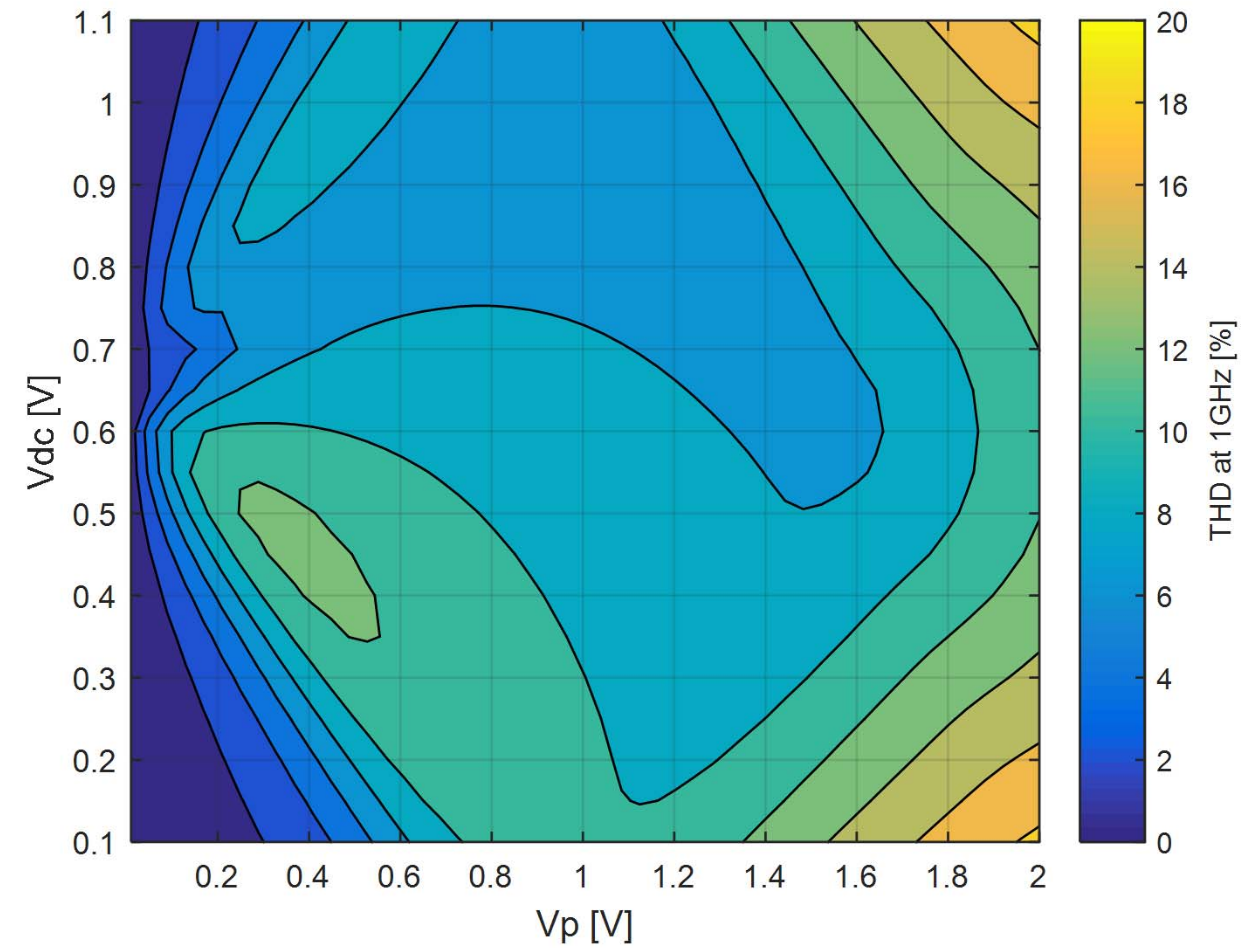
PSEC4 Analysis: Single Sampling Cell

Performance: Noise & Distortion, part 3

Distortion at fixed Vdc



Distortion at fixed Frequency



- **Most of the distortion comes from the Ron variation over the input voltage range**

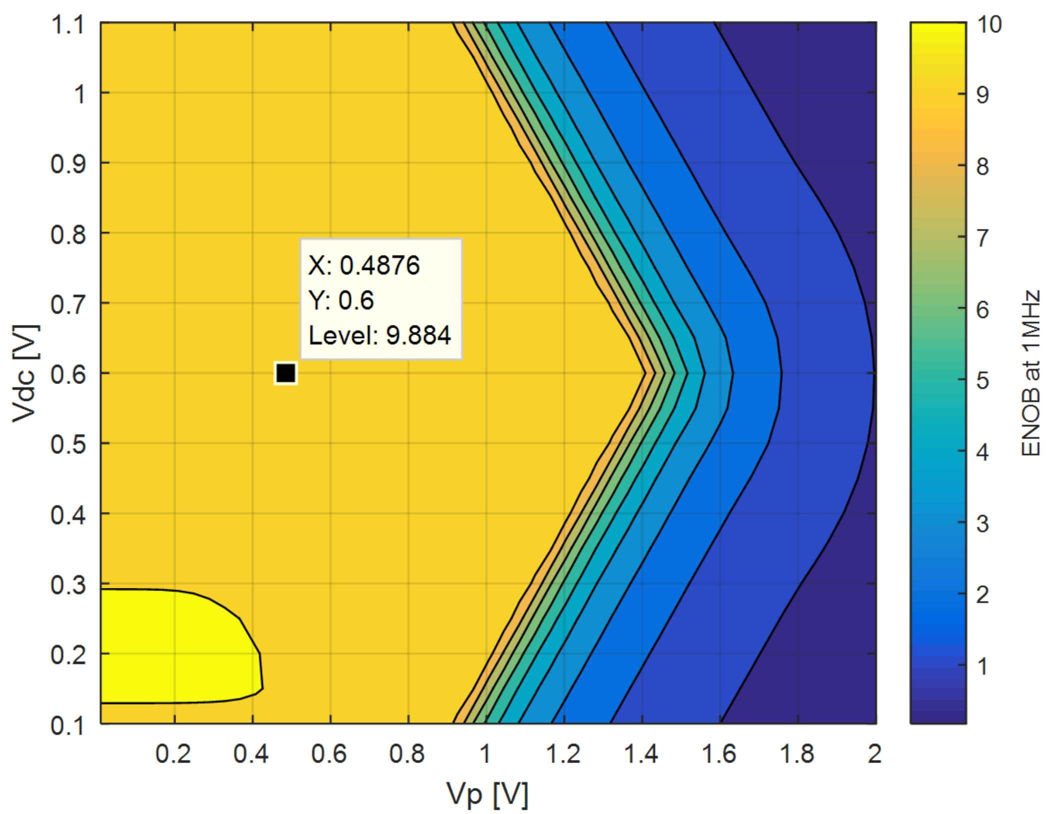
PSEC4 Analysis: Single Sampling Cell

Performance: SINAD & ENOB

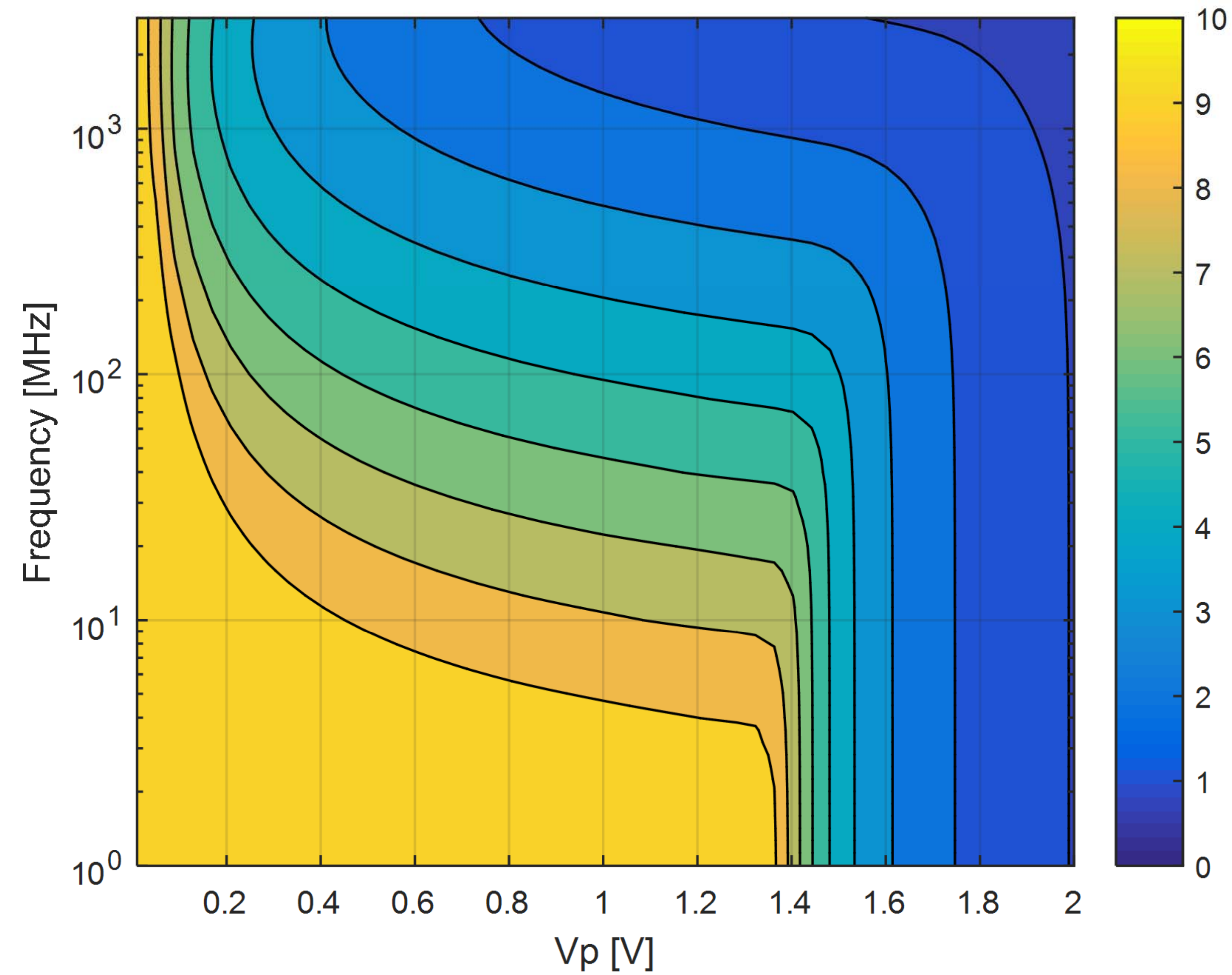
$$SINAD = -10\log_{10}\left[10^{-\frac{SNR}{10}} + 10^{-\frac{THD}{10}}\right]$$

$$ENOB = \frac{SINAD - 1.76 + 20\log_{10}\left(\frac{Fullscale}{Input}\right)}{6.02}$$

ENOB at low frequency



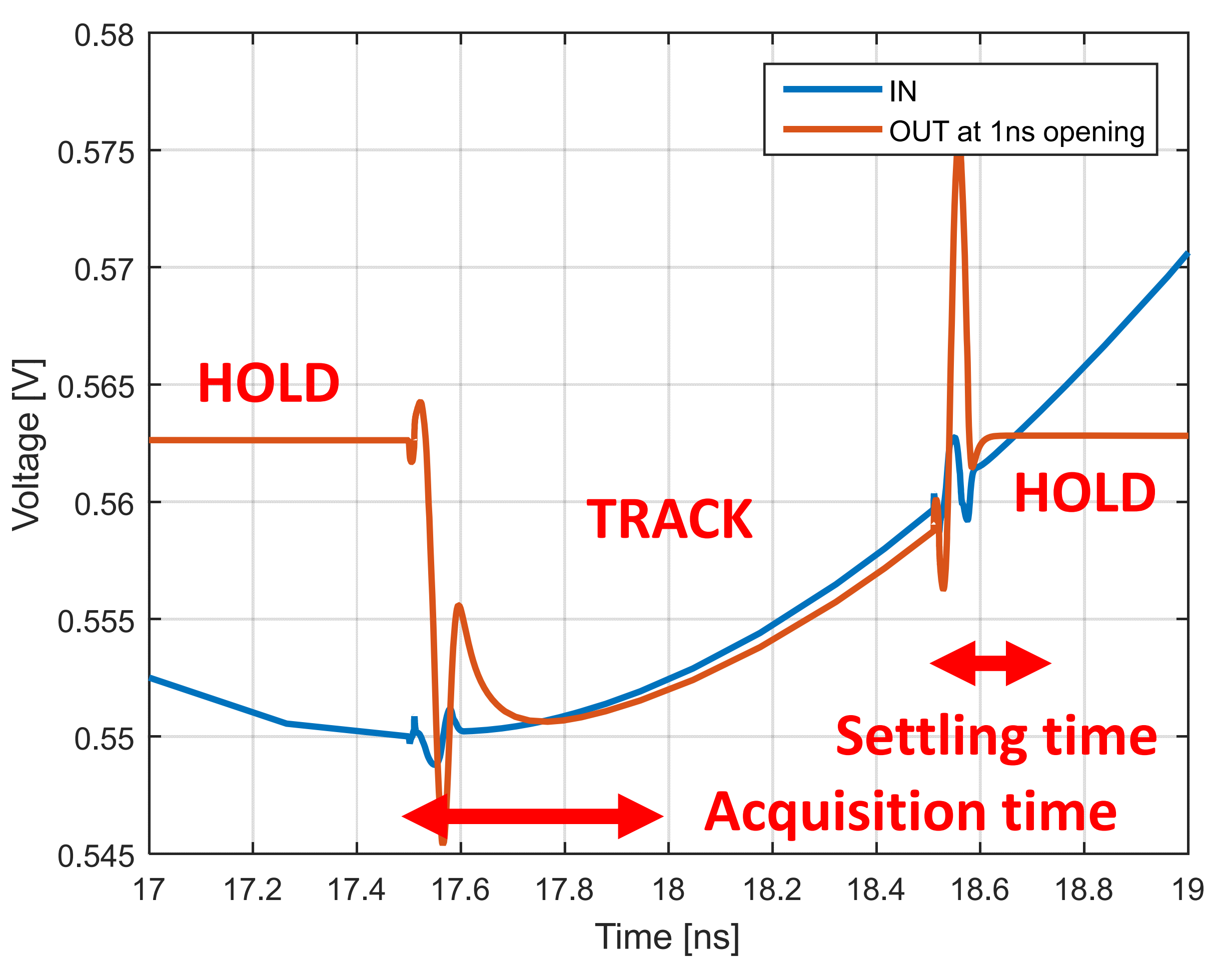
ENOB versus frequency

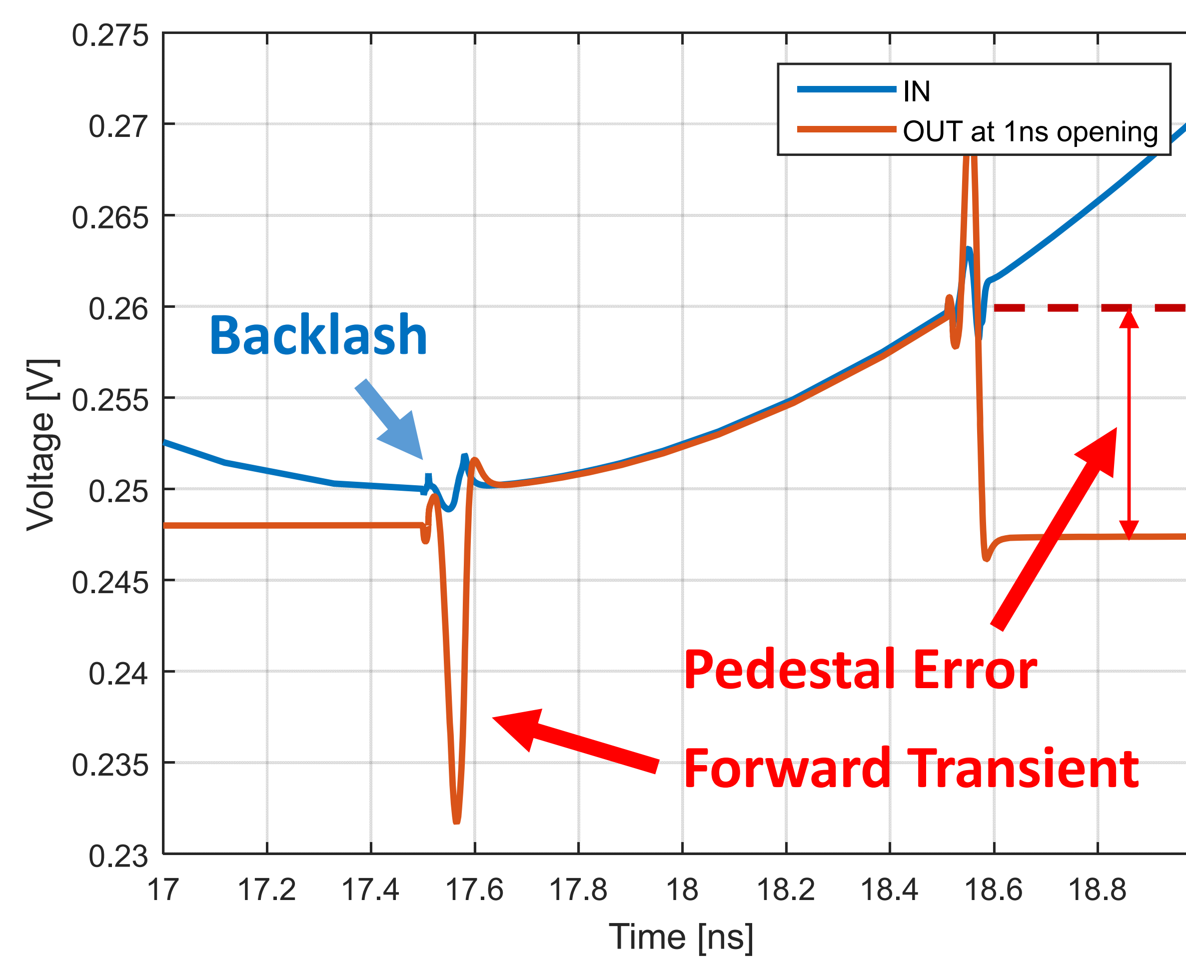


- ENOB DOMINATED BY DISTORTION!

PSEC4 Analysis: Single Sampling Cell

Performance: Transient response





Input Vdc voltage	Acquisition time	Settling time
300mV	0.14ns	0.11ns
600mV	0.68ns	0.11ns
900mV	0.52ns	0.11ns

- Worst case window time is 0.8ns or 1.25GHz -> due to low bandwidth
- Best case is 0.25ns or 4GHz

- 15% backlash at 30mV forward transient
- Pedestal error due to charge injection and transistor mismatch dominate

Summary

Comparison with requirements

Parameter	Measured (worst cases)	Requirements
Speed (sampling frequency)	1.25GHz (No overlapping)	20GHz
Bandwidth (Single cell)	1.7GHz @665Vdc @50Ω	3GHz
Bandwidth (Multi cell)	1.0GHz @665Vdc @50Ω	3GHz
SNR	61.7 dB	58dB
ENOB	9.8 bits (very small region)	9.4 bits

Things to improve:

- **Reduce Ron variance over the dynamic range to reduce distortion and increase the ENOB**
- **Bandwidth dominated by Cin:**
  - **Reduce Cin or reshape the channel to increase the bandwidth (first pole)**
  - **Reduce Ron overall value to increase the bandwidth (second pole)**
- **Speed dominated by bandwidth:**
  - **Increase bandwidth**
  - **Overlapping of sampling cell windows to increase the effective sampling frequency**
- **Use differential configuration to reduce pedestal error and increase noise coupling and crosstalk immunity**