Vivado Makefile System

- Combination of makefiles and tcl scripts that locate relevant sources and cores and compile for a specific target.
- Some typical commands:
  - make test
    - Verifiy that all sources are properly located.
  - make gui
    - Launch your target project in the Vivado GUI.
  - make
    - Compile your entire target through to .bit and .mcs*

      *Note that mcs generation uses promgen which, for now, still requires ISE. ☹
- Current status:
  - Linux only (developed under RHEL 5.10).
  - Using Vivado 2014.1 but known to work under 2013 revisions as well.
  - Tested on idlab server (CentOS 5.10) and required no special changes beyond a working Vivado installation*.
- Using it as-is will require some tweaks to the directory structure we previously discussed…

Proposed Directory Structure

<repo>/trunk/firmware

<repo>/trunk/firmware/modules/ <- most HDL lives in subdirectories here

modules/SlacStdLib <- proposed softlink to “official” copy of distributed lib

modules/IRSXControl

modules/…

<repo>/trunk/firmware/targets

targets/SCROD.revB

targets/SCROD.revB/Version.vhd <- this file sets a register readable version number

targets/SCROD.revB/hdl <- includes top level for the target & constraints

targets/SCROD.revB/images <- .bit and .mcs are copied here after build w/ ver. #

targets/ZC706

targets/…

<repo>/trunk/firmware/build <- usually a softlink to some scratch space. Logs & raw outputs found here.

<repo>/trunk/firmware/build/zc706 <- one subdirectory per target

<repo>/trunk/software

Status & Example Project

- Beginning to restructure directories on Hawaii SVN now.
- (Still) working on an example ethernet DAQ project for the ZC706 board that can be used to test out the system.
  - Will commit as soon as it's ready and notify by email.
  - Need this in place along with some simple ASIC testing blocks by the time IRSX FMC cards return (~1-2 weeks?).