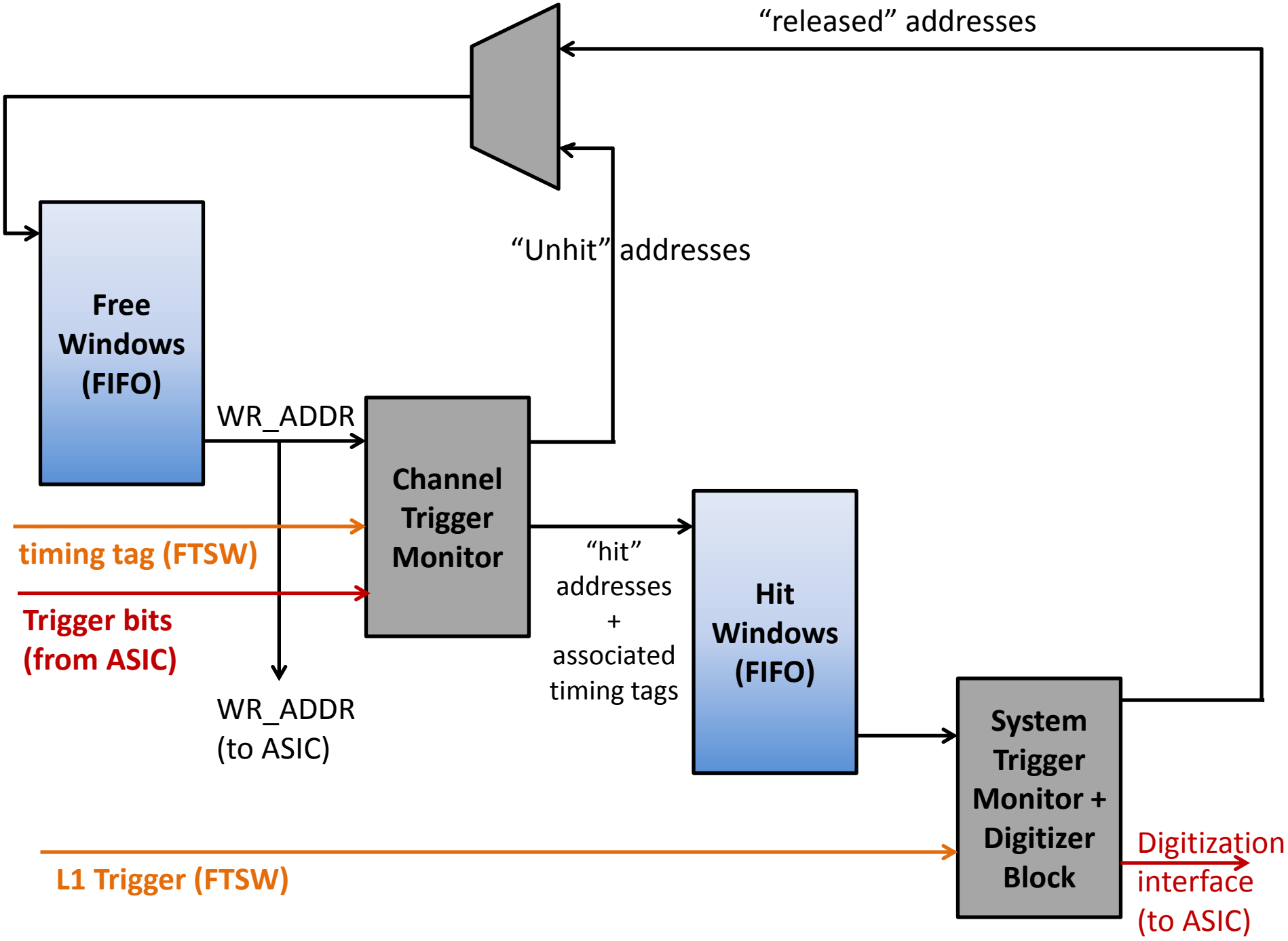
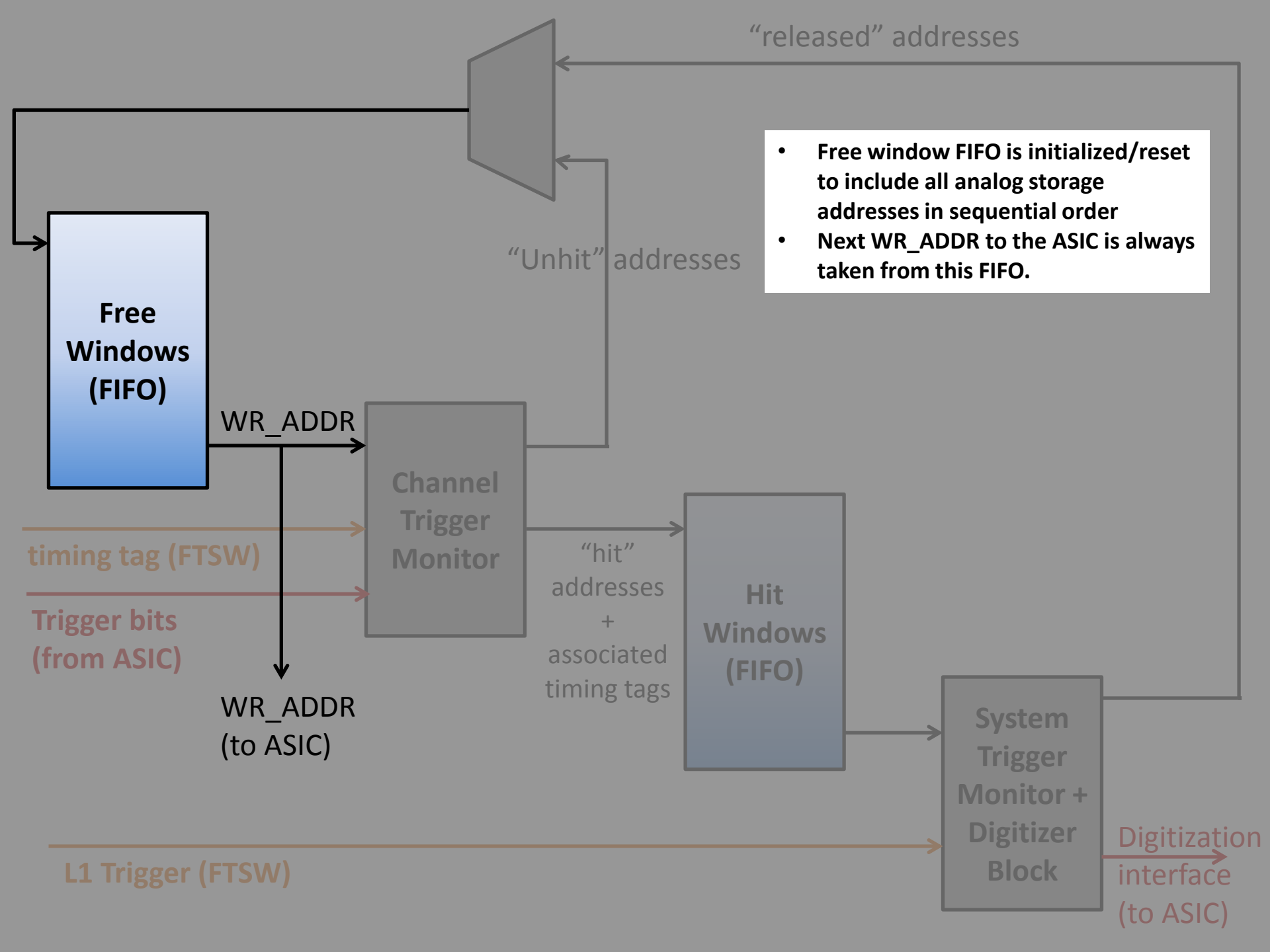

"released" addresses
"Unhit" addresses
Free Windows (FIFO)
WR_ADDR
Channel Trigger Monitor
timing tag (FTSW)
Trigger bits (from ASIC)
WR_ADDR (to ASIC)
"hit" addresses + associated timing tags
Hit Windows (FIFO)
System Trigger Monitor + Digitizer Block
L1 Trigger (FTSW)
Digitization interface (to ASIC)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System Trigger Monitor + Digitizer Block
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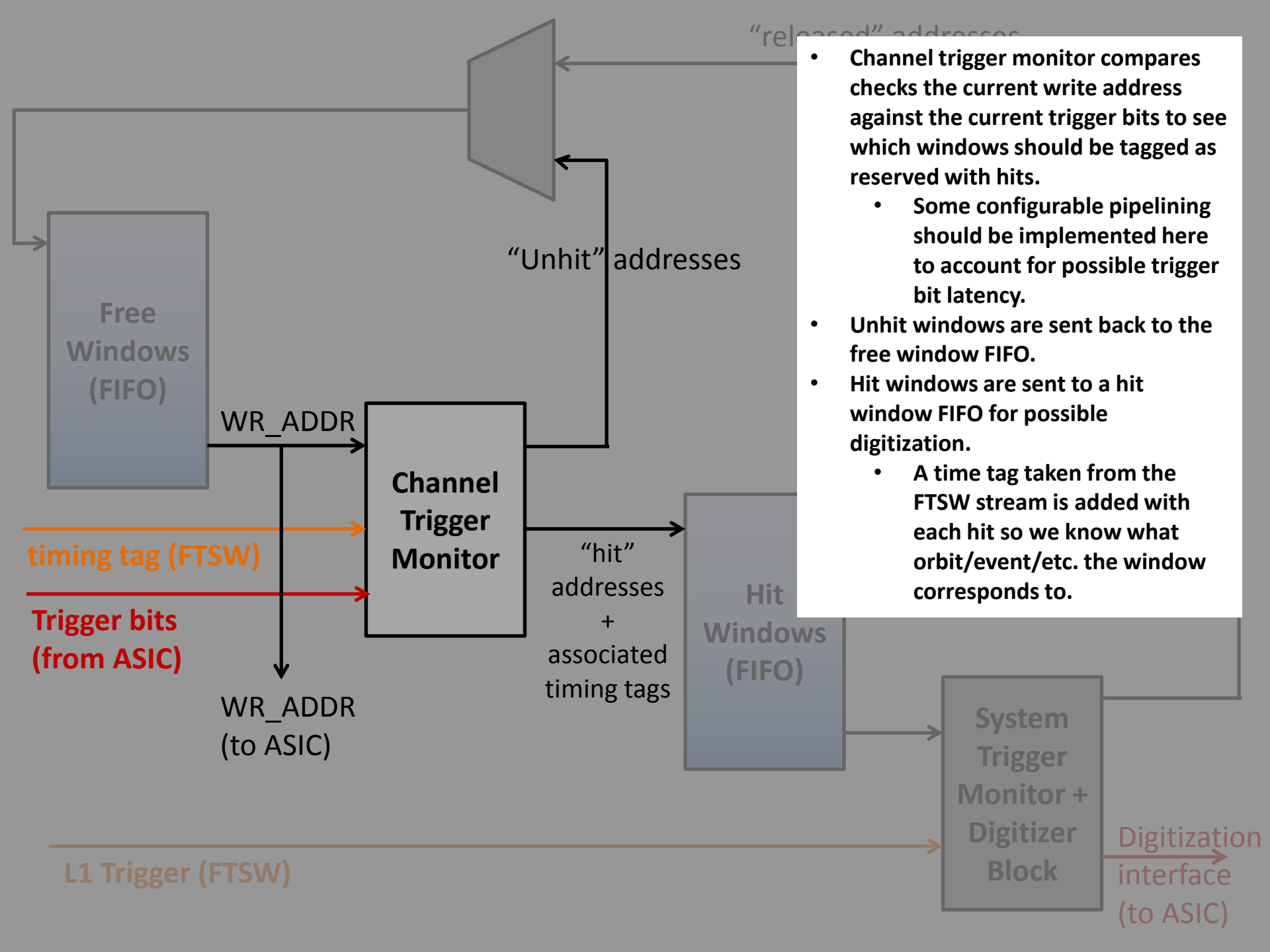
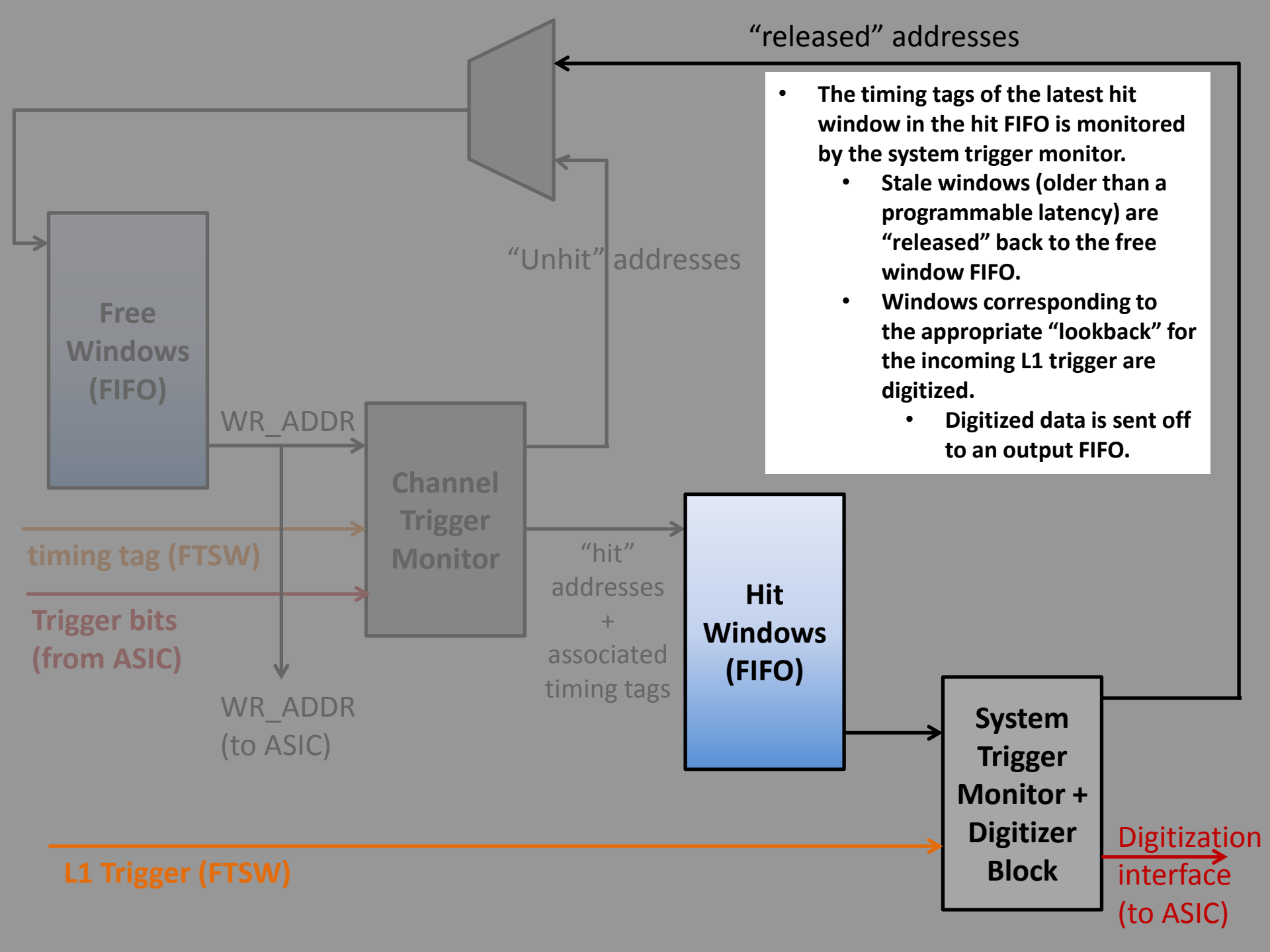
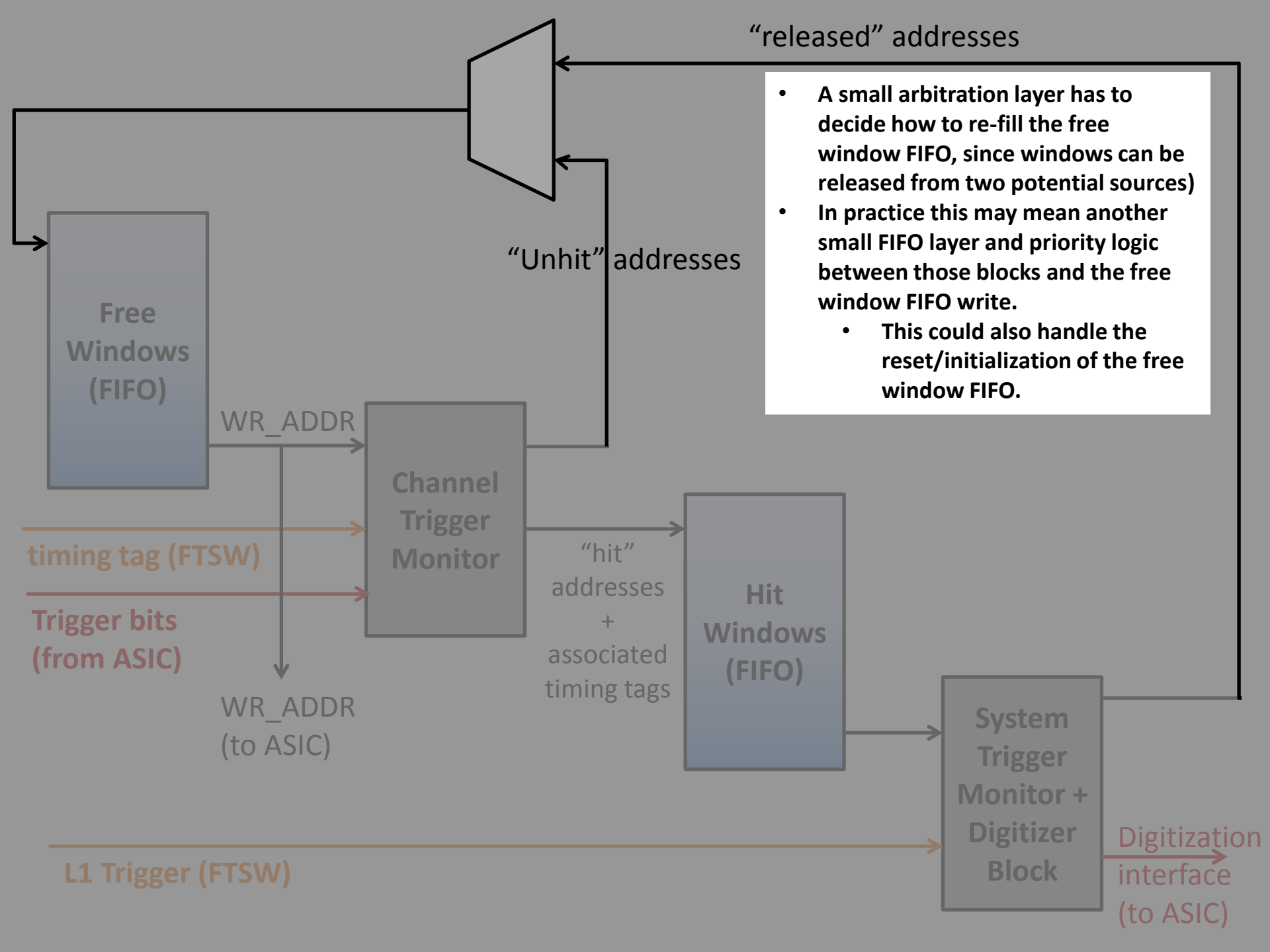
Digitization interface (to ASIC)
• Free window FIFO is initialized/reset to include all analog storage addresses in sequential order
• Next WR_ADDR to the ASIC is always taken from this FIFO.



- **Channel trigger monitor compares checks the current write address against the current trigger bits to see which windows should be tagged as reserved with hits.**
  - **Some configurable pipelining should be implemented here to account for possible trigger bit latency.**
- **Unhit windows are sent back to the free window FIFO.**
- **Hit windows are sent to a hit window FIFO for possible digitization.**
  - **A time tag taken from the FTSW stream is added with each hit so we know what orbit/event/etc. the window corresponds to.**



- **The timing tags of the latest hit window in the hit FIFO is monitored by the system trigger monitor.**
  - **Stale windows (older than a programmable latency) are “released” back to the free window FIFO.**
  - **Windows corresponding to the appropriate “lookback” for the incoming L1 trigger are digitized.**
    - **Digitized data is sent off to an output FIFO.**



- **A small arbitration layer has to decide how to re-fill the free window FIFO, since windows can be released from two potential sources)**
- **In practice this may mean another small FIFO layer and priority logic between those blocks and the free window FIFO write.**
  - **This could also handle the reset/initialization of the free window FIFO.**