Reported in TDR (Oct 2010)

Table 13.1: Estimated average occupancy and data size and required number of subcomponents such as the number of Belle2Link for data transfer and number of COPPER modules. In addition to the listed subdetectors, trigger information is also planned to be read out in a similar way.

	#ch	occ. [%]	#link	/link [B/s]	#COPPER	ch size [B]	ev size [B]	total [B/s]	/COPPER [B/s]
PXD	8M	1	40	182M	—	4	320k	7.2G	—
SVD	243456	1.9	80	6.9M	80	4	18.5k	555M	6.9M
CDC	15104	10	300	0.6M	75	4	6k	175M	2.3M
BPID	8192	2.5	128	7.5M	8	16	4k	120M	15M
EPID	77760	1.3	138	0.87M	35	0.5	4k	120M	15M
ECL	8736	33	52	7.7M	13	4	12k	360M	30M
BKLM	21696	1	86	9.7M	6	8	2K	60M	10M
EKLM	16800	2	66	19.5M	5	4	1.4k	42M	8.4M

- Table has always been confusing:
  - 4k/event x 30kHz event rate = **120 MB/sec**
  - 8192 chan x 2.5% occup = **~205 channels hit/event**
  - **4k total event size** = 16(+4?) bytes/channel x 205 channels
- 128 links / 8 COPPERs = 16 links / COPPER?
  - Should be 64 links (4 x 16) = **8 links/COPPER**
  - If using stock HSLB: **require 16 COPPERs?**

Estimated by Kurtis (Jan 2014)

- 30kHz x 4 windows x 1% occ. x ~2 trigger
  x 128 channels = **308k conversions/sec per boardstack**
- 308k conversions/sec x 64 samples/conversion x 16 bits = **40MB/sec**

- TDR-like rate calculation: 308k/4 hits/sec x 64 boardstacks = 4.9M hits/sec
  x 20 bytes =
  98 MB/sec

- Compare to TDR at:
  120 MB/sec

- **Maybe we don't have much DAQ headroom?**

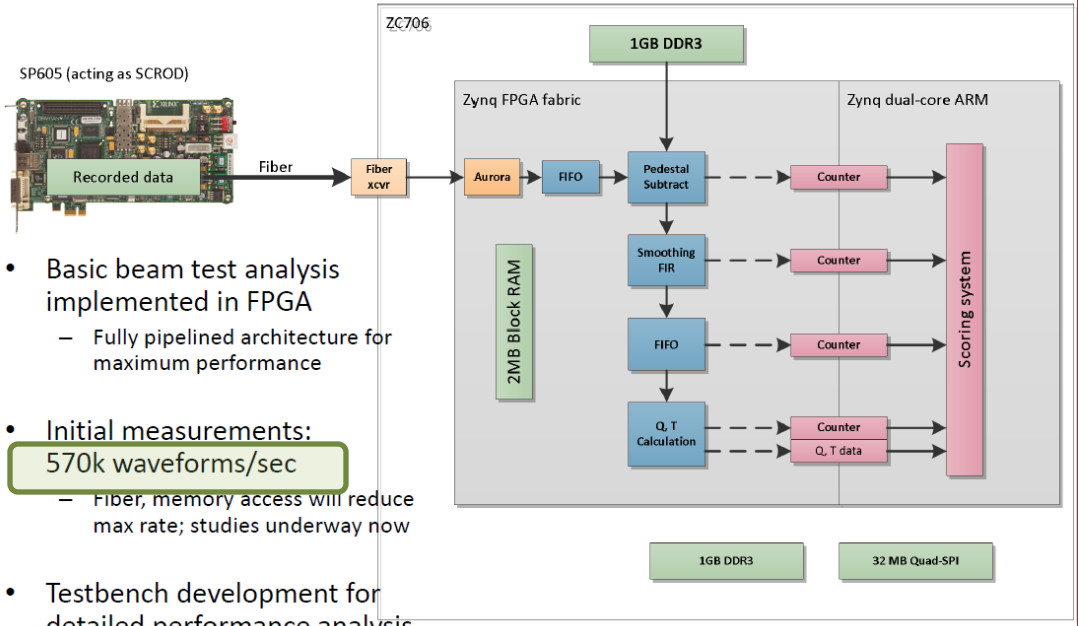
Data Rates

- 30 kHz sustained L1 trigger rate:
  - Numbers generally trying be conservative.
    - Assume 256 samples (4 windows) per digitization
    - 1% occupancy per L1 trigger.
    - 16 bits per data word sent down link.
    - ~~x2 IRSX trigger ambiguity (in principle we can decode based on length, though)~~
    - ➔ Per carrier (32 channels):
      - 76.8k conversions / s
      - 78 Mb / s.
    - ➔Per board stack (128 channels):
      - 308k conversions / s
      - 314 Mb / s.
  - Obviously data volumes go down significantly if feature extraction is performed on carriers or on SCROD.
  - Existing board stacks would not meet the 308k conversions per second rates due to the way ASIC address lines are bused. This can be solved either by going to IRSX (point-to-point digitization address selection) or multi-FPGA architecture (different carriers could have different read address buses).

Measured by PNNL (Dec 2013)

- FPGA in ideal situation (no deadtime):
  570k waveforms/sec x 4 windows/waveform = 2.03M conversions/sec
- ~7x above Kurtis' estimate, but potential slowdowns still possible
  - Waveforms w. multiple events
  - Data fetch from DDRAM
- In the ARM (also an ideal situation):
  - Current rate ~20k waveforms/sec (80k conversions/sec)
  - Definite room for optimization (was 8k earlier this week…)

Data Analysis in Hardware



- Basic beam test analysis implemented in FPGA
  - Fully pipelined architecture for maximum performance
- Initial measurements:
  570k waveforms/sec
  - Fiber, memory access will reduce max rate; studies underway now
- Testbench development for detailed performance analysis with replayed data underway

Pedestal Storage

- Kurtis did this calc already – nowhere near enough BRAM
  (I had the total number of storage cells waaay off in my head)

Feature Extraction & Memory

- Memory requirements dominated by pedestals:
  - Per carrier:
    - ~1 Mpedestals = 32,768 cells x 32 channels
      - 16.8 Mb at 16 bits per pedestal.
      - 12.6 Mb at 12 bits per pedestal.
      - 8.4 Mb at 8 bits per pedestal.
    - XC7Z030 has ~8 Mb of block RAM.
  - Total:
    - ~4 Mpedestals = 32,768 cells x 128 channels
      - 67 Mb at 16 bits per pedestal.
      - 50 Mb at 12 bits per pedestal.
      - 34 Mb at 8 bits per pedestal.
    - XC7045 has ~17 Mb of block RAM.

➔ Both single- and multi-FPGA architectures will require substantial amount of external memory. How it is distributed is a point for discussion.

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