VHDL and Verilog Crash Course for FPGA firmware design

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1 Homework No. 3

The purpose of the third day's exercise is to design a small but useful module, write its constraints, and complete its implementation.

2 Design Specification

Design, test and implement a Time-to-Digital Converter (TDC) for fast measures of time intervals (1 ns), with a maximum count of 200ns. The module should receive an external differential clock at 200MHz, multiply it to 1GHz, and use the 1GHz clock to run a very fast counter that is started and stopped by 2 different inputs. When the start signal arrives, an internal counter starts. When the stop signal arrives, the content of the counter gets copied into a register clocked at 50MHz and output together with a flag indicating valid count. The flag gets cleared at the beginning of a new measure (start bit going up).

For the implementation use a Spartan6 device.

In order to generate the 1GHz clock, use the entity provided with the file myclock_gen.vhd, and connected in the way shown below.

```
clkgen_u : myclock_gen
  port map
   (-- Clock in ports
    CLK_IN1_P => clk_p,
    CLK_IN1_N => clk_n,
    CLKFB_IN => CLKFB,
    -- Clock out ports
    CLK_OUT1 => CLK1G,
    CLK_OUT2 => CLK50M,
    CLKFB_OUT => CLKFB);
```

Note: the tricky part of the design is finding a fast architecture for the adder - experiment various options - standard 32 bit adder, faster adders, cascaded counters, Johnson counters. Try to get as close as possible to satisfy the requirements.

3 Testing

Write a single testbench that will prove the correct behavior of the system.

4 Pin placement

Write a correct user constraint file with appropriate placement for the inputs and outputs. Pay particular attention to the start and stop inputs, to help reduce the insertion delays.

Complete the .ucf by adding appropriate time constraints: note that you might need to constraint not only the clock but also the input data - to minimize the effect of insertion delay. Alternatively, you might need to specify location for components.

6 Implementation

Run the implementation and correct anything in your design if error occur, and/or the design does not meet design specifications.