VHDL and Verilog Crash Course for FPGA firmware design

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1 Homework No. 2

The purpose of the second day's exercise is to try a slightly more practical design (either in Verilog or VHDL - better Verilog to gain experience in both)

2 Design Specification

Design a modules to allow communication with an SPI component. Given the data sheet of the SPI-based DAC from Microchip, design a module that allows to load a generic value on the output, following the protocol specifications on page 18.

3 Procedure

Design your module modelled on the examples seen in class - the protocol is quite simple, but make sure that the final design respects the timing diagram shown on page 19. Encode the input in whatever way you prefer, trying to make sure that the module is easily usable in a larger design. Assume you are given a 20MHz clock, and follow the specifications of the datasheet to make sure the speed is adequate (not too fast) for the device.

4 Testing

Write a single testbench that will exercise a few possible inputs.