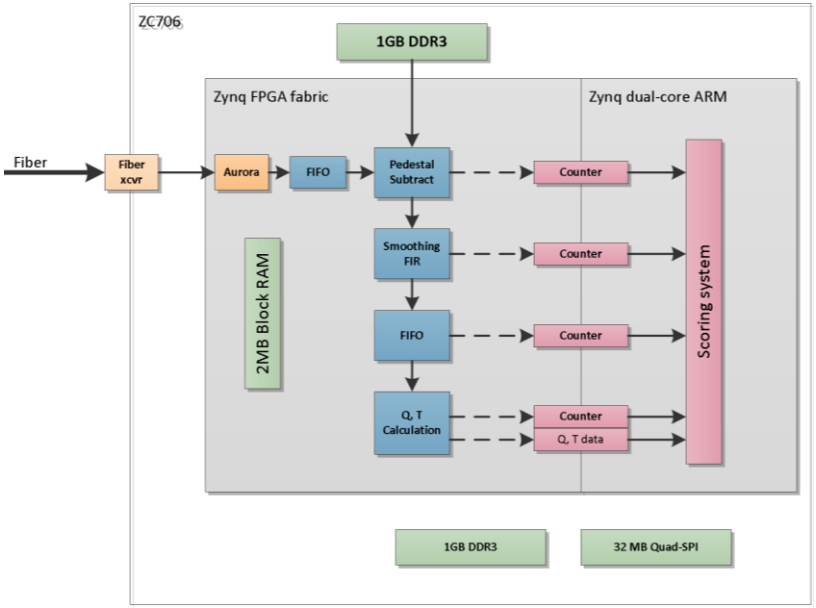
Feature Extraction Status

- In 2013, key components of SPring-8 feature extraction implemented in both ARM C and Zynq firmware for the Z'045:
  - Pedestal subtraction
  - Smoothing filter
  - CFD



- Code (both C and Verilog) now in repository*
  - I (Lynn) have been very remiss in this (and can no longer complain about others not submitting code!)

** at some point today; see slide at end*

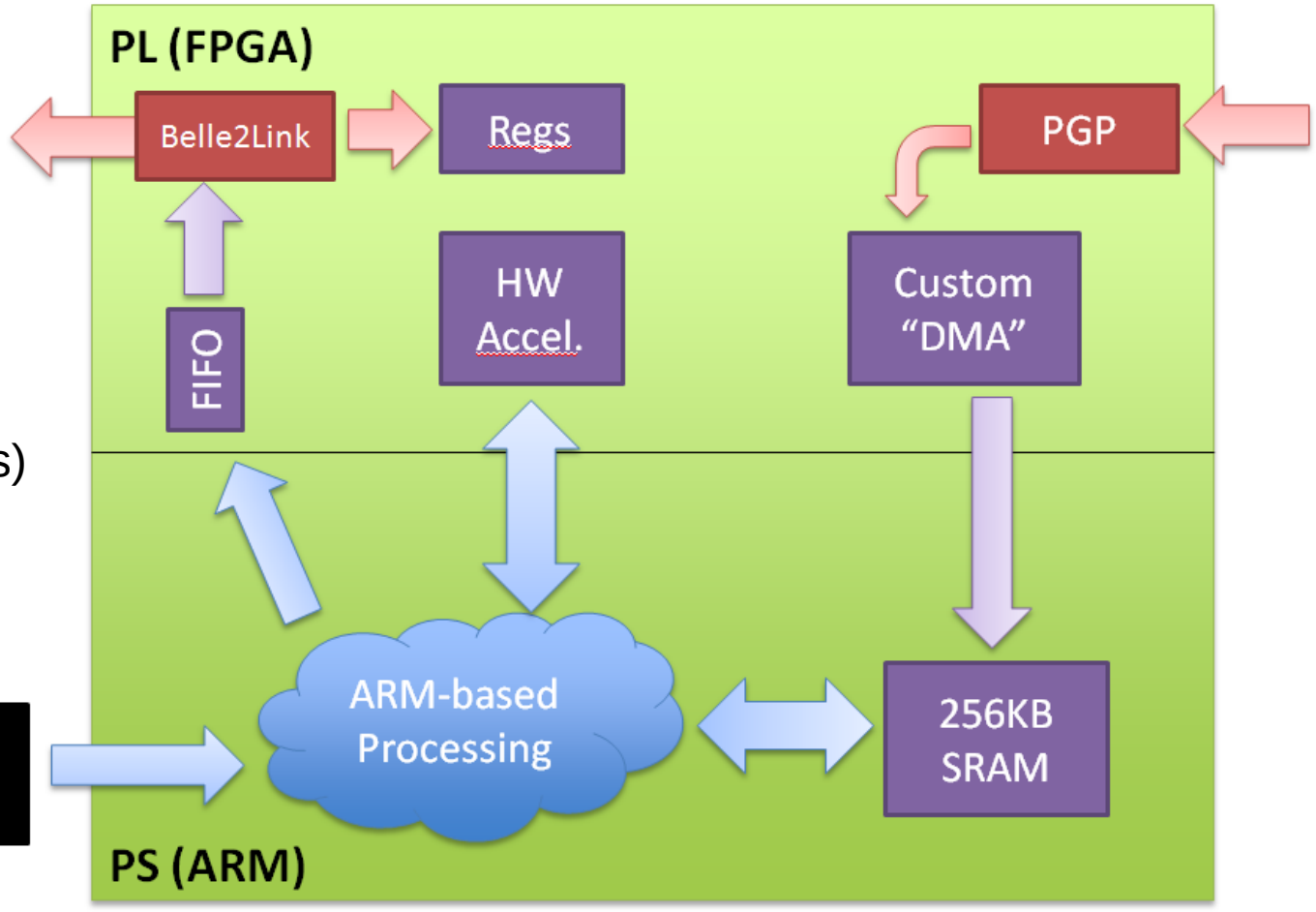
Feature Extraction Status

- **Pedestal subtraction**
  - Streaming in FPGA
  - Currently stored in BRAM → move to “realistic” storage (DDR)
- **Smoothing filter**
  - Streaming in FPGA → needs proper normalization, but also hopefully not needed in the end…
- **CFD**
  - Fast (but not streaming) in FPGA
  - Only nearest bin pickoff → needs sub-bin timing (doable)
- **Overall**
  - Needs multiple peak handling
  - Needs to have PS/PL integration
  - Needs VALIDATION! → run lots of data w. lots of variations

  - WHAT ELSE NEEDS TO BE INCLUDED?

Proposed Zynq Feature Extraction (draft)

- PL reads PGP
- PL pushes data to PS SRAM
  - Ring buffers and status
- ARM processes data (possible HW accelerators)
- Processed data put in B2L FIFO



Things to Start Thinking About

- Details of register interface between ARM and FPGA?
- Can we store pedestals in BRAM? (should we?)
  - When do we need to worry about BRAM integrity vs. DDR?
- Baseline design: all processing in SCROD, on ARM cores
  - Should we do anything (pedestal subtraction?) on carriers?
- Design document available “soon”

Repo Organization

- Feature extraction “ready to be submitted”, but…
- Current feature extraction is not final
  - Will not be used as basis for new effort
  - But parts of code will be borrowed
- In a typical repo, this would be a “branch” – a work in progress, not part of the official release (merged back in later)
  - **Where** do we want to store such things?
    - trunk/common/src/branches/…
    - trunk/targets/SCROD.revB/src/branches/…
    - trunk/branches/…
    - Other suggestions???