WBS 1.3 Electronics Common readout/global

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Belle II Physics Rates

Process	σ (nb)	Rate (Hz) @ L=8x10^{35}
Upsilon(4S)	1.2	960
Continuum	2.8	2200
μμ	0.8	640
ττ	0.8	640
Bhabha *	44	350
γ-γ *	2.4	19
Two photon **	80	15000
Total	67	~20000

* Rate of Bhabha and γ-γ are pre-scaled by factor 100

** Rates are estimated by the luminosity component in Belle L1 trigger rate

- **Physics triggers**
  - **Upsilon 4S + continuum**
    - **Three-track**
    - **Total energy**
    - **Isolated cluster**
  - **Tau pair**
    - **Two-track**
- **Calibration triggers**
  - **Bhabha**
    - **Pre-scaled by Bhabha trigger (ECL)**
  - **γ-γ**
    - **Pre-scaled by γ-γ trigger (ECL)**
  - **Mu pair**
    - **Two-track**
  - **Random trigger**
- **Veto**
  - **Beam injection**
  - **Two photon events if necessary**
    - **Low level reconstruction is necessary**

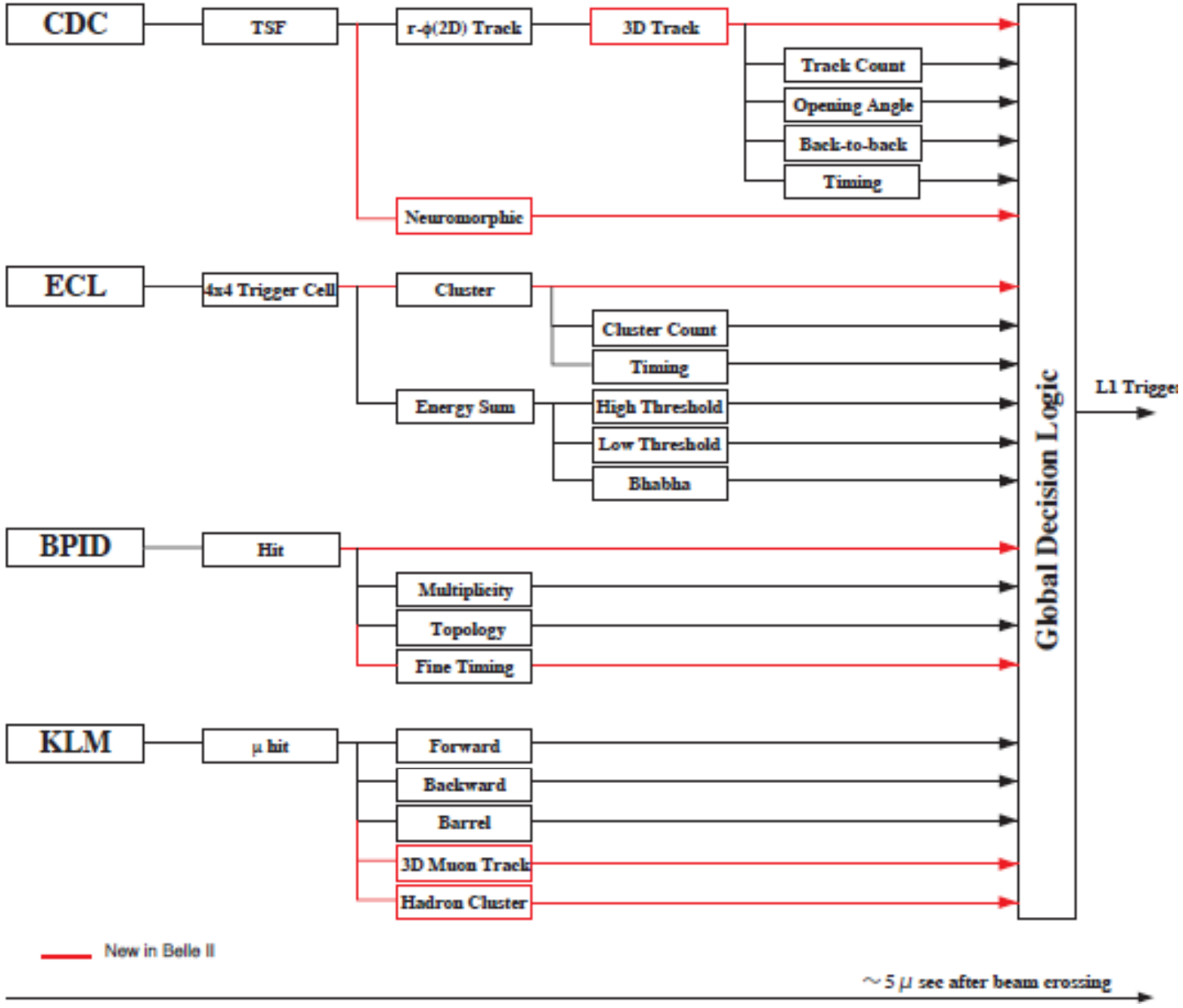
Belle-II Trigger System

Korea U.
National United U.
Fu Jen Catholic U.
Heidelberg U.
KEK

Hanyang U.
Seoul National U.

Hawaii U.
Univ. of Pittsburgh

Virginia Tech.
Hawaii. U.



Belle II Trigger Strategy

- **Requirements** (☑ = ok, ☒ = under study or unknown)
  - ☑ High efficiency — almost 100% for Upsilon 4S events
    - No deadtime -> pipeline
    - Redundant and independent TRG logics -> 3 main TRG
  - ☒ Max. average rate — 30 kHz @ 8×10^{35} $cm^{-2}s^{-1}$
    - Limit from DAQ
    - Good background reduction
      - Flexible TRG logics to manage BG rates
      - Low level event reconstruction to identify BG
  - ☑ Latency — ~5 usec
    - Limit from SVD front-end
  - ☑ Timing precision — less than 10 nsec
    - Request from SVD front-end
  - ☒ Event separation — 200 nsec
    - Request from DAQ
- **Belle triggering scheme is employed again**
  - Sub-Triggers + Global Decision Logic
  - Basic idea is same, but each components will be improved

    Data flow : parallel -> high-speed serial

    Data rate : 16 Mbps -> 190 Mbps (CDC wire case)

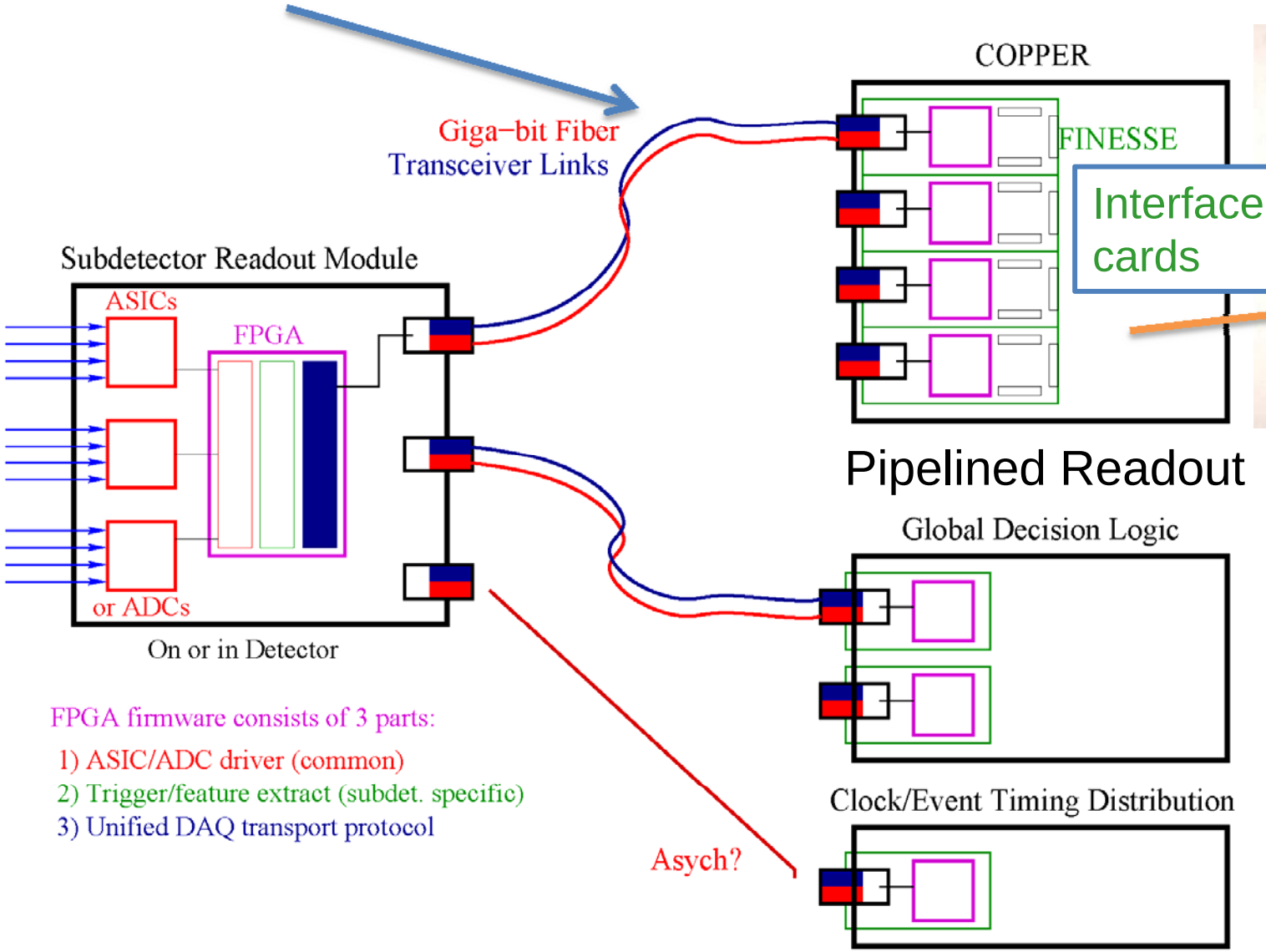
    Logic : hard-coded -> FPGA

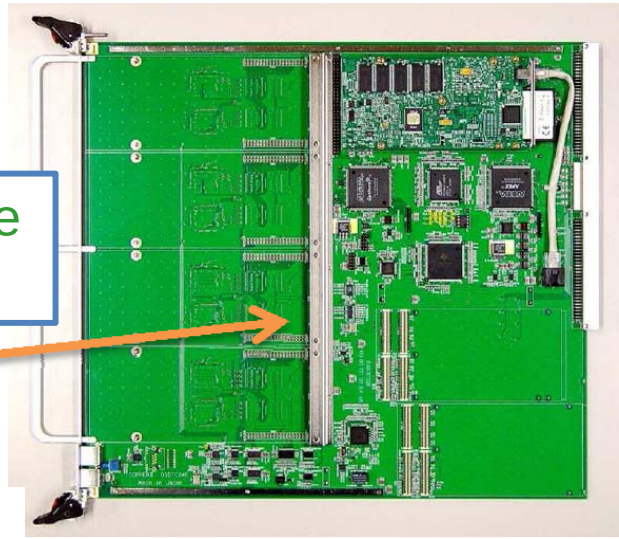
    #cables and modules : O(1000) -> O(100)

Unified Readout for Belle II

- At full luminosity, the data rate is 900 MB/sec.
- A high performance DAQ system is being designed by KEK and IHEP Beijing

Belle2link protocol

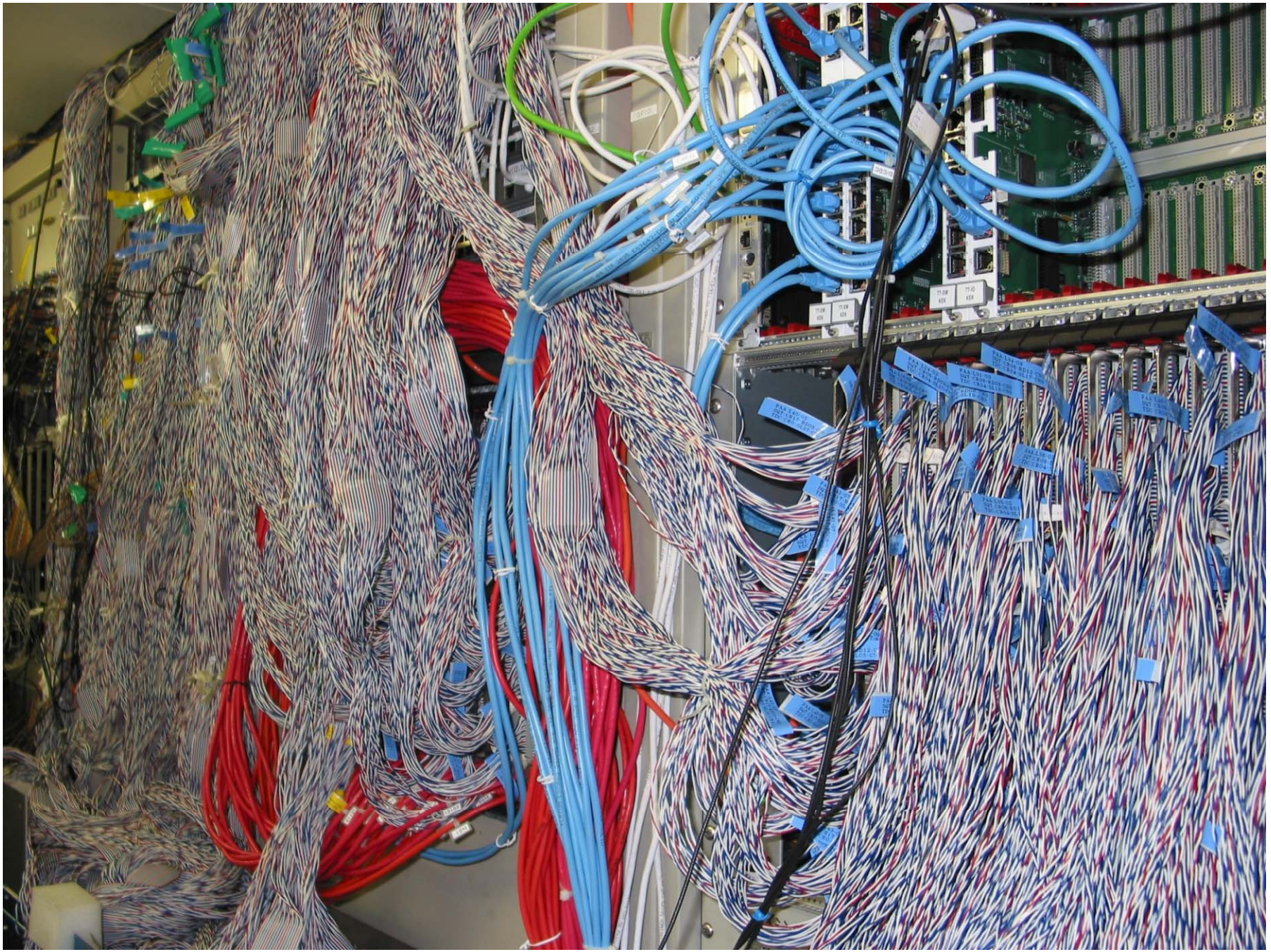




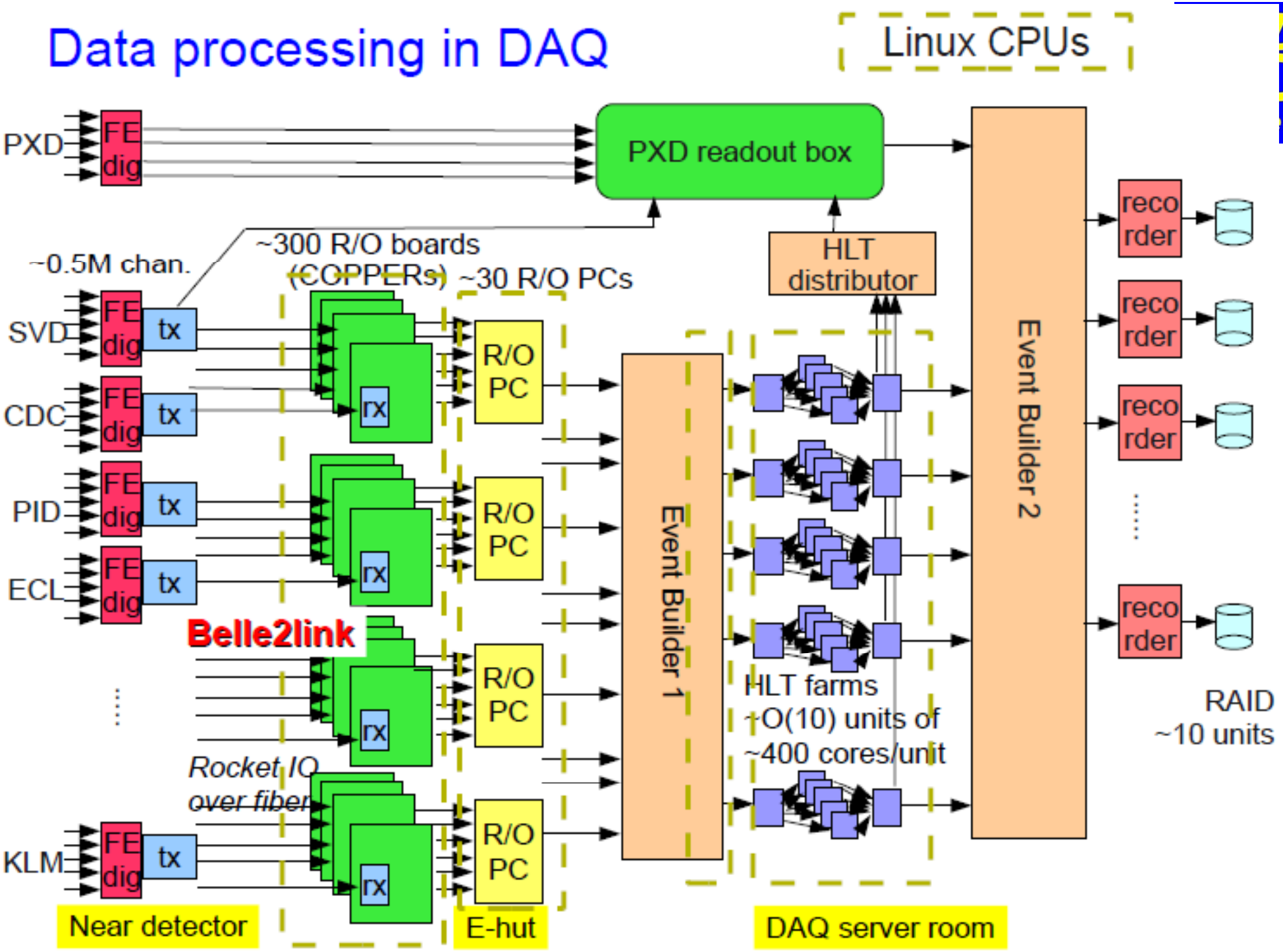
FPGA firmware consists of 3 parts:

1) ASIC/ADC driver (common)
2) Trigger/feature extract (subdet. specific)
3) Unified DAQ transport protocol

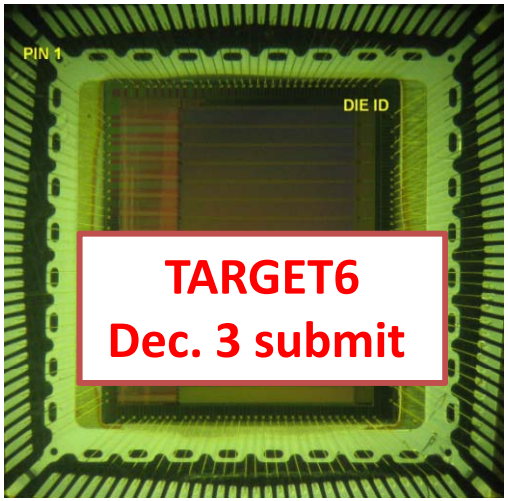
Belle II DAQ: Got fiber?



Data processing in DAQ



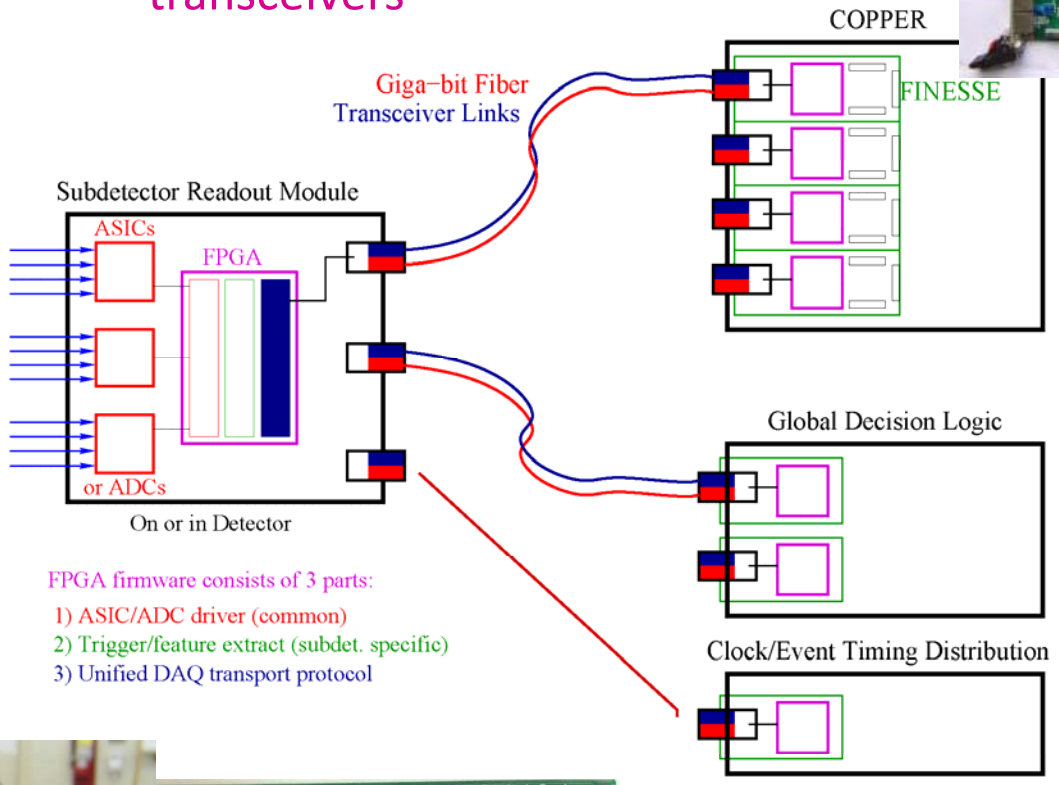
Scint. KLM Readout



20k channels
1.25k 16-channel Waveform sampling (TARGET) ASICs
112+32 SRM

112+32 DAQ fiber transceivers

36 HSLB FINESSE
9 COPPER

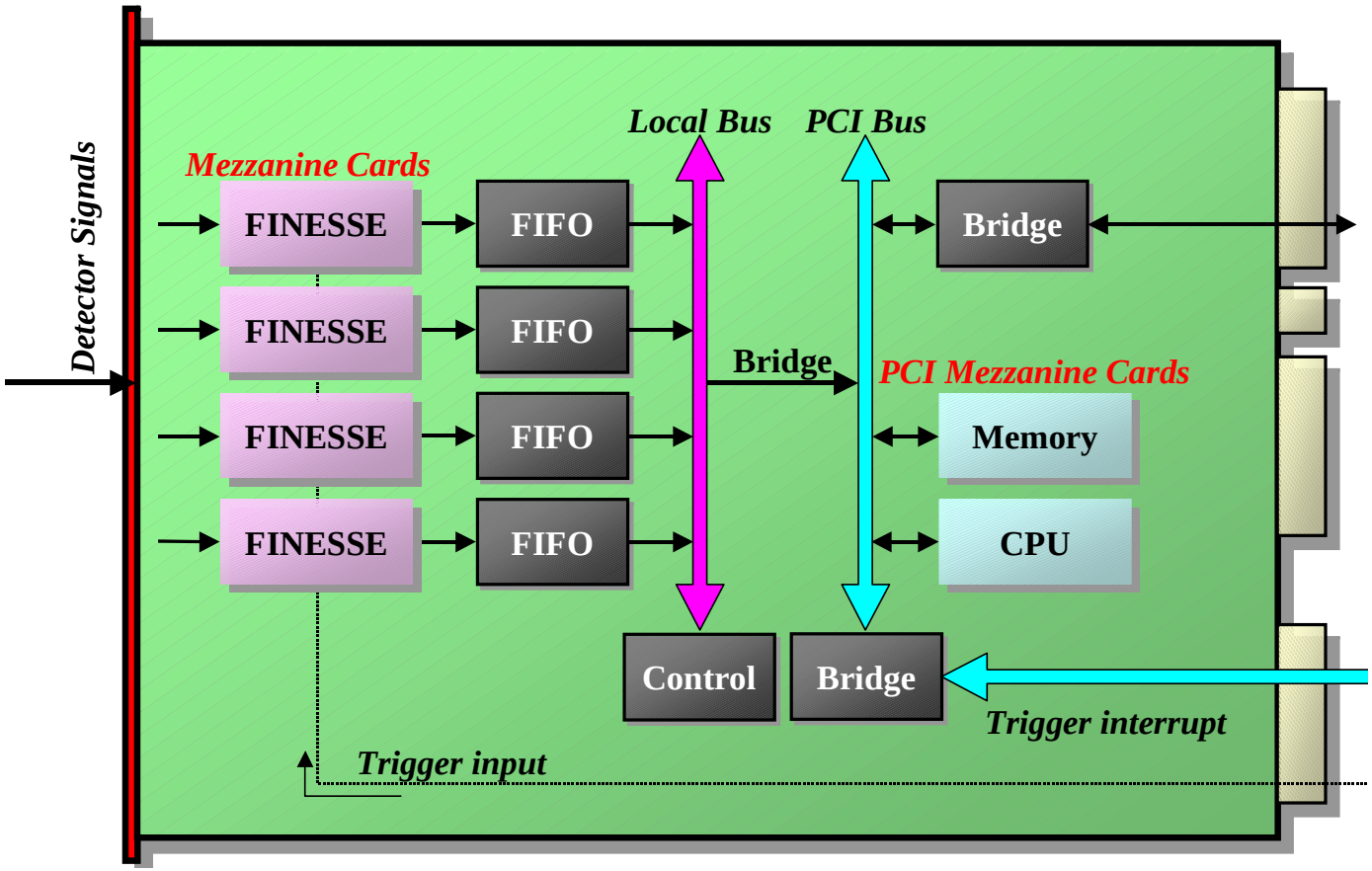


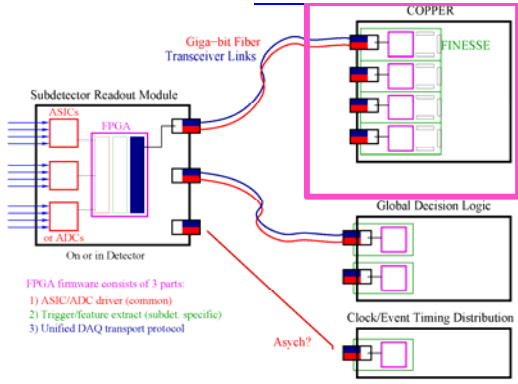
Trigger is common with RPC/barrel : Use a common merge board

FTSW for programming/ timing/trigger

Pre-amp Production Complete by end of JFY

Technical Status: back-end (1)





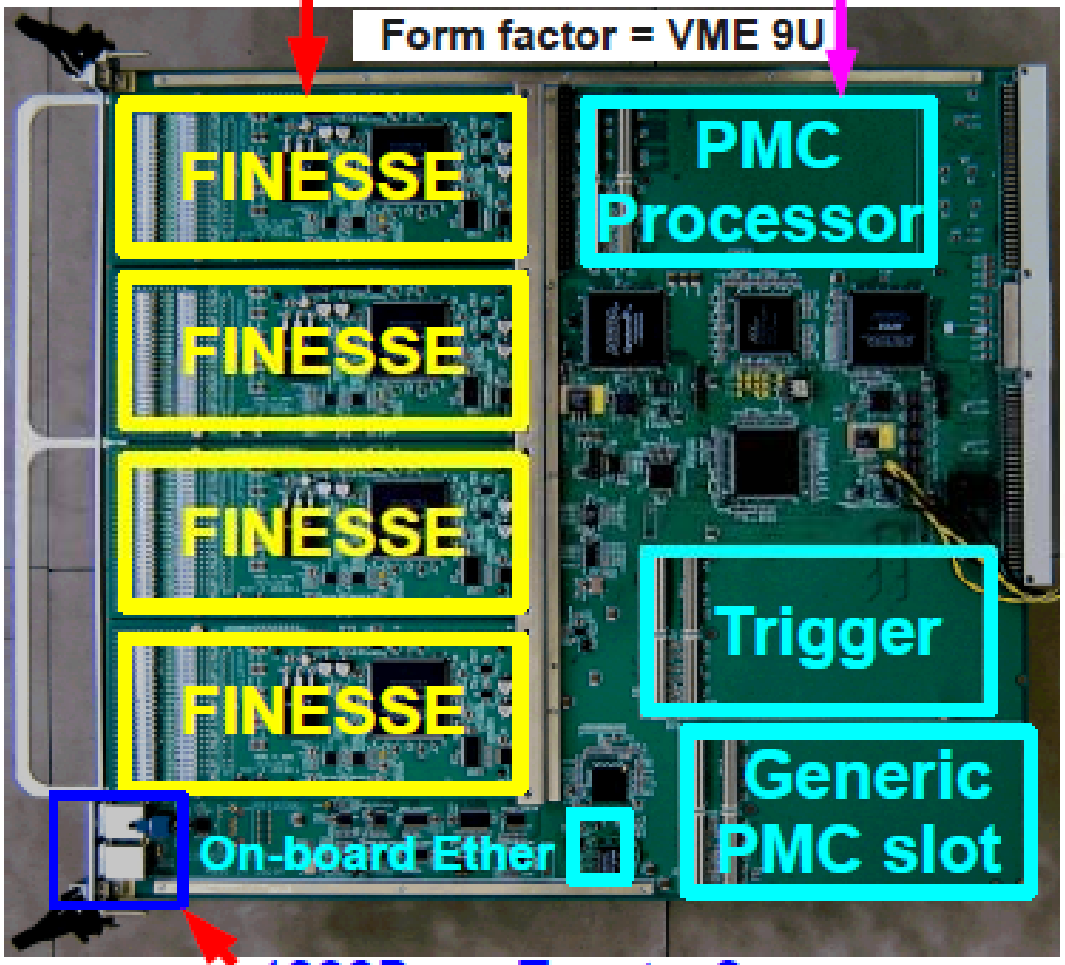
Upgraded for Belle II

- COPPER (COmmon Pipelined Platform for Electronics Readout)
- Used in Belle, J-PARC experiments
- FINESSE (Front-end Instrumentation Entity for Subdetector Specific Electronics)

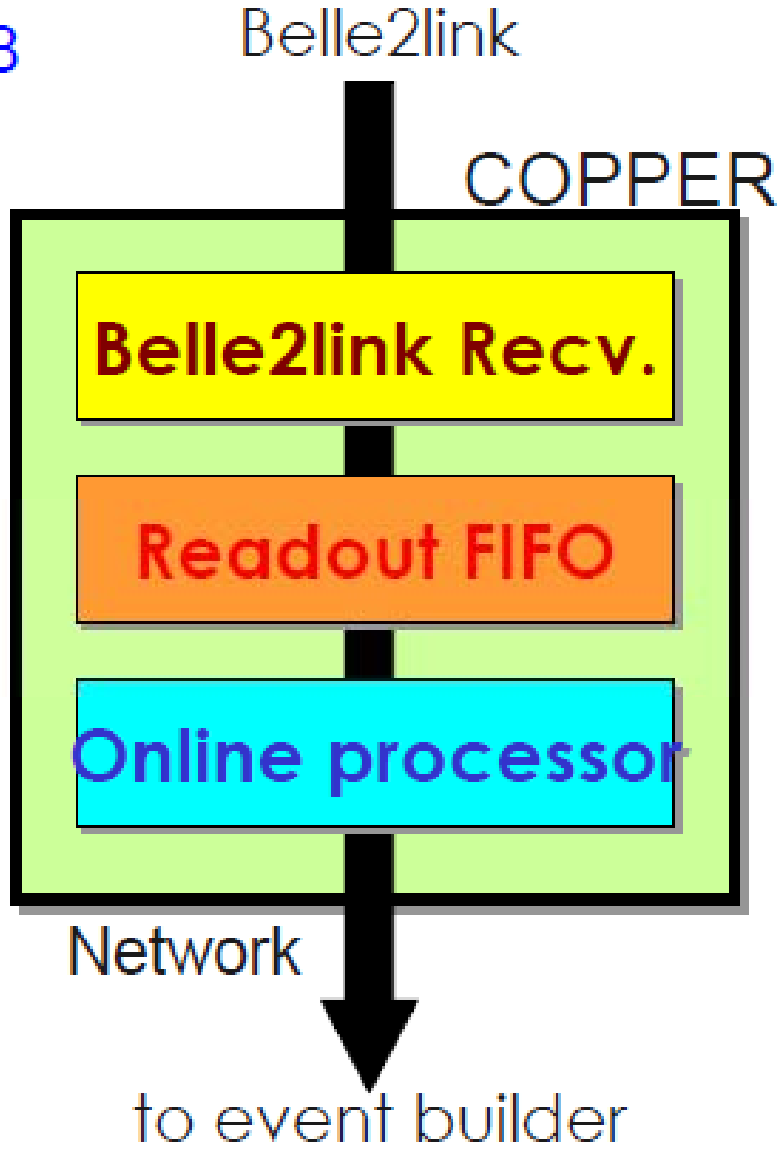
COPPER

Digitizer cards
(Belle2link recv.)

CPU (Linux)
ATOM 1.6GHz
Memory : 512MB

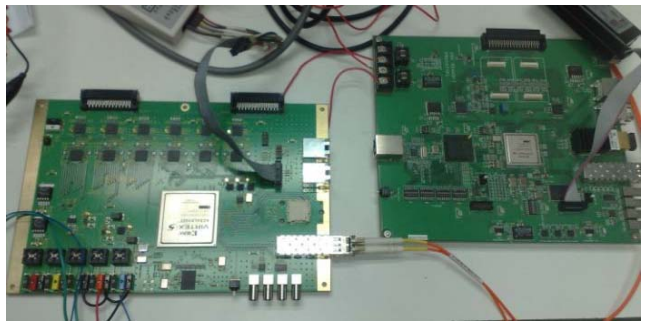


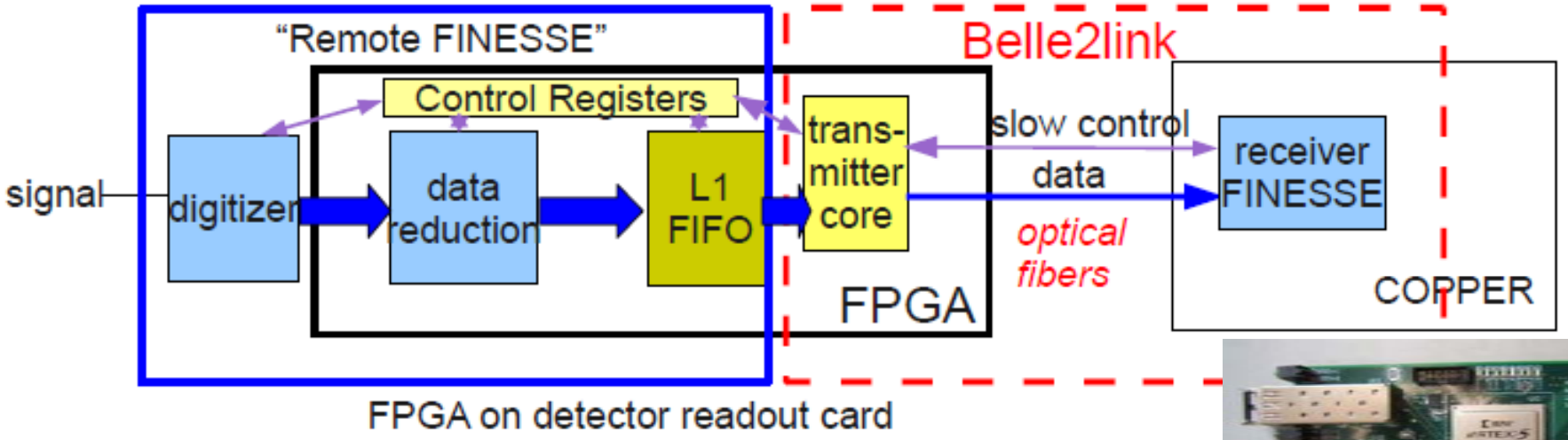
1000Base-T port x 2



Technical Status: back-end (2)

Belle2link



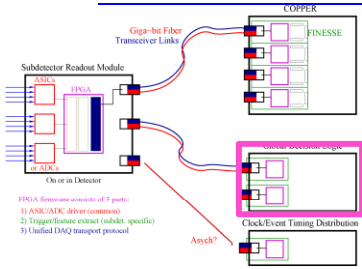


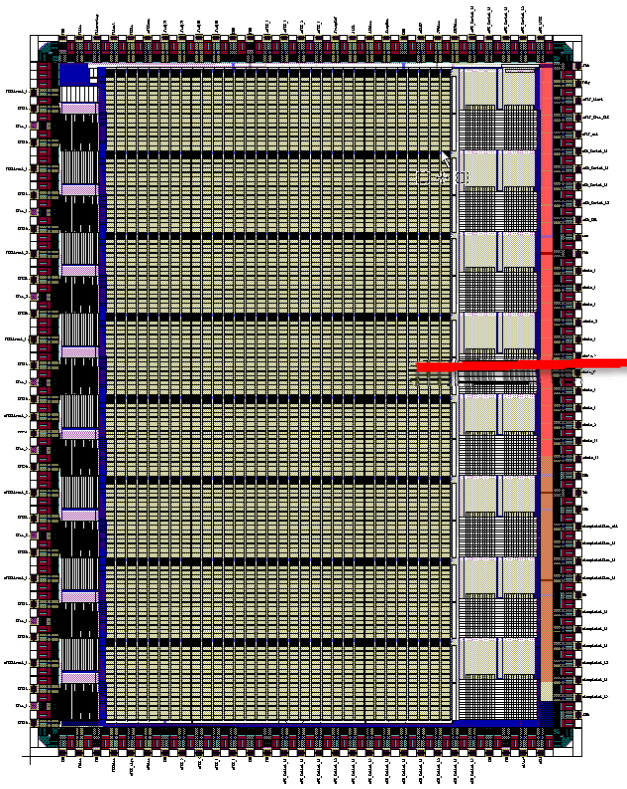
Functionality of Belle2link

1) Data transmission from detector FEE to COPPER
   <- Performance (3Gbps link) was already reported laast year.
2) Parameter downloading to FEE and various slow control from COPPER

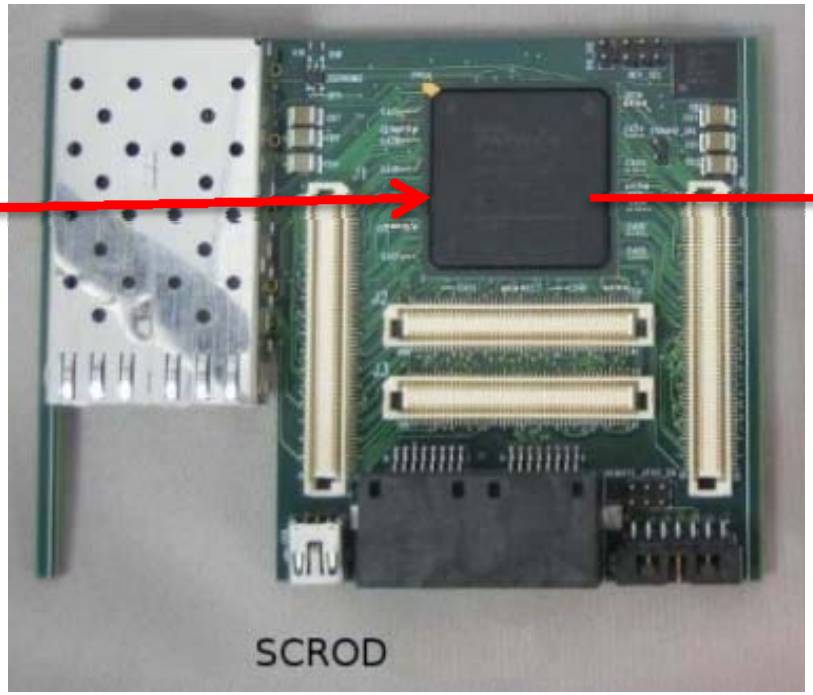
* Being developed by IHEP, Beijing

Technical Status: Trigger

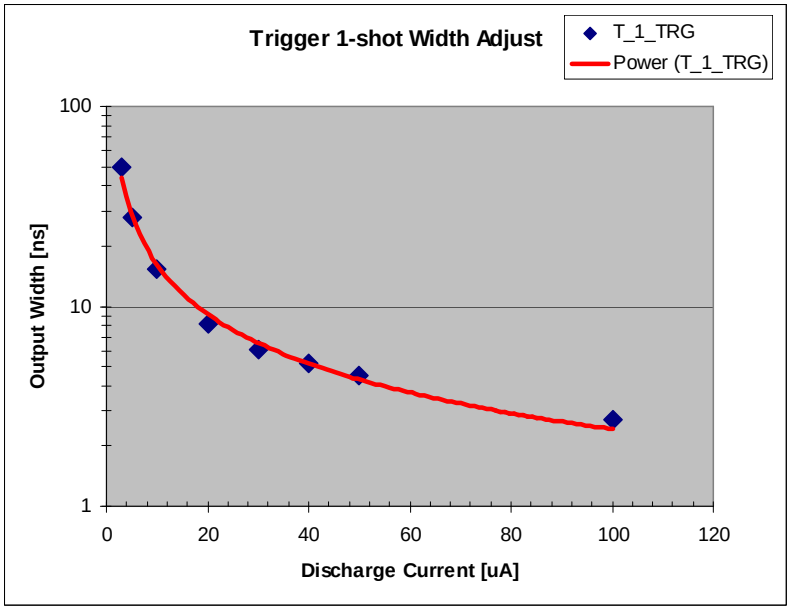




Trigger time-stamping same as iTOP



Fiber Link Merge



A wide variety of established FPGA-based TDCs with few ns resolution

Need anyway for readout hit-matching

Trigger/Timing Distribution (FTSW)

From Nakao-san's documentation:

20110805 version

Timing signals over CAT7 cables

7 ports, O1 to O7

ACK ← ACK: 254 Mbps serialized, unused
TRG ← TRG: 254 Mbps serialized
RSV ← RSV: pulled down to GND
CLK ← CLK: 127 Mhz

JTAG signals over CAT7 cables

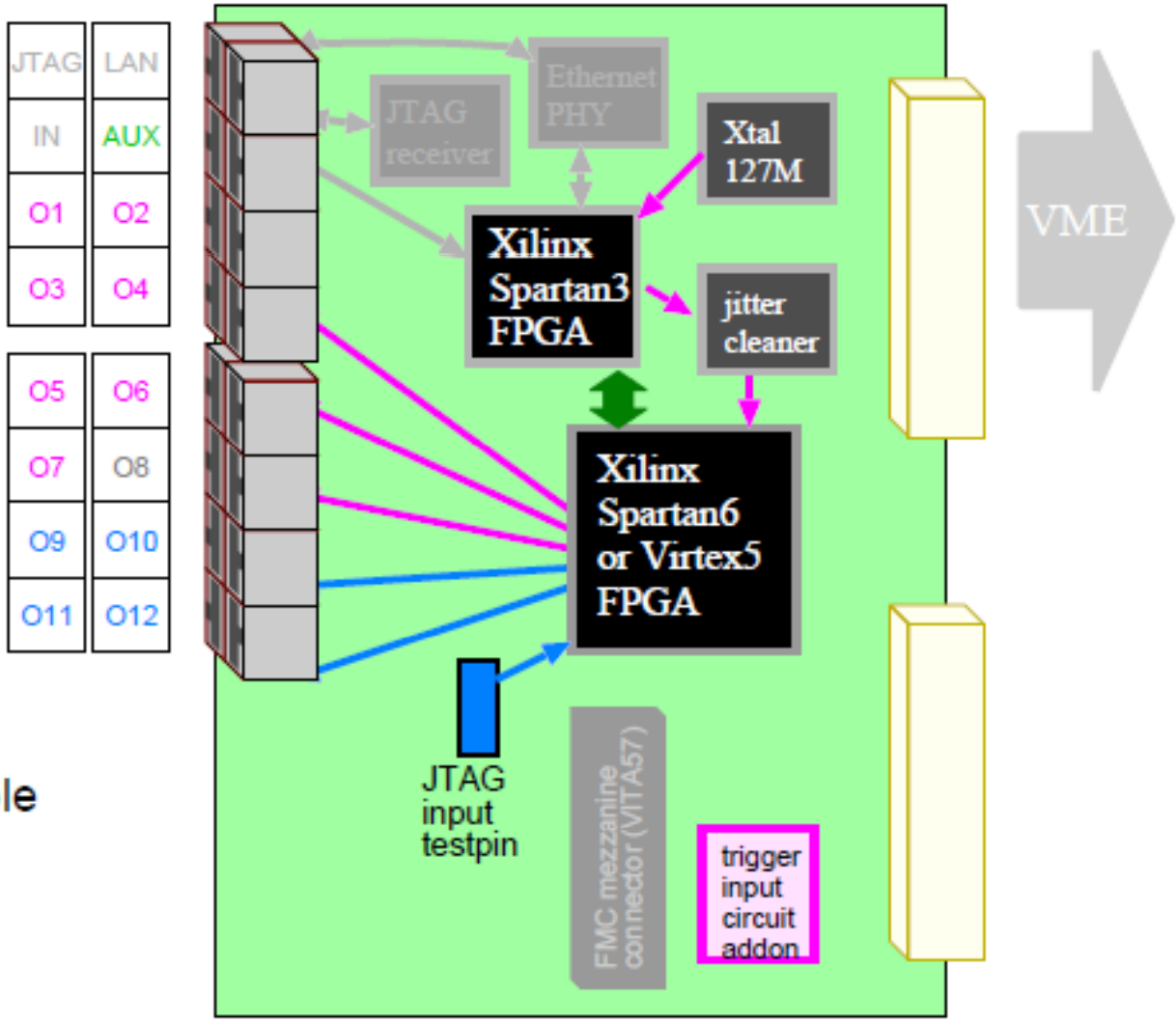
4 ports, O9 to O12

TCK ←
TMS ←
TDI ←
TDO →

Monitoring signals over a CAT7 cable

AUX port

trgin ← copy of trigger input
trg21 ← latched with 21MHz clock
trgpulse ← trgin and (not trg21)
clk21 ← 21MHz clock



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- CLK ← CLK: 127 Mhz

JTAG	LAN
IN	AUX
O1	O2
O3	O4
O5	O6
O7	O8
O9	O10
O11	O12

JTAG signals over CAT7 cables

4 ports, O9 to O12

- TCK ←
- TMS ←
- TDI ←
- TDO →

Monitoring signals over a CAT7 cable

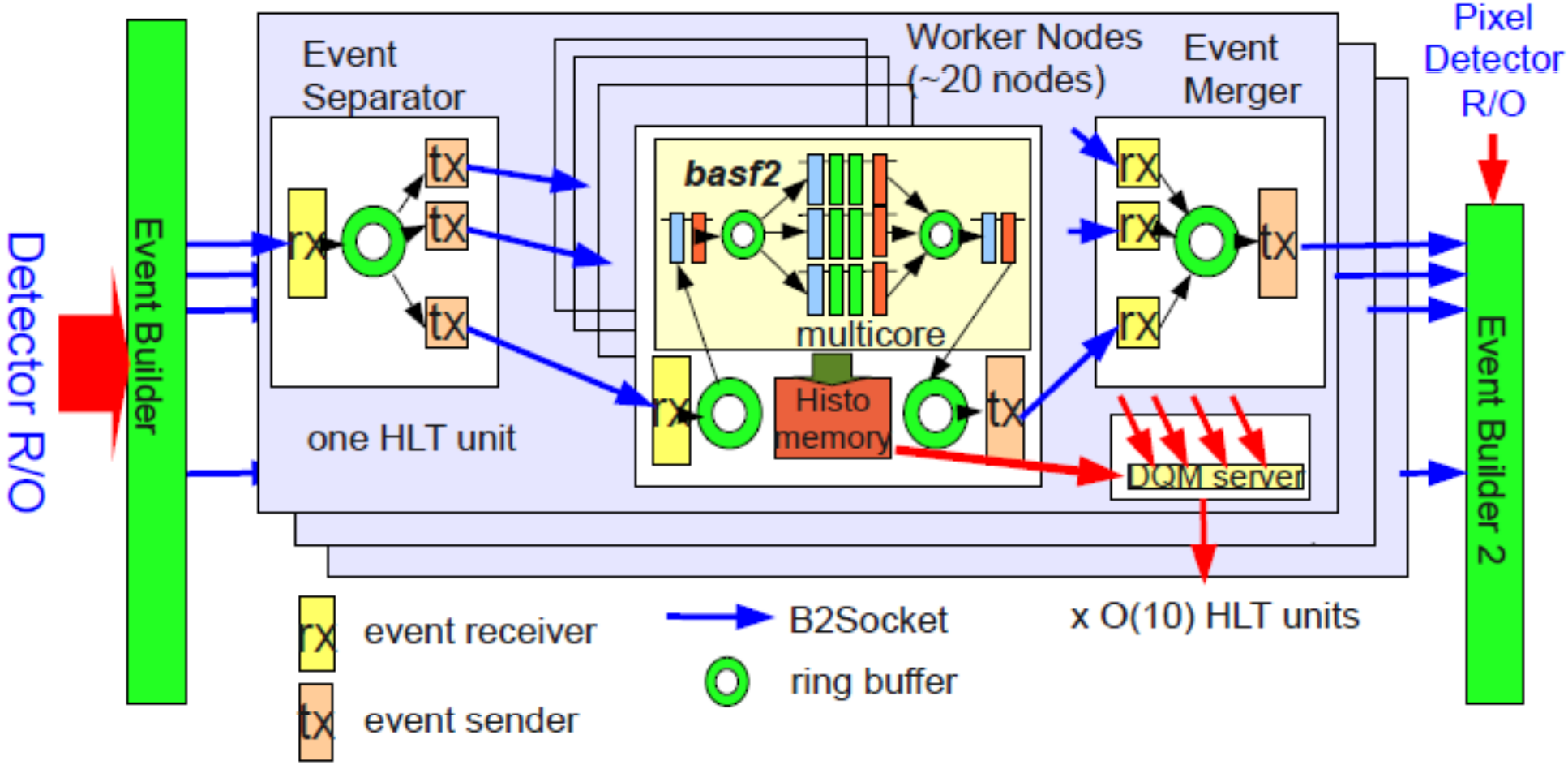
AUX port

- trgin ← copy of trigger input
- trg21 ← latched with 21MHz clock
- trgpulse ← trgin and (not trg21)
- clk21 ← 21MHz clock

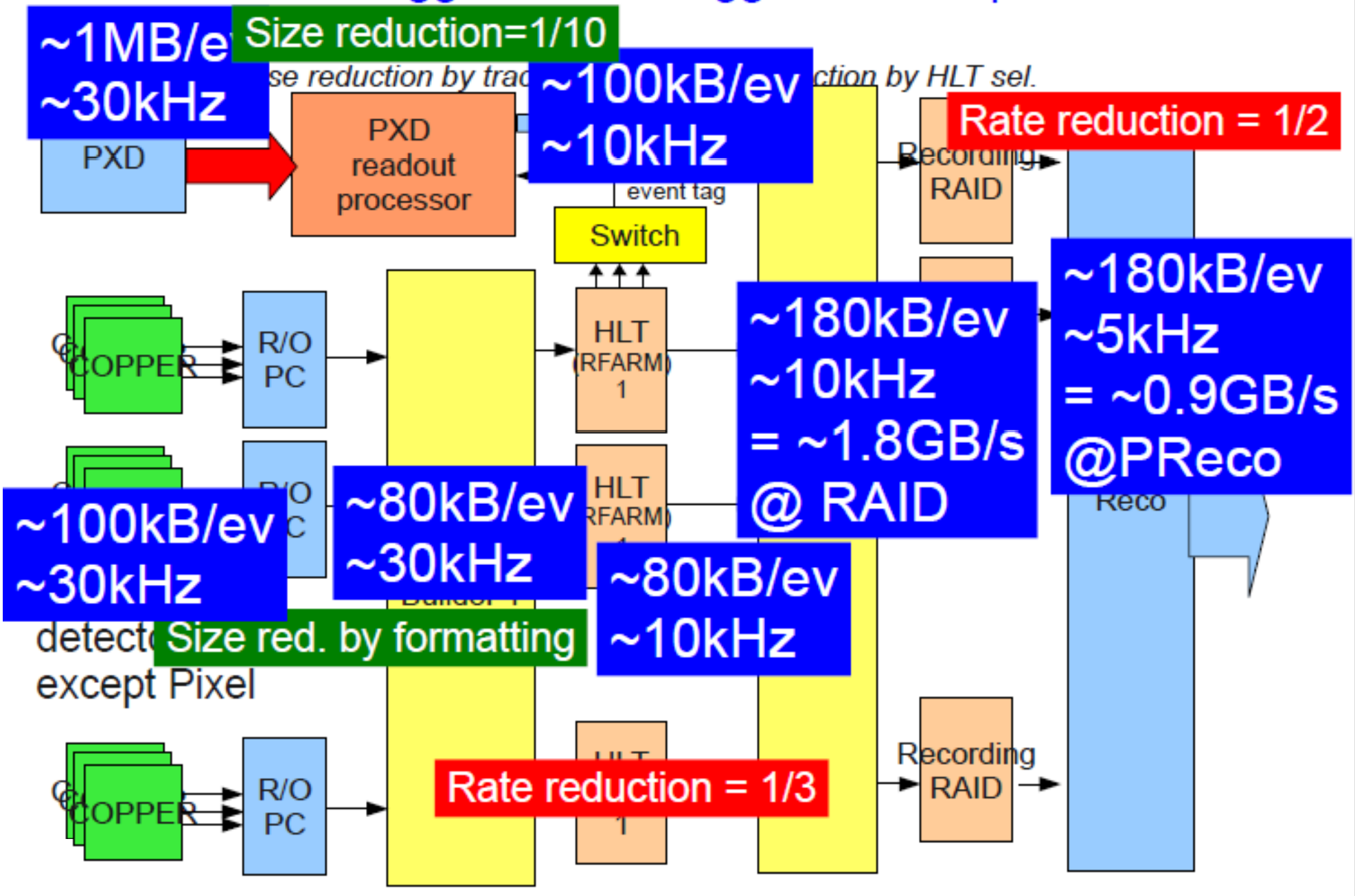
VME

High Level Trigger (HLT)

- Unit structure (O(10))
  - * to reduce the number of output port of event builder
  - * to keep up with the gradial luminosity increase
  - * fault-tolerant : each unit is completely independent
- Based on the parallel processing technology developed for basf2



Expected data rate/size reduction for L1 trigger rate=30kHz with loose HLT trigger + Final trigger at PromptReco



Belle II Throughput

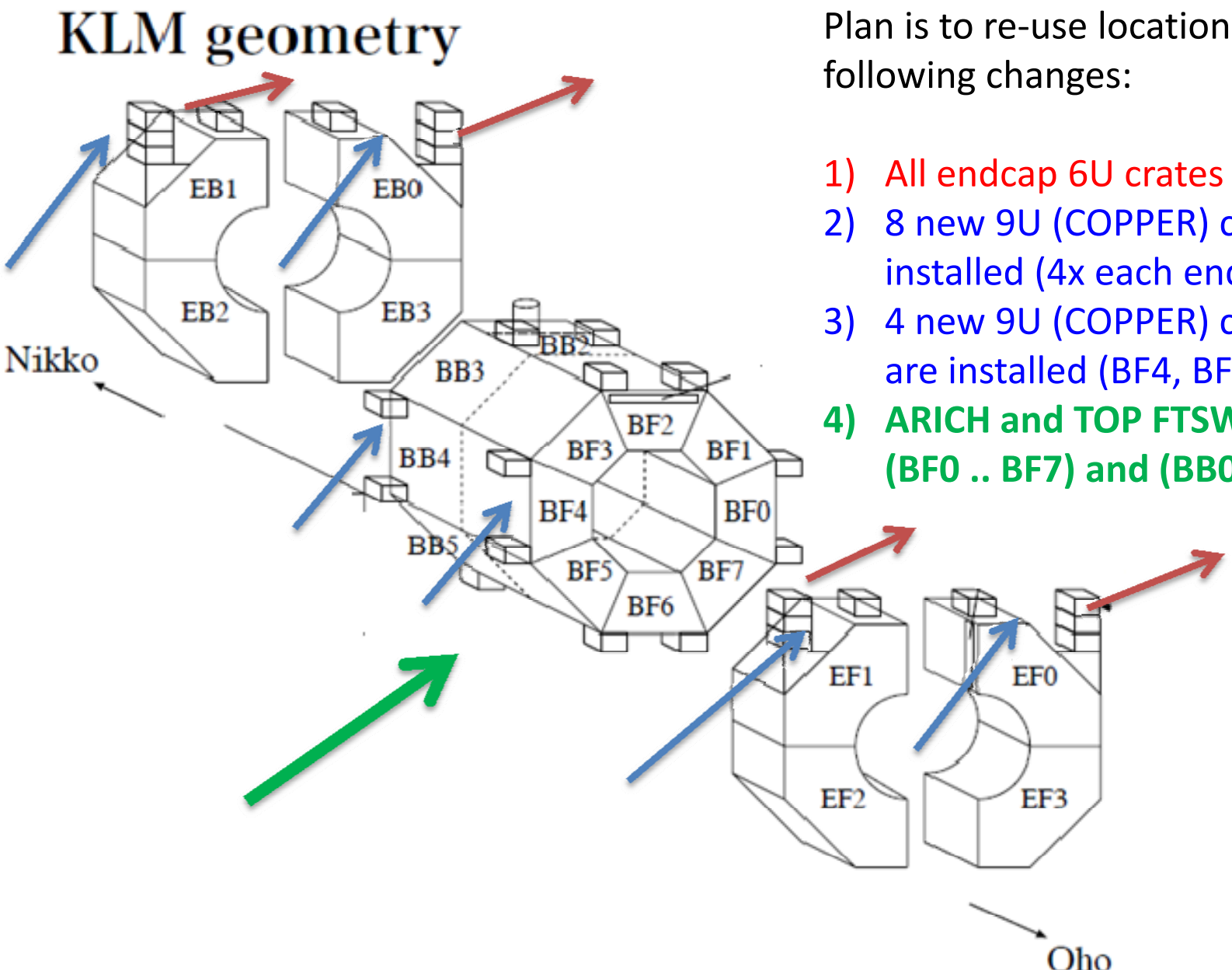
Estimated event size and bandwidth

Assumed L1 rate = 30kHz (maximum of average)

	#ch	occ [%]	#link	/link [B/s]	FNS	#CPR	ch sz [B]	ev sz [B]	total [B/s]	/CPR [B/s]
PXD	8M	2	40	455M	—	—	4	800k	18.2G	—
SVD	243456	1.9	40	13.8M	HSLB	40	4	18.5k	555M	13.8M
CDC	14336	10	302	0.6M	HSLB	75	4	6k	175M	2.3M
BPID	8192	2.5	128	7.5M	DSP	16	16	4k	120M	8M
EPID	65664	1.5	78	1.1M	HSLB	20	2.8	2.8k	84M	4.2M
ECL	8736	33	52	7.7M	HSLB	26	4	12k	360M	15M
BKLM	19008	1	16	9.7M	HSLB	6	8	2K	60M	10M
EKLM	16800	2	66	19.5M	HSLB	to be fixed	4	1.4k	42M	5.3M
TRG					HSLB	10				

Fixed by proposed layout

Overview of KLM Crate Utilization



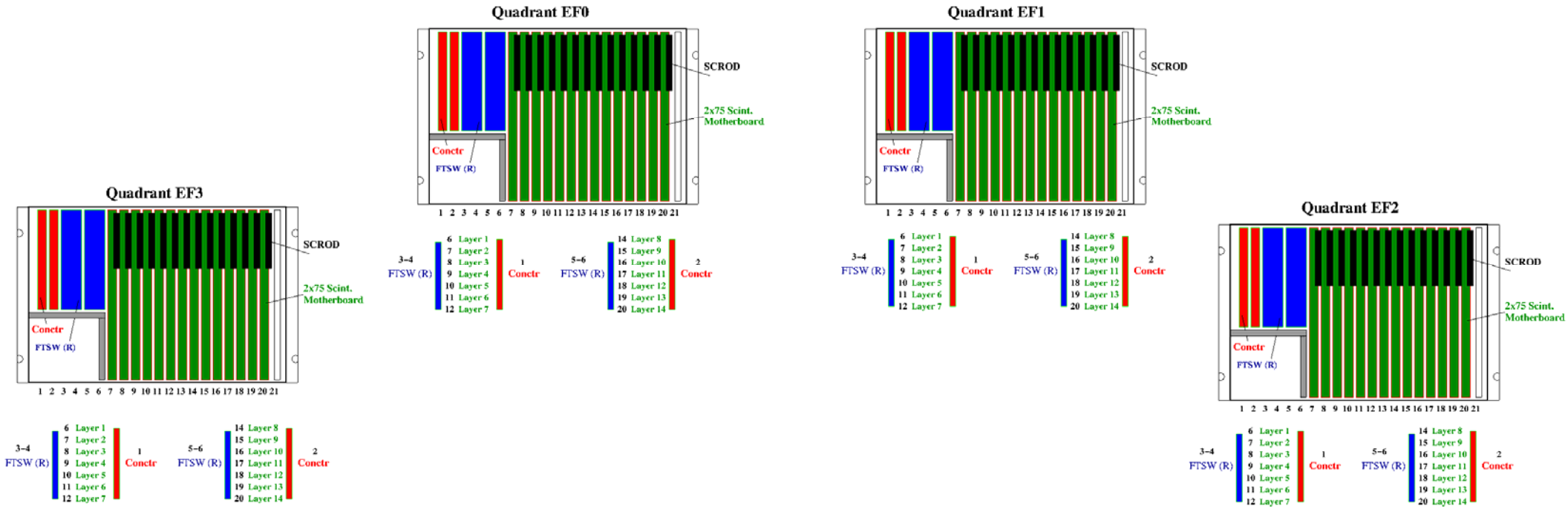
Belle Crate Configuration shown

Plan is to re-use locations, but with the following changes:

1) All endcap 6U crates are removed
2) 8 new 9U (COPPER) crates for endcap are installed (4x each end, 2x each door)
3) 4 new 9U (COPPER) crates for barrel scint are installed (BF4, BF0, BB4, BB0)
4) **ARICH and TOP FTSW located in 8 crates (BF0 .. BF7) and (BB0 .. BB7) respectively**

Forward
Endcap (Scintillator) KLM

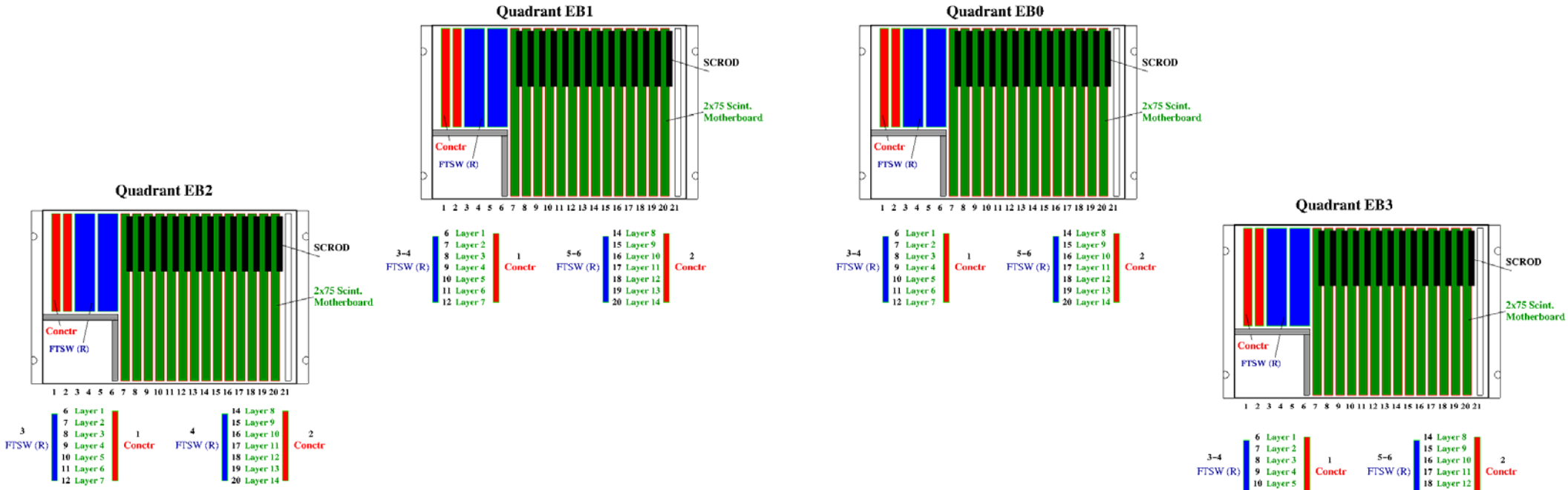
Forward Endcap KLM (Oho side –– view toward Oho)



Right Endcap Door | **Left Endcap Door**

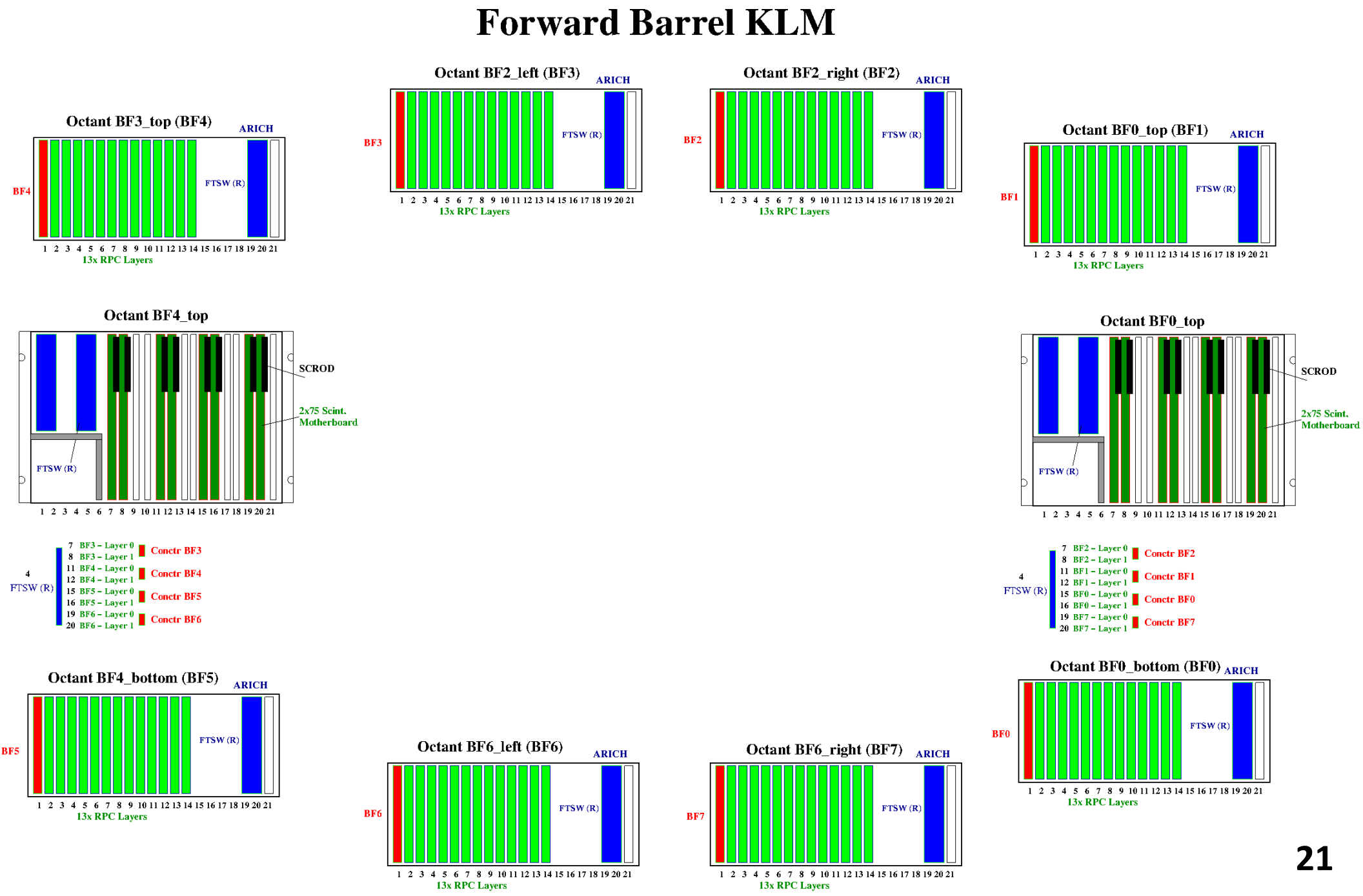
Backward
Endcap (Scintillator) KLM

Backward Endcap KLM (Nikko side –– view toward Nikko)

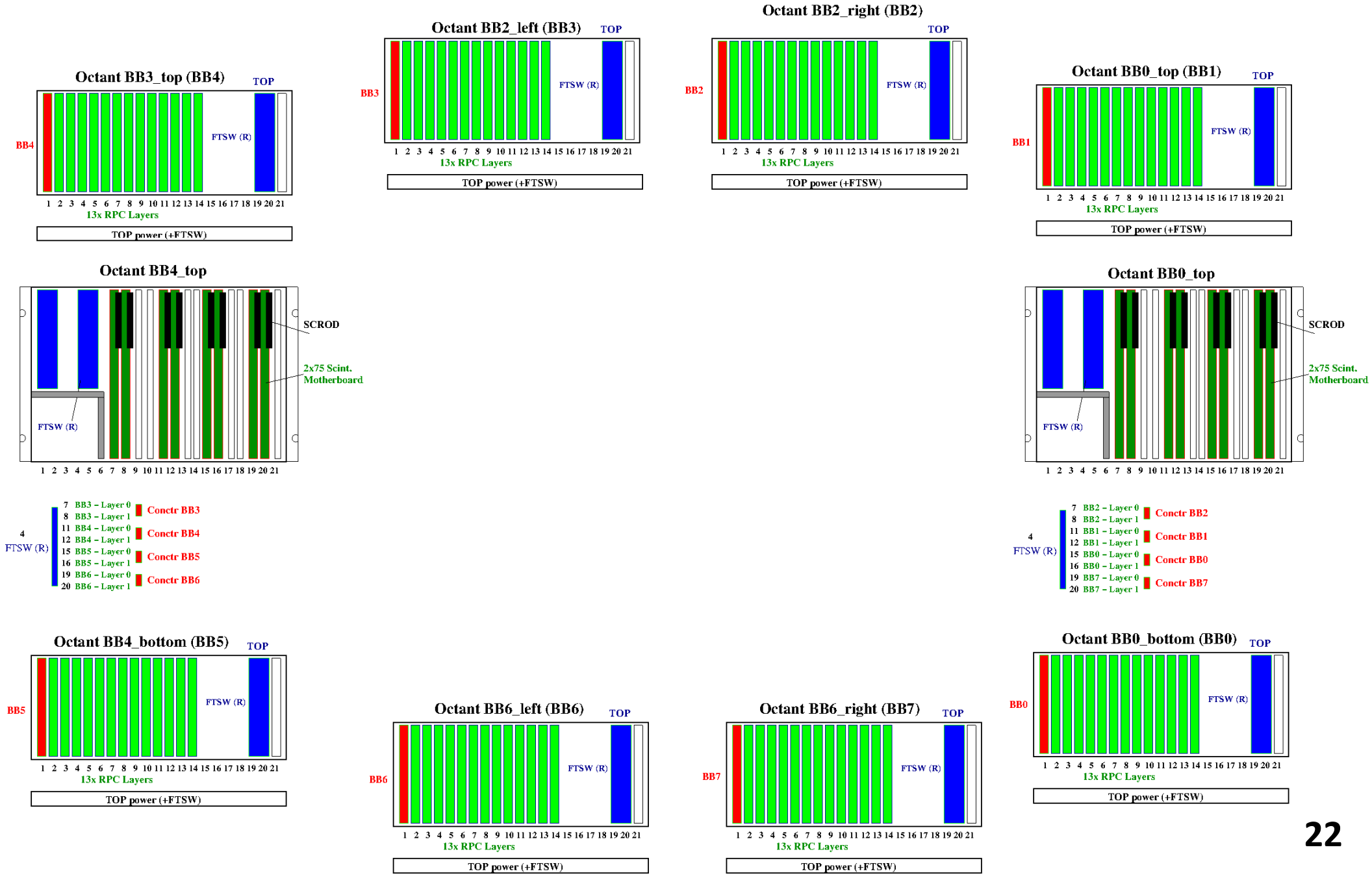


Right Endcap Door | **Left Endcap Door**

Forward Barrel KLM



Backward Barrel KLM



KLM Readout Tasks

- SRM firmware lagging (KEK/ITEP)
  - Some experience in recent tests at KEK
  - Installed modules ready to be read out
- Pre-amps, carrier cards produced (cabling/testing @ Wayne State)
- (pre-)Production TARGET7(X) ASIC (Hawaii)
- TARGET6 daughtercard (Hawaii)
- 9U VME version 2 of SRM (Hawaii)
- Trigger/fiber merge board (Indiana)
- Trigger firmware (Virginia Tech)

KLM Readout Summary

- TARGET6 vs. TARGETX (TARGET7 w/KLM trigger)
  - TARGET6 testing in progress
  - TARGET7 just received (January TARGETX submission)
- Daughtercards almost same (MC, RHIC same)
- Mechanical support/cable strain relief
- Could start taking cosmic data (barrel & endcap) right away
- Manpower shortage identified
- Production resources needed