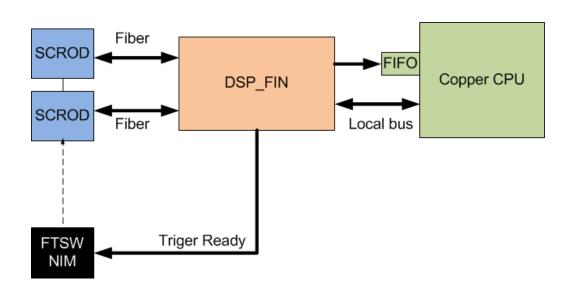
FINESSE Redesign



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- Current design has:
 - Limited throughput between FPGA and DSP
 - Outdated components
 - Clunky DSP support
- Goal of redesign:
 - Simplify design/layout wherever possible
 - Flexible processing capabilities
 - Looked at Zynq,
 Virtex-5 w/ PowerPC,
 Virtex-7, CPUs



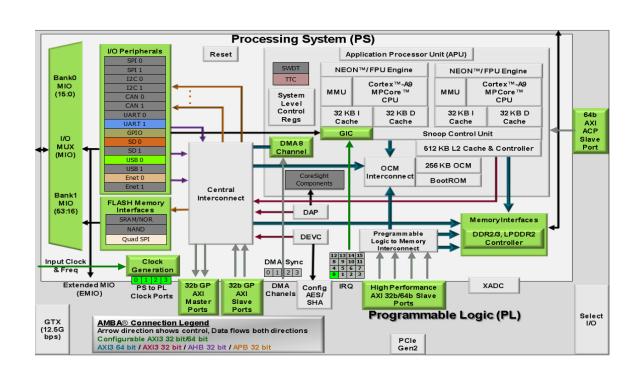
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Proposed Processing Unit



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- ► Based on Xilinx Zync SoC (XC7Z045 or XC7Z030)
 - Kintex-7 FPGA (125-350K logic cells)
 - 667MHz up to 1GHz dual-core ARM Cortex-A9 (depends on speed grade)
 - 256KB on-chip memory, 8 DMA controllers
- Interconnect between FPGA and processor
- Support for bare metal, minimal kernels, Linux
 - XilKernel
 - **μC/OS**
 - eCos

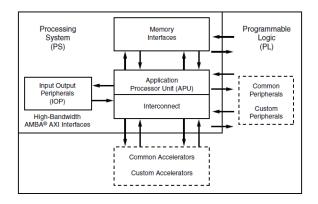


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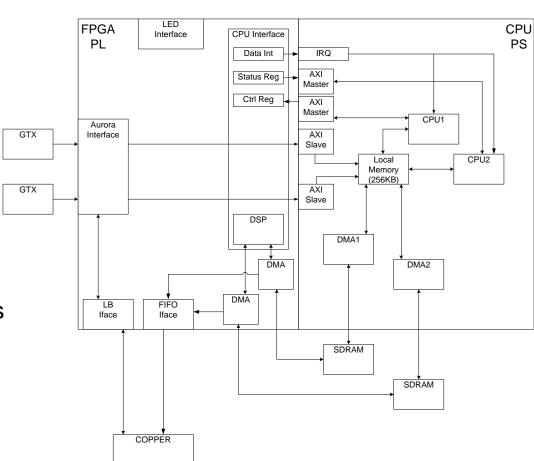
Data Handling



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- AXI interface to FPGA
- DMA controllers on both sides
- "heavy lifting" by FPGA, "steering" by CPU



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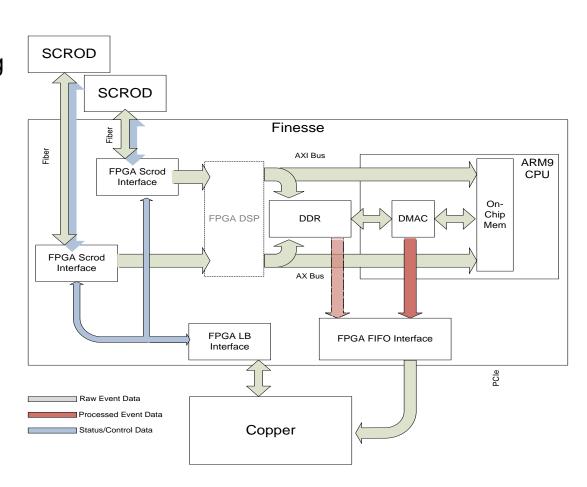
Data Handling



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Can combine FPGAand CPU-based processing

- FPGA receives data and stores to memory via DMA, notifies CPU
- CPU manages data, passes commands to FPGA for dedicated processing
- FPGA writes data to COPPER FIFO



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Potential Design Simplification



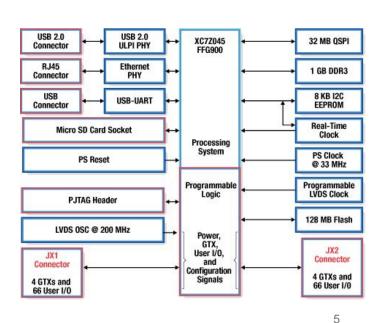
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- Use existing Zyng "module"
 - Simplify layout, memory, etc.
 - **BUT** most designed with XC7Z020 = no high-speed serial :v(
 - (talked to Enclustra, looking for large order to trigger design)





- Only vendor with Zynq > 020 is Avnet: "Zynq-7000 Mini-Module"
 - XC7Z045-1 (667 MHz)
 - 1GB DDR3, 128MB parallel flash, 32MB QSPI flash
 - All GTX ports come off board
 - Debug: microSD, USB/UART, JTAG, CPU JTAG
- Possible concerns:
 - Size: width, height?
 - Heat dissipation?
 - Power?
 - Cost (spendy, \$1400 = FPGA cost)
 - Nice if we could find a 030-based board (~\$300?)



Next Steps



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- First draft of design document complete
 - Posted to indico page for this meeting
 - Just a first pass, looking for lots of discussion
- Need better understanding of:
 - Data rates
 - Required processing