



ANITA III - SURFv4



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- SURFV4: ANITA-III readout motherboard

An Introduction to the Acronyms

- SURFv4
 - Signal Unit for Radio Frequency signals.
- ASIC
 - Application-Specific Integrated Circuit.
- LAB4B (LABRADOR-4 revision B)
 - Large Analogue Bandwidth Recorder and Digitizer with Ordered Readout.
- RITC2
 - Real-time Independent Three-bit Converter



SURFv4

Design improvements from SURFv3:

- 1) Short buffer depth of 250 samples
- 2) Reduce crosstalk in high frequencies (10%)
- 3) Ability to trim time differences between samples and thus save power



SURFv4 (The Lead Board)

- 1) 12 LAB4B ASICS
- 2) 4 RITC2 ASICS
- 3) 3, 676 pin, 8 gate, FPGAs (5/5 clearance rules required for break out routing)
- 4) Over 1300 additional parts

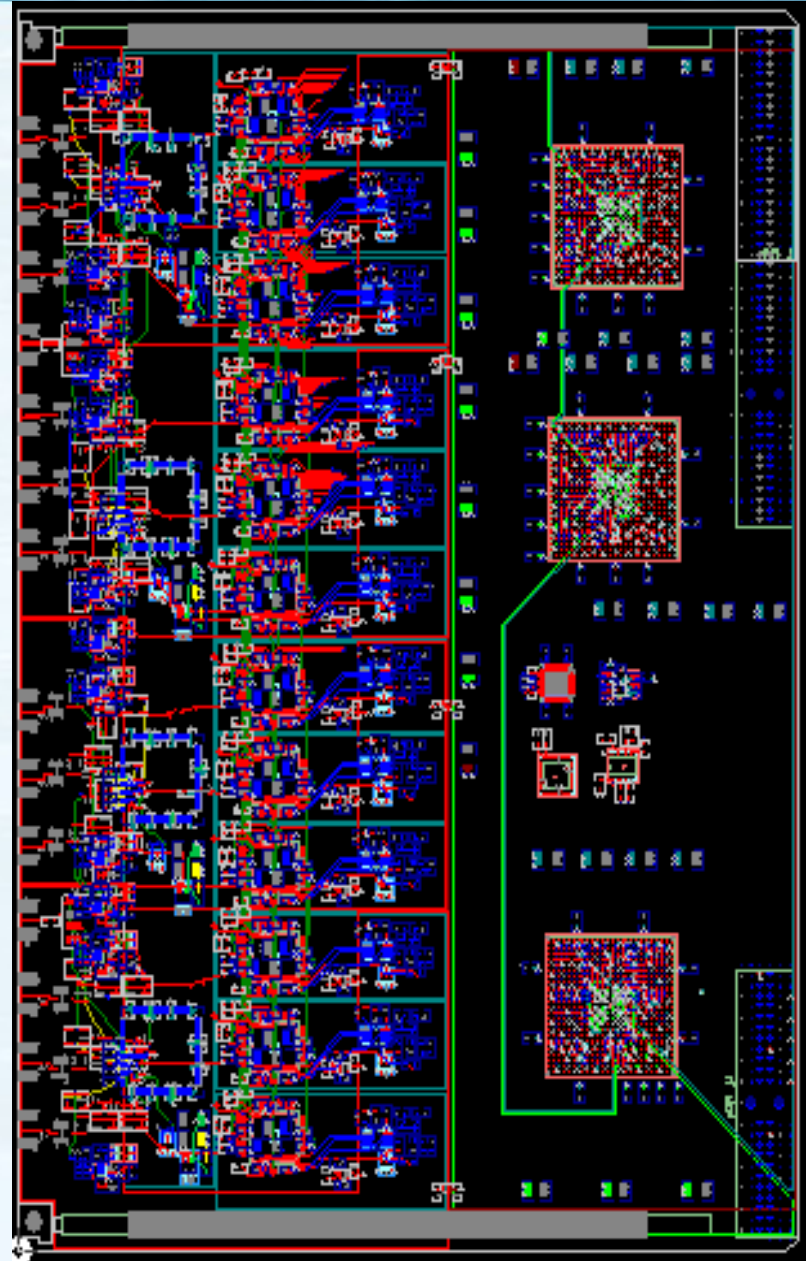


SURFv4 Layer Definition

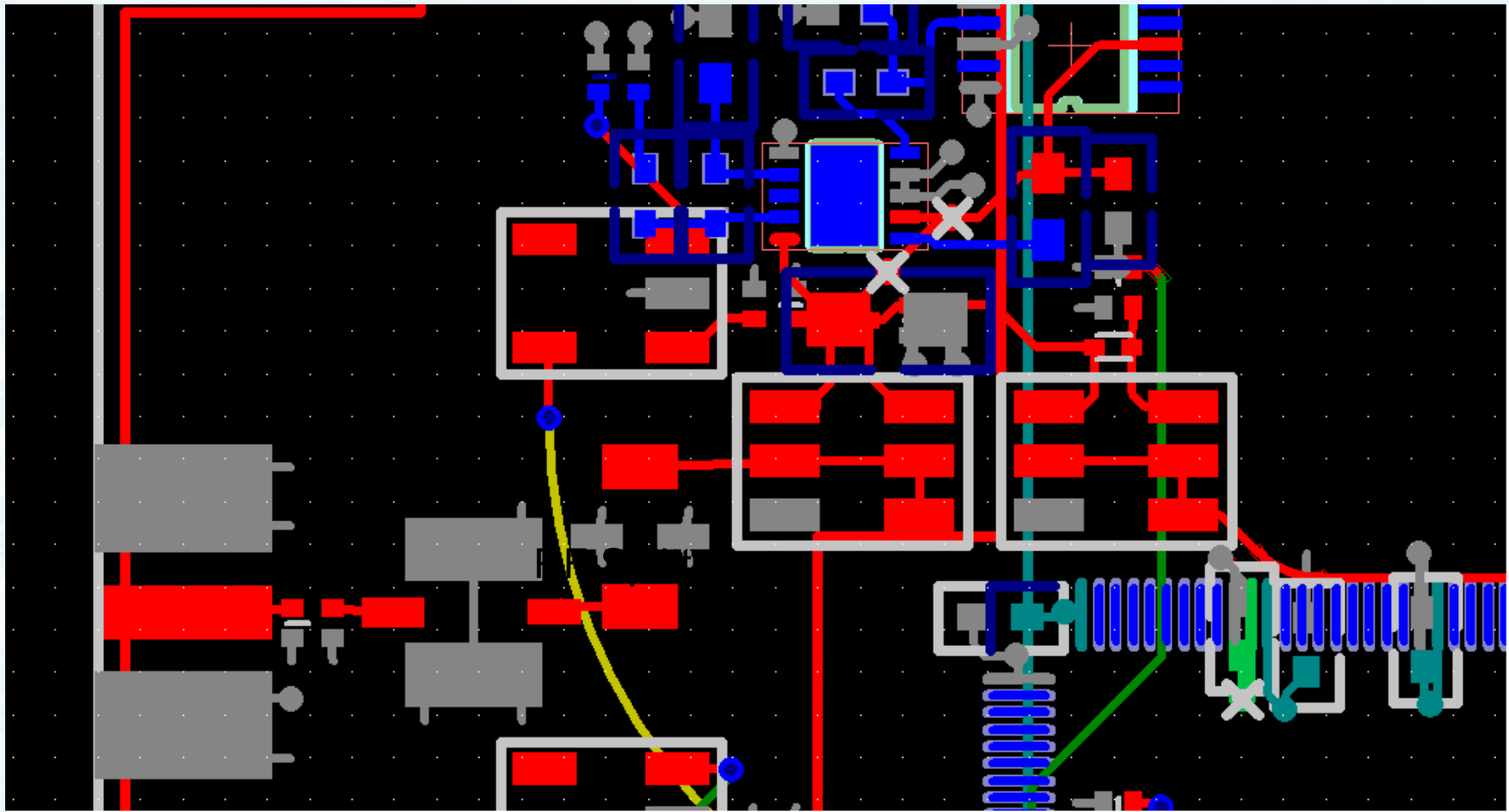
- 12 electrical layers
 - 1 - Top
 - 2 - GND1
 - 3 - SIG 1
 - 4 - PWR 1 (mixed power plane)
 - 5 - SIG 2
 - 6 - PWR 2 (MPP)
 - 7 - SIG 3
 - 8 - PWR 3 (MPP)
 - 9 - GND 2
 - 10 - SIG 4
 - 11 - GND 3
 - 12 - Bottom

SURFv4 Board general Layout

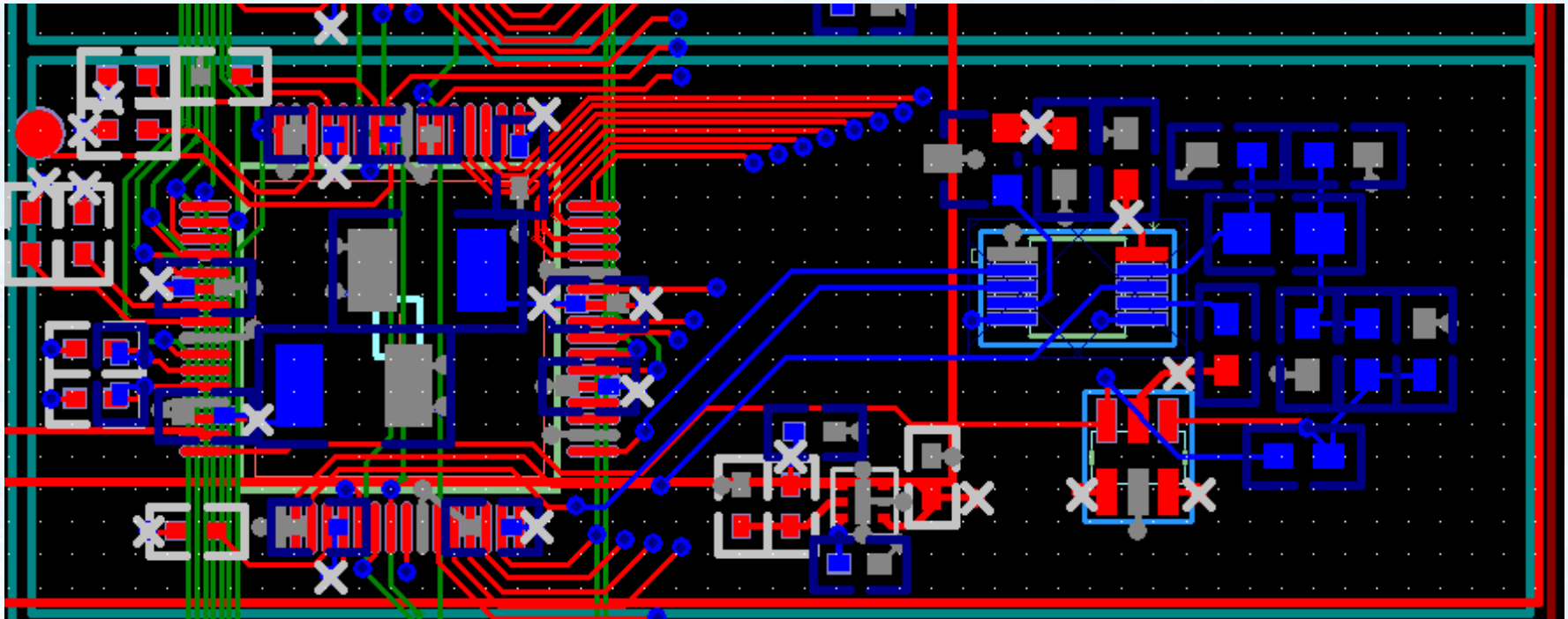
- 1) Input RF signals left
- 2) RF splitters + power monitors by input signals
- 3) RITC2s place on bottom s input signals
- 4) LAB4s place on top layer as close to inputs as possible
- 5) 3 FPGAs near CPCI connectors/outputs



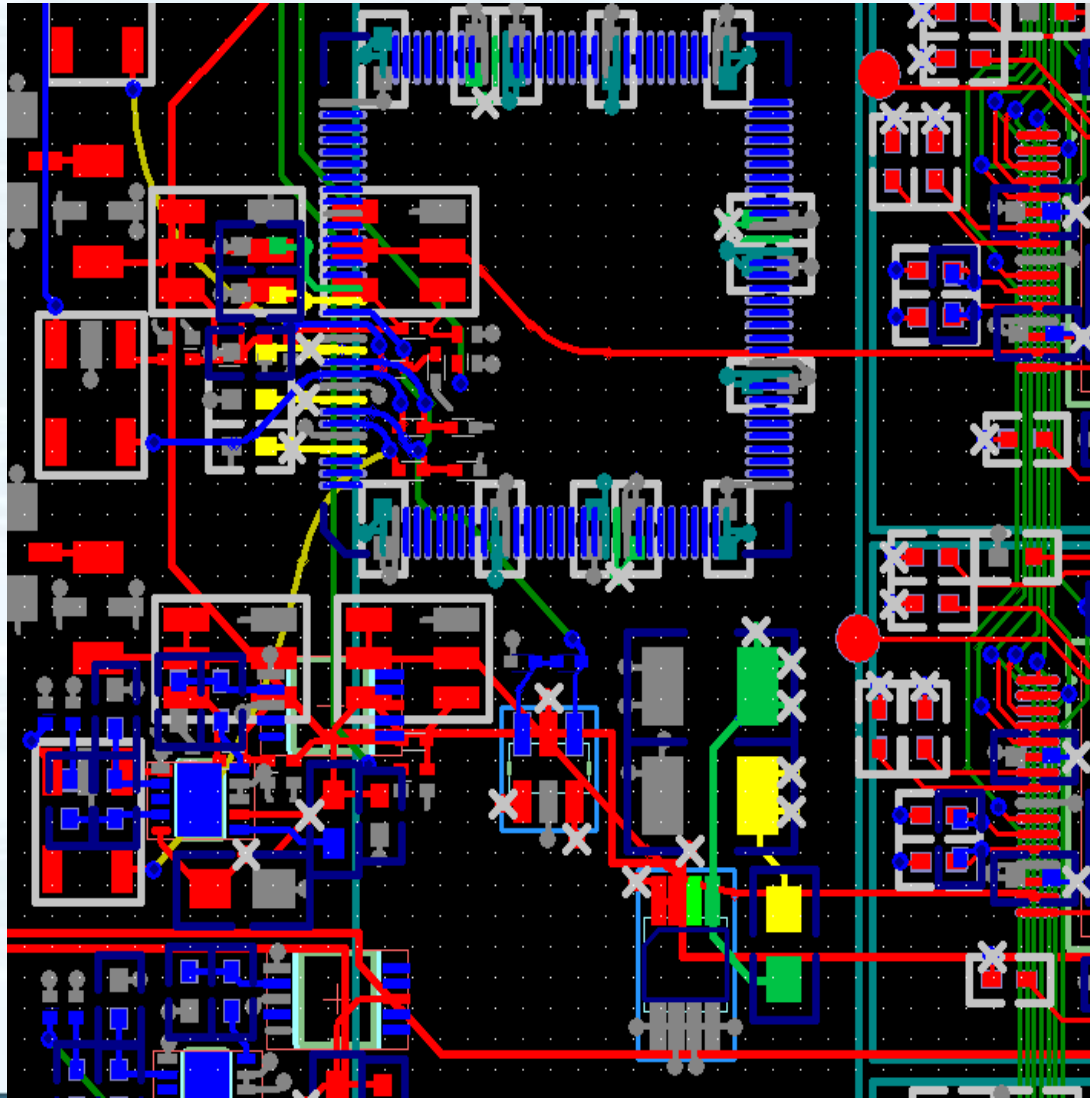
A closer look at the input chain...



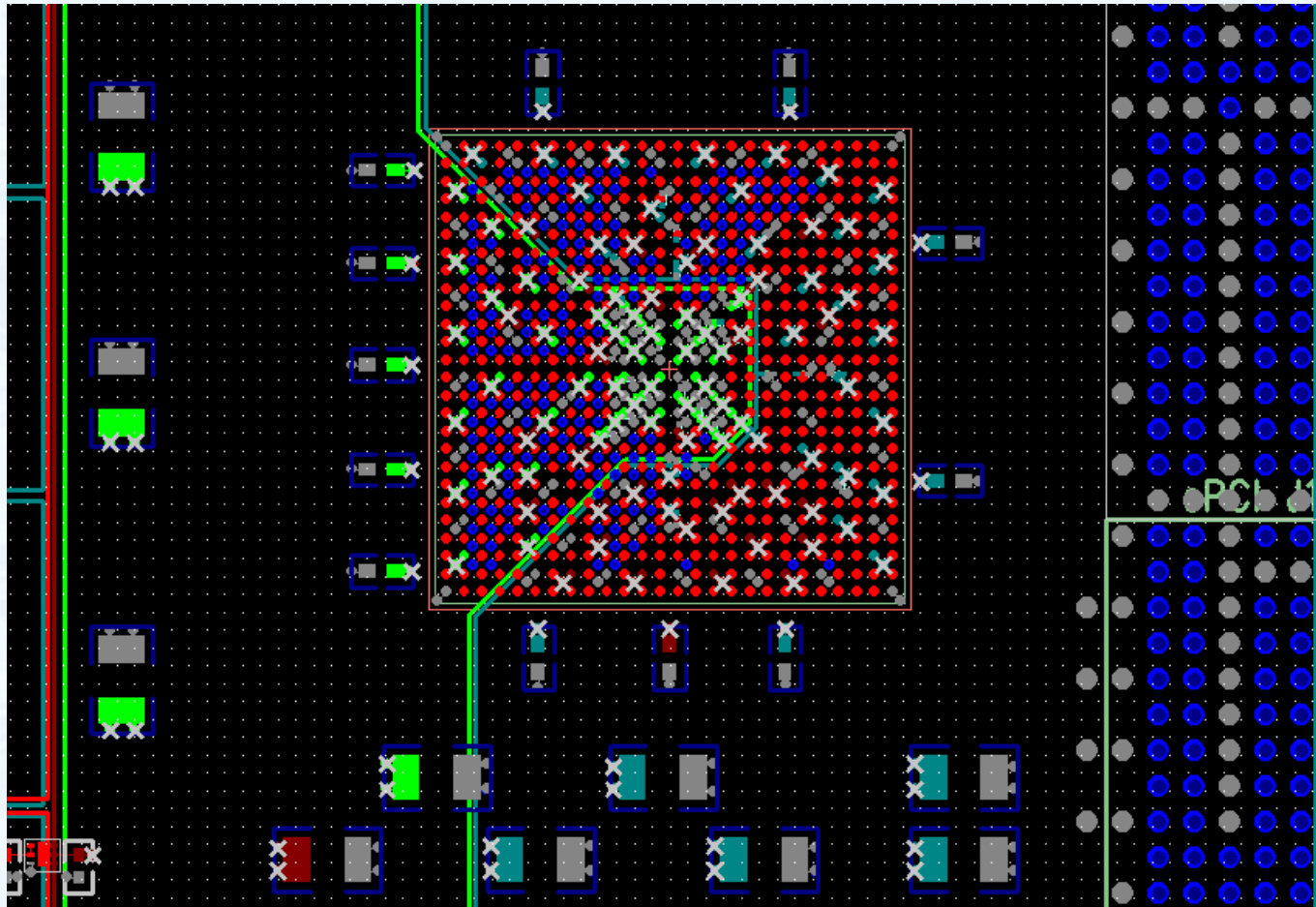
A closer look at the LAB4 + voltage regulator...



Powered RITC2 on bottom layer (Temp reg.?)



FPGA fanout and bypass cap arrangement.



Conclusion

- Due to high density the SURF is (very) difficult to route.
- Introduction of a daughter board for the RITC2 may be a possible solution.
- Status of RITC2?
- Status of power monitor?
- Status of LAB4B?