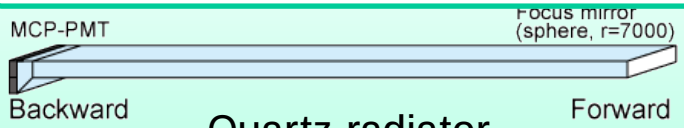
Specifications/Constraints, missing Specs

Particle Identification

Barrel PID: Time of Propagation Counter (TOP)



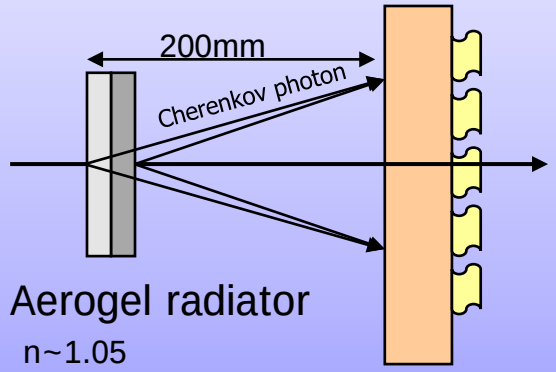
Quartz radiator

Focusing mirror

Small expansion block

Hamamatsu MCP-PMT (measure t, x and y)

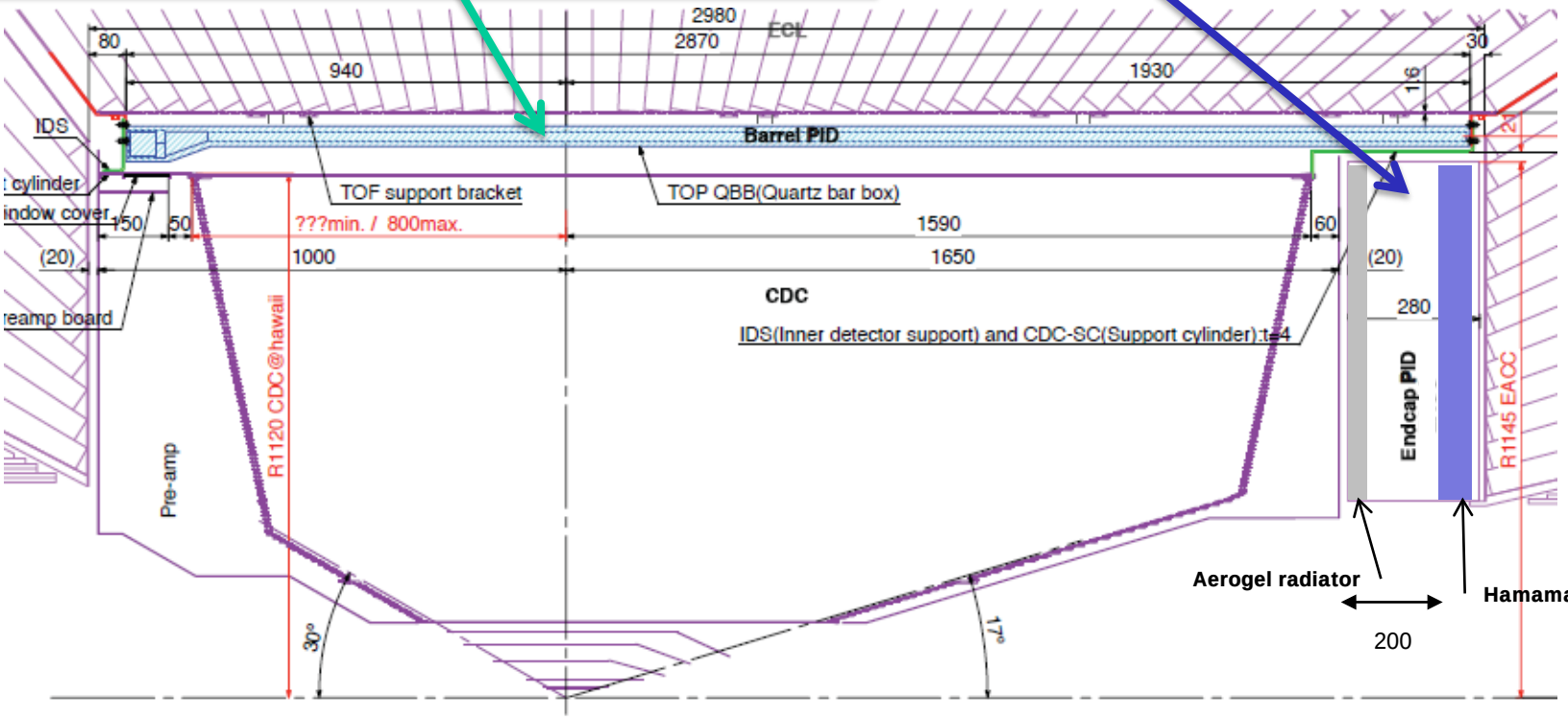
Endcap PID: Aerogel RICH (ARICH)



Aerogel radiator

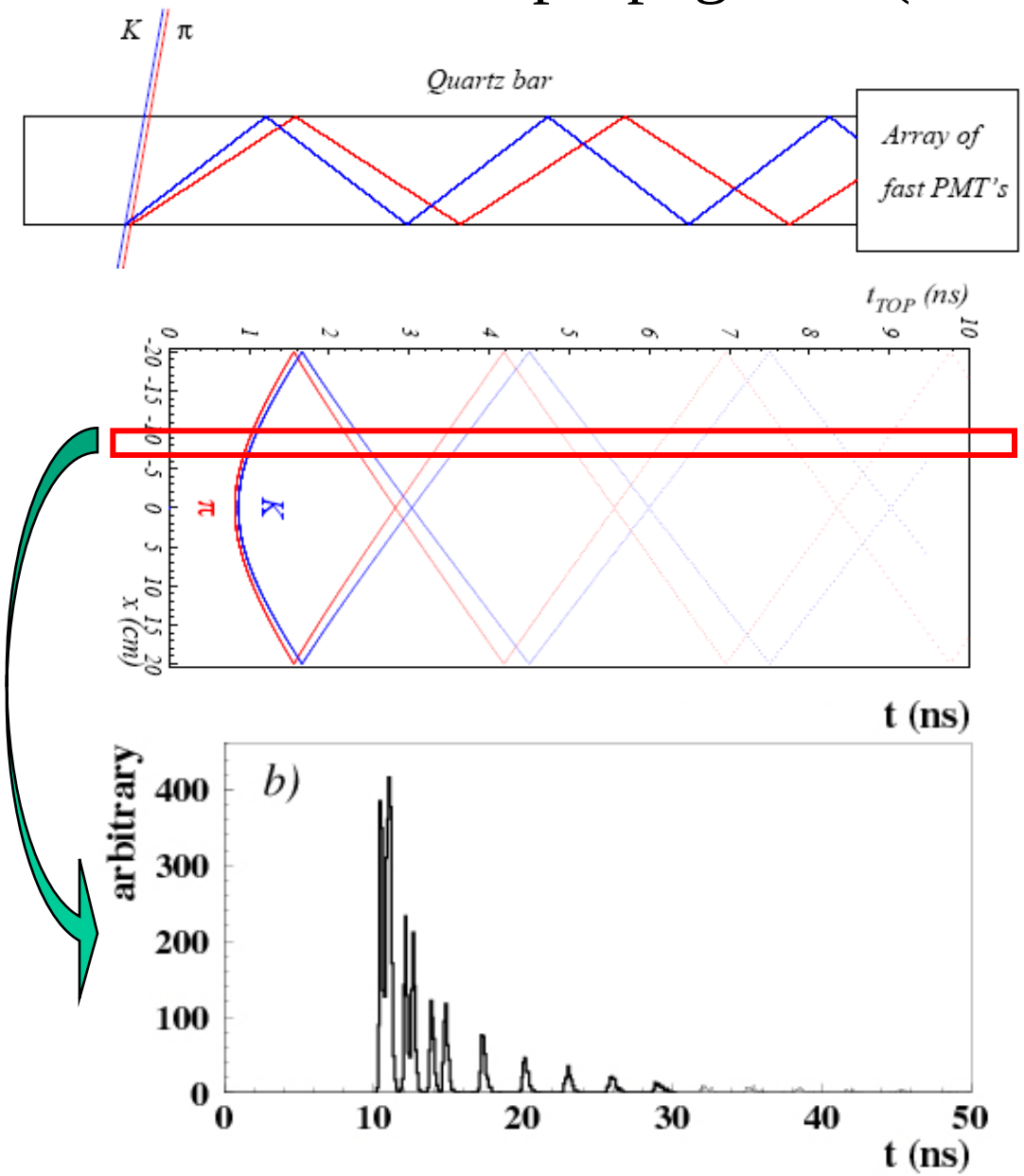
n~1.05

Hamamatsu HAPD
+ new ASIC



Barrel PID: imaging

Time of propagation (iTOP) counter

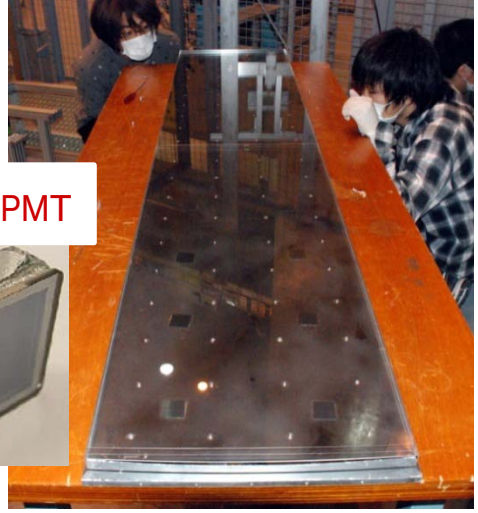


- Cherenkov ring imaging with precise time measurement.
- Reconstruct angle from two coordinates and the time of propagation of the photon
  - Quartz radiator (~2cm)

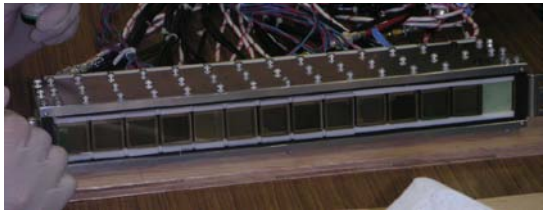
Time distribution of signals recorded by one of the PMT channels: different for **p** and K

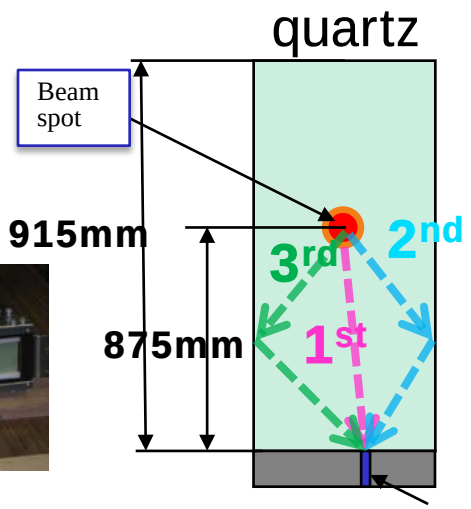
TOP (Barrel PID)

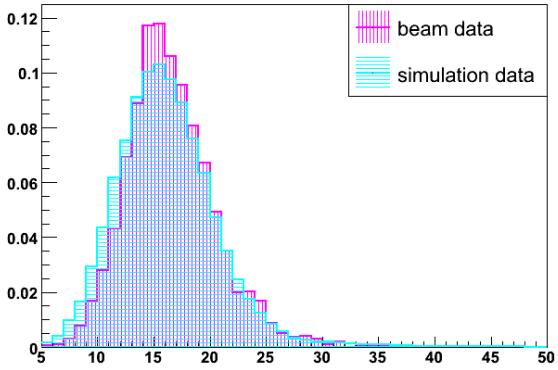
- Quartz radiator
  - $2.6m^{L}$ x $45cm^{W}$ x $2cm^{T}$
  - Excellent surface accuracy
- MCP-PMT
  - Hamamatsu 16ch MCP-PMT
    - Good TTS (<35ps) & lifetime
    - Multialkali photo-cathode → SBA
- Beam test in 2009
  - # of photons consistent
  - Good time resolution



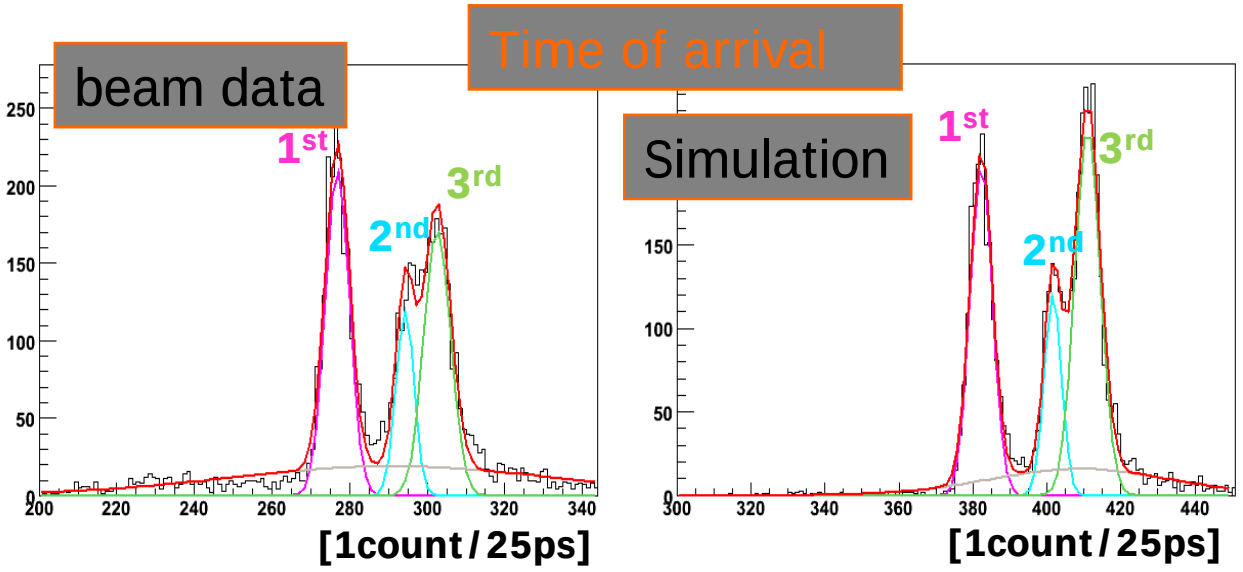
SL10 MCP-PMT





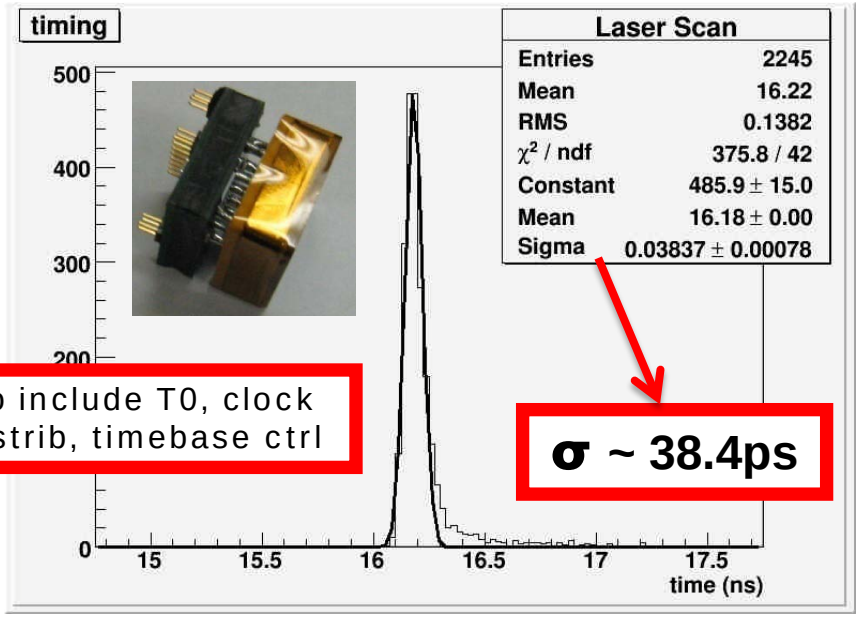


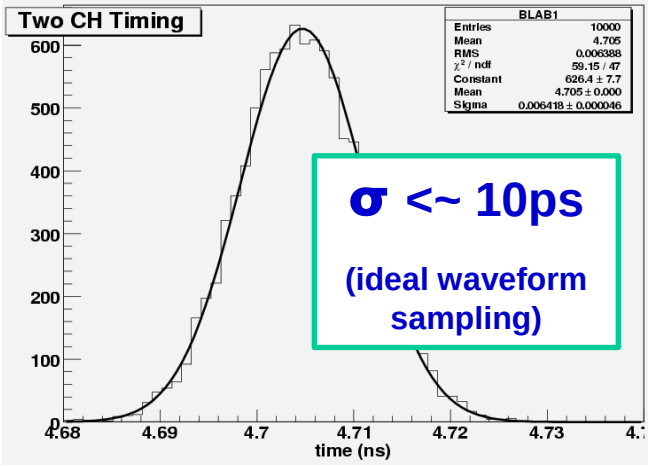
# of photons



Particle ID basis (TOP)

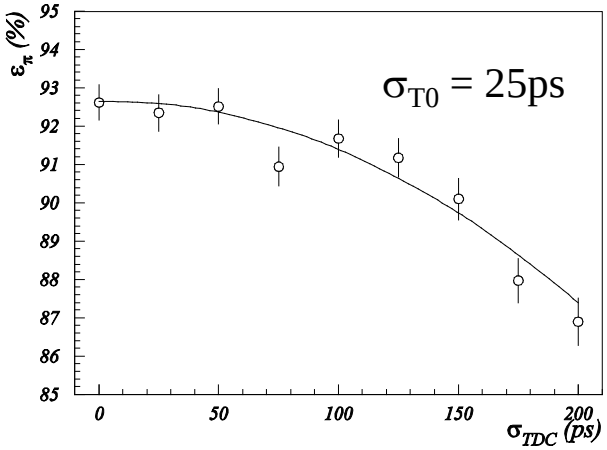
- Single photon timing for MCP-PMTs

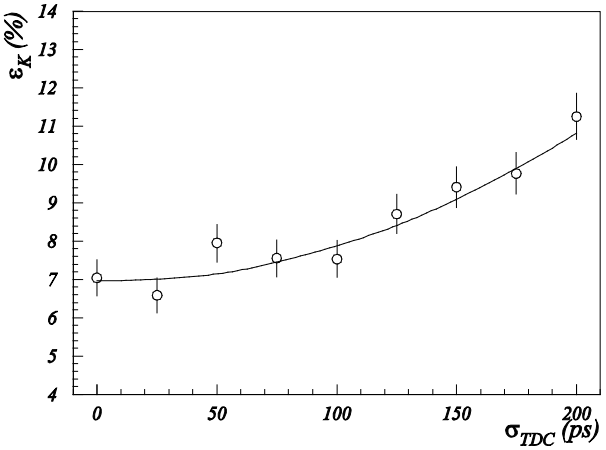




NIM **A602** (2009) 438

σ <= 100ps ➔ 1% impact





σ <~ 50ps target

NOTE: this is single-photon timing, **not** event start-time "T_0"

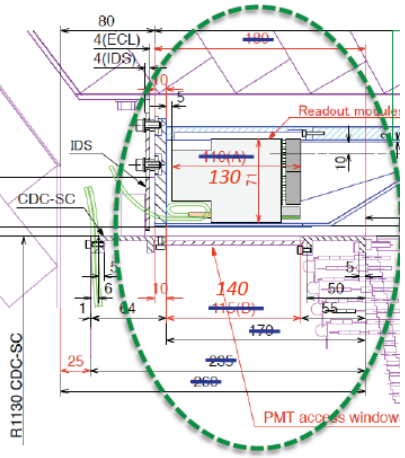
TOP Overview/Design Constraints

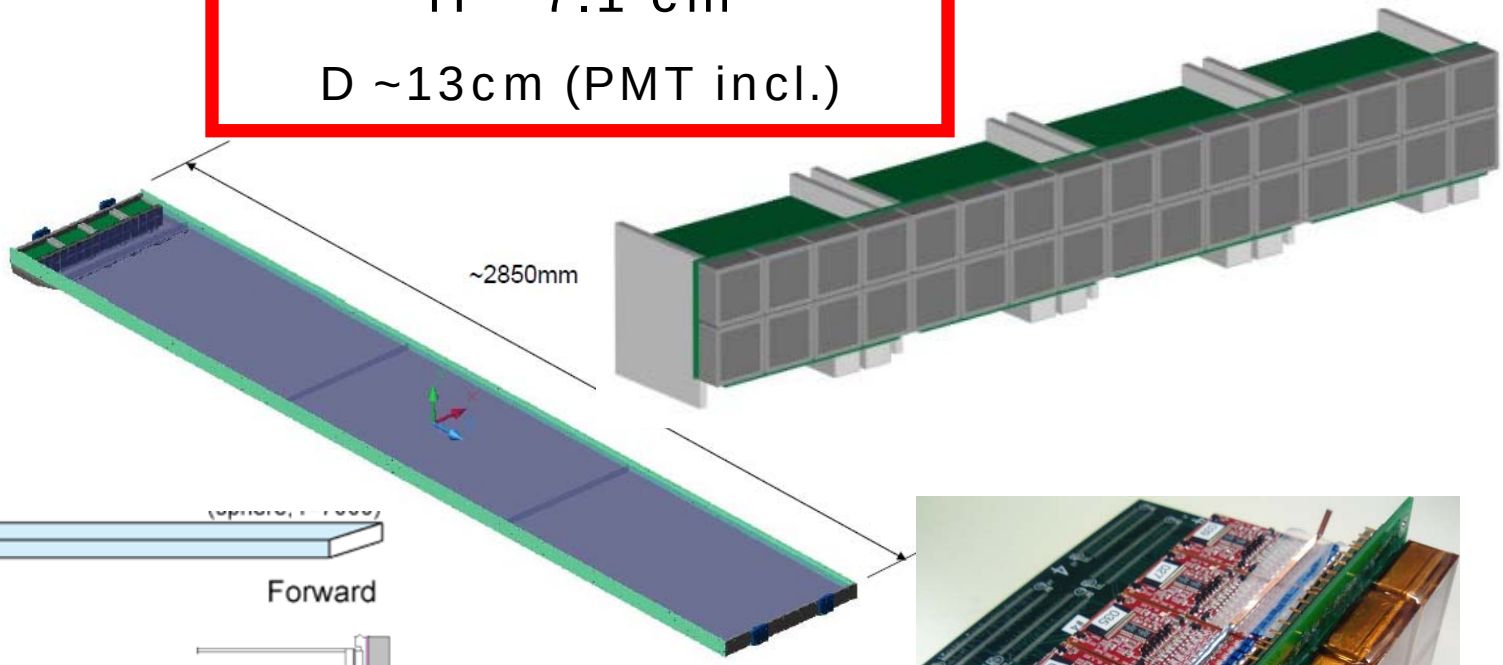
- Must fit in a very crowded envelope

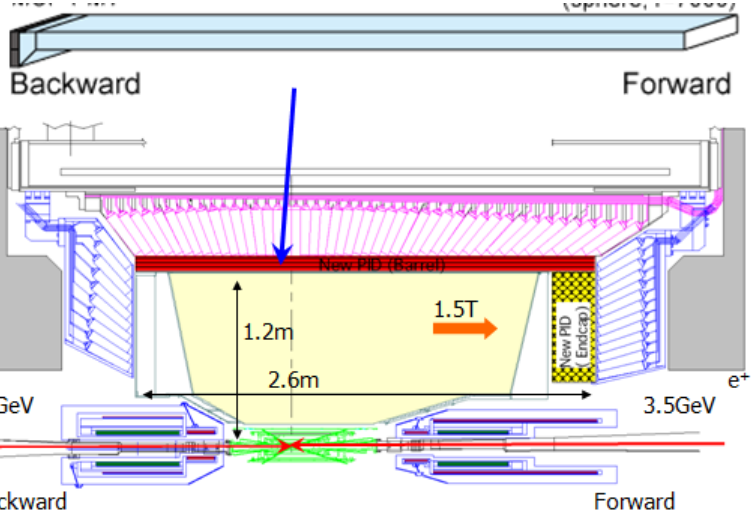
H ~ 7.1 cm

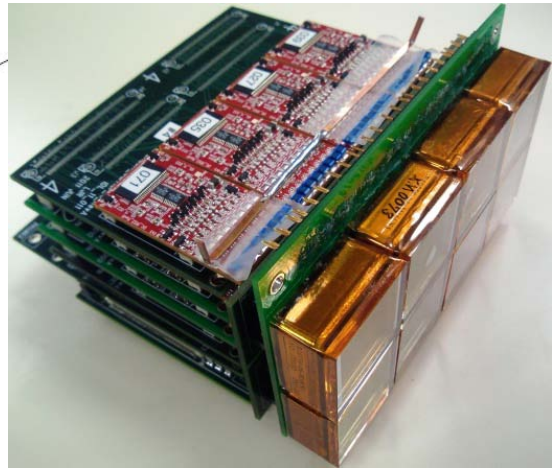
D ~13cm (PMT incl.)

512 channel readout

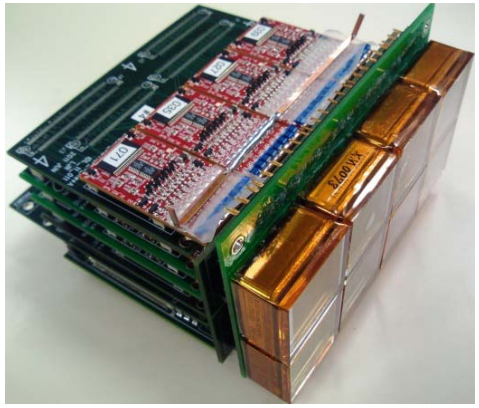




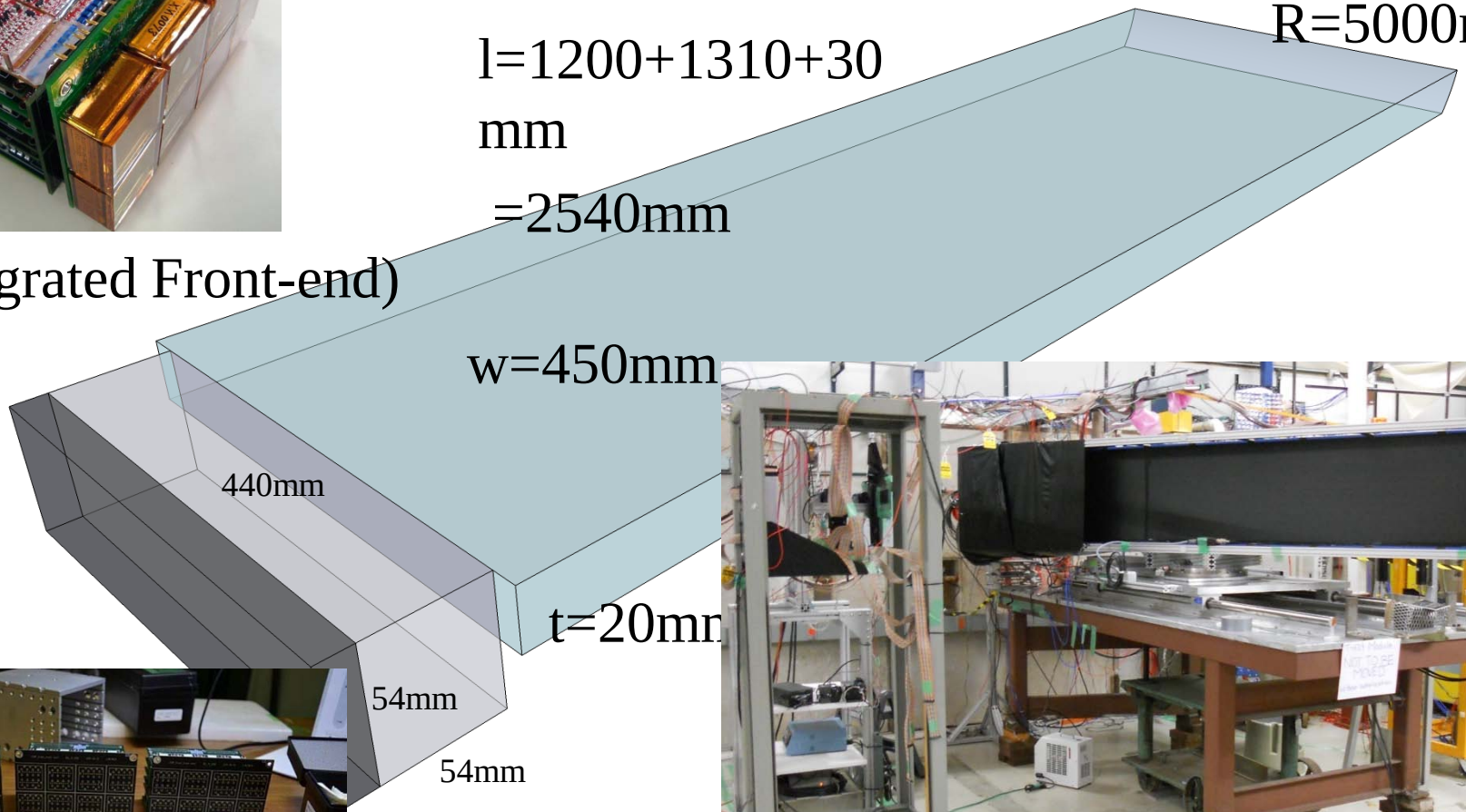


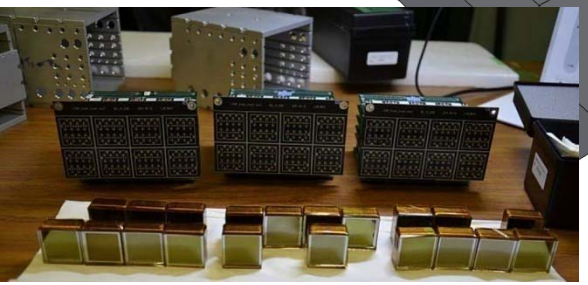


2011-2012 Fermilab Beam Test



(Integrated Front-end)

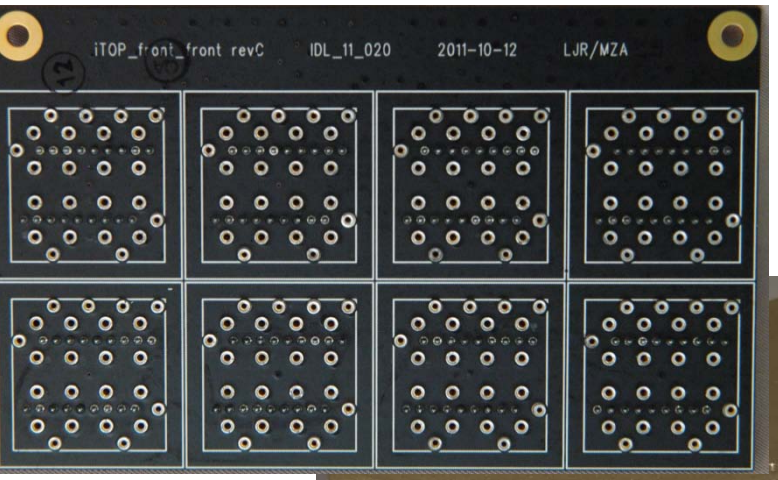


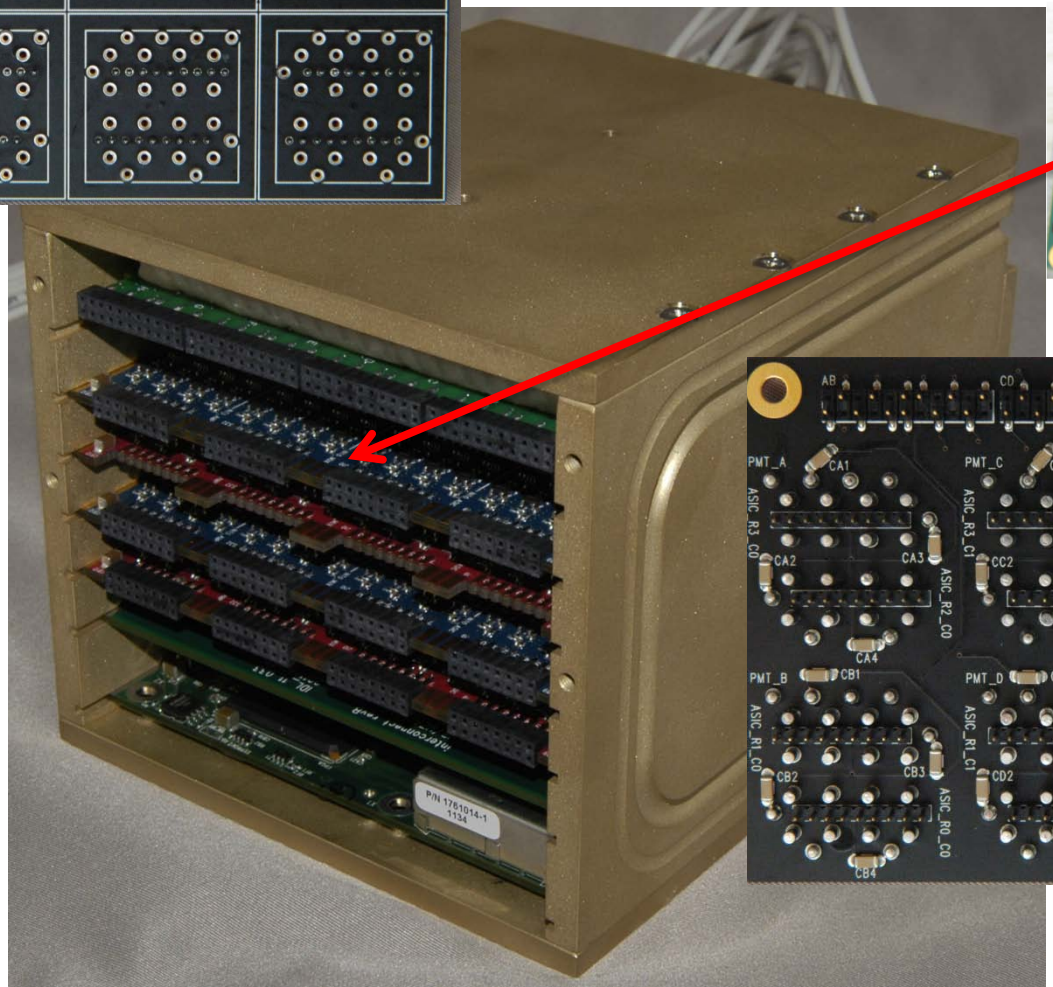


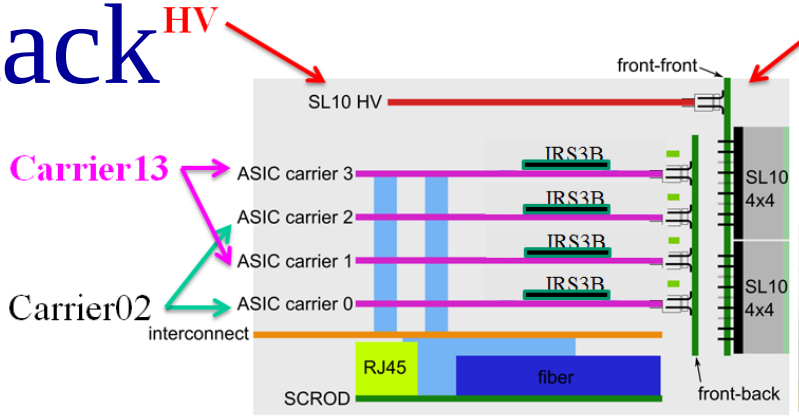
Fermilab Beamtest Prototype Lessons

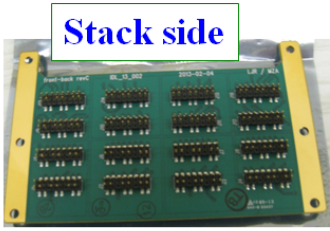
1. ASIC configuration, sampling issues
2. Timebase stabilization (servo-loop)
    1. Firmware needed to be re-written
    2. Improved phase control
3. SCROD module (“final” form factor)
4. Better thermal management (85C redline ops)
5. HV divider redesign; packaging SL-10 into module by HPK/Nagoya
6. Demonstrate DSP (real time) data reduction
7. In-situ (on demand) calibration

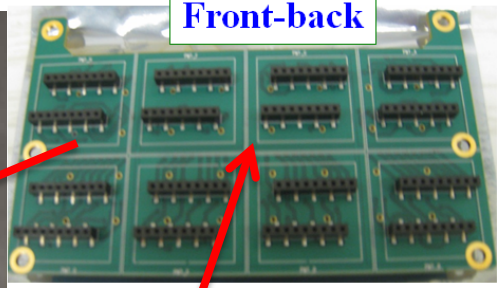
Rev. A2 board stack

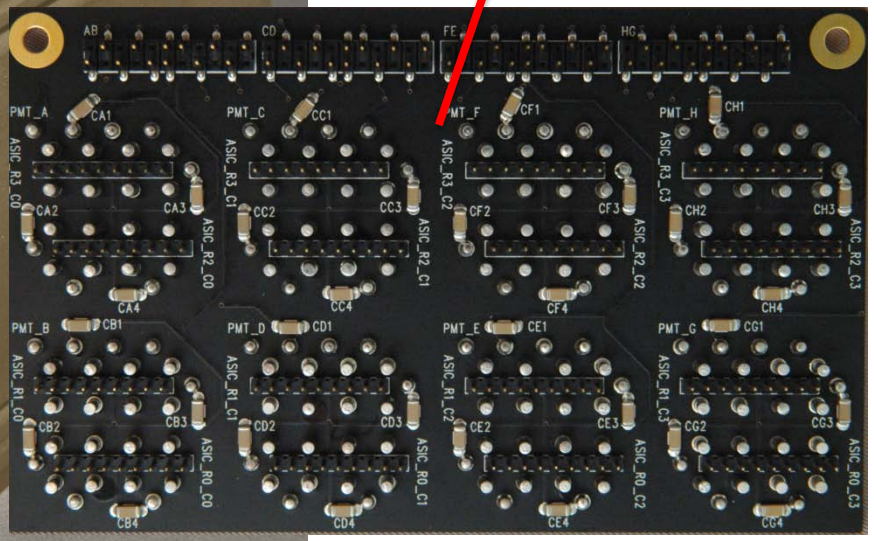












9

Items Prior to Production

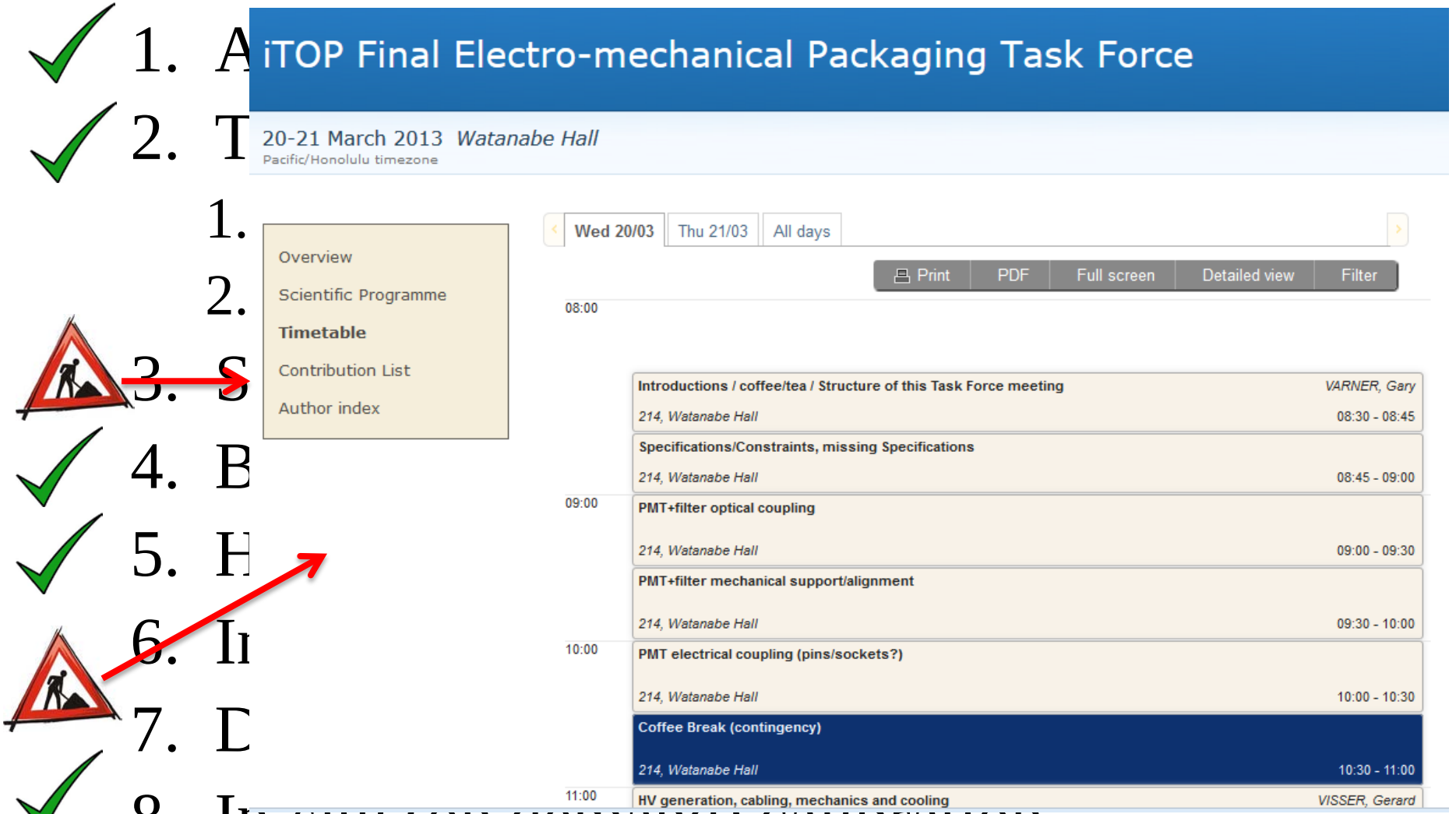
1. ASIC configuration, sampling issues
2. Timebase stabilization (servo-loop)
    1. Firmware needed to be re-written
    2. Improved phase control
3. SCROD module (“final” form factor)
4. Better thermal management (85C redline ops)
5. HV divider redesign
6. Improved SL-10 electro-mech interface
7. Demonstrate DSP (real time) data reduction
8. In-situ (on demand) calibration

= Demonstrated

= to be done “pre-production”

Items Prior to Production

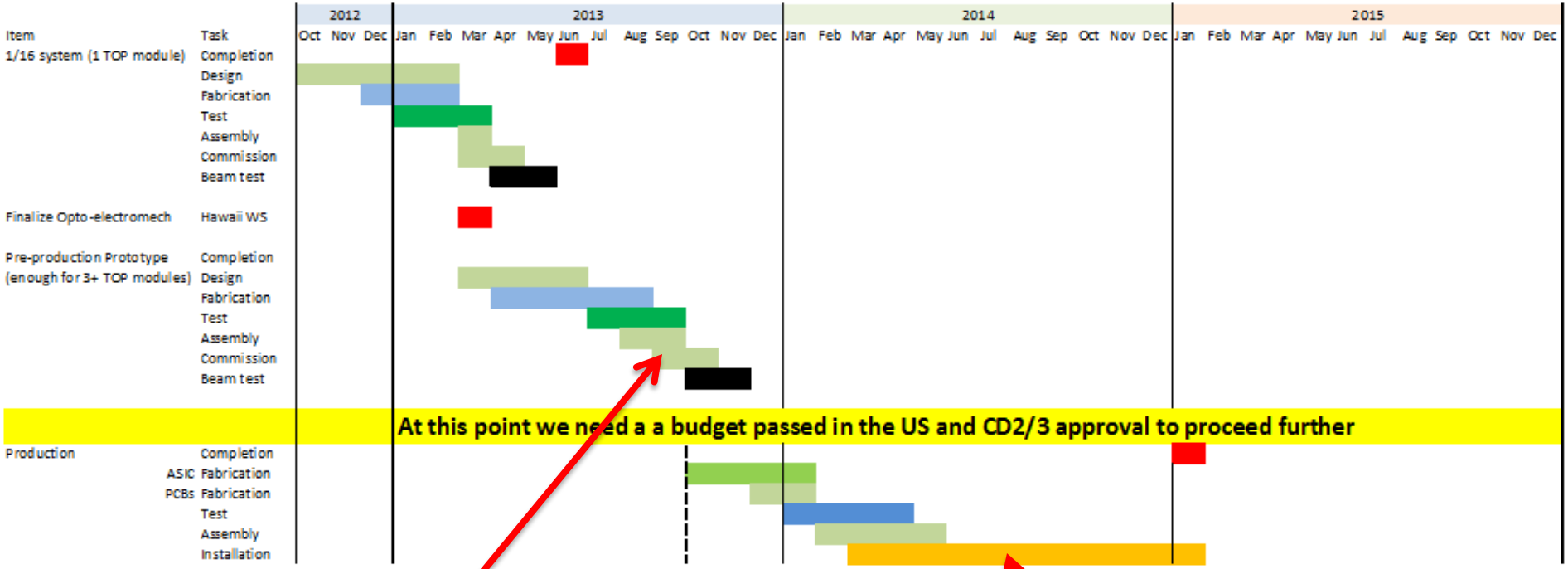
1. A
2. T
   1.
   2.
3. S
4. B
5. H
6. In
7. C
8. In-situ (on demand) calibration



= **Demonstrated**

= **to be done "pre-production"**

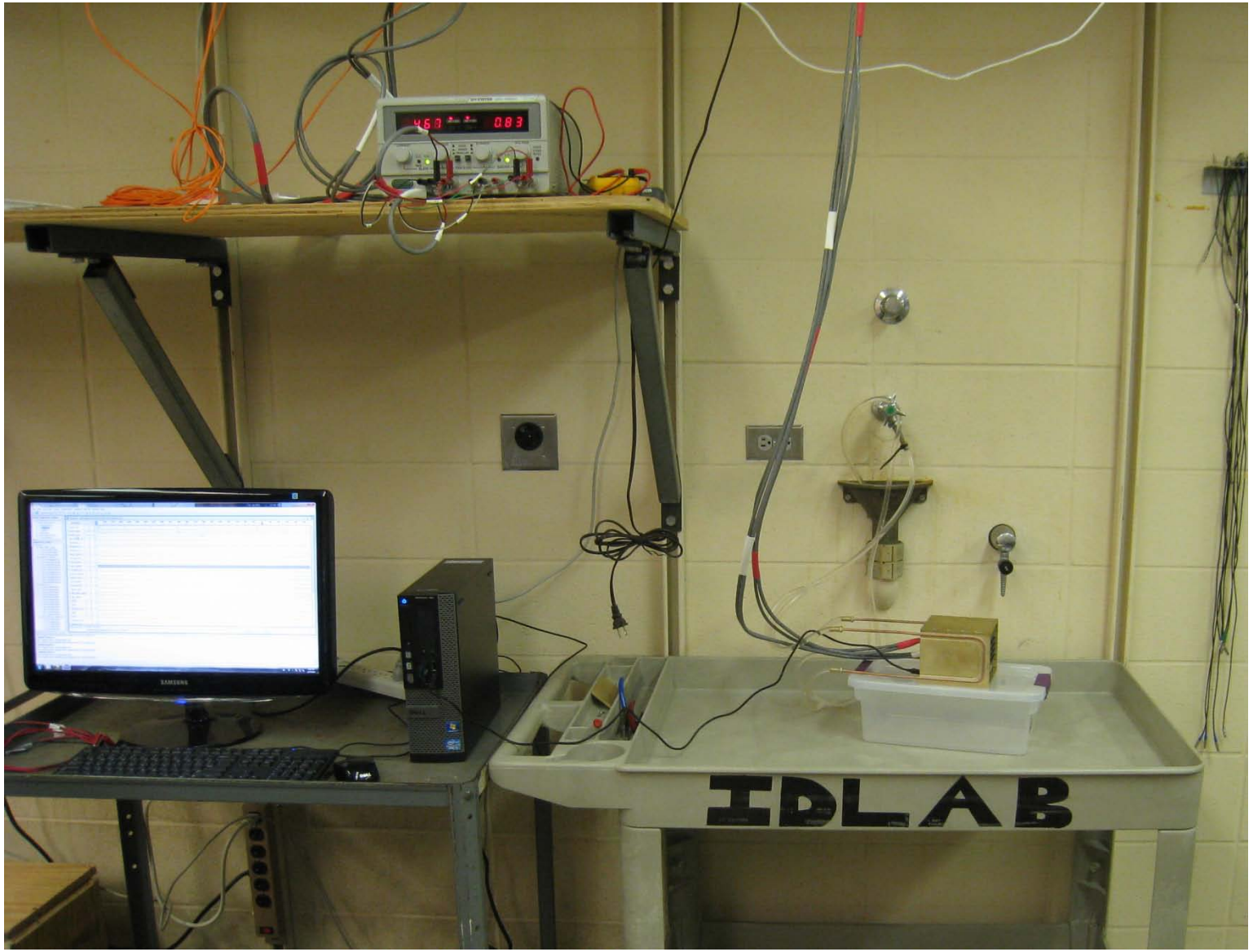
TOP Mechatronics Production Schedule



3+ TOP modules of readout

Install and operate completed modules in Fuji CRT

Back-up slides



Electronics Summary

• IRS3B working very well (only change is a possible method to reduce power-on current surge).
No major problems Rev A2 boards

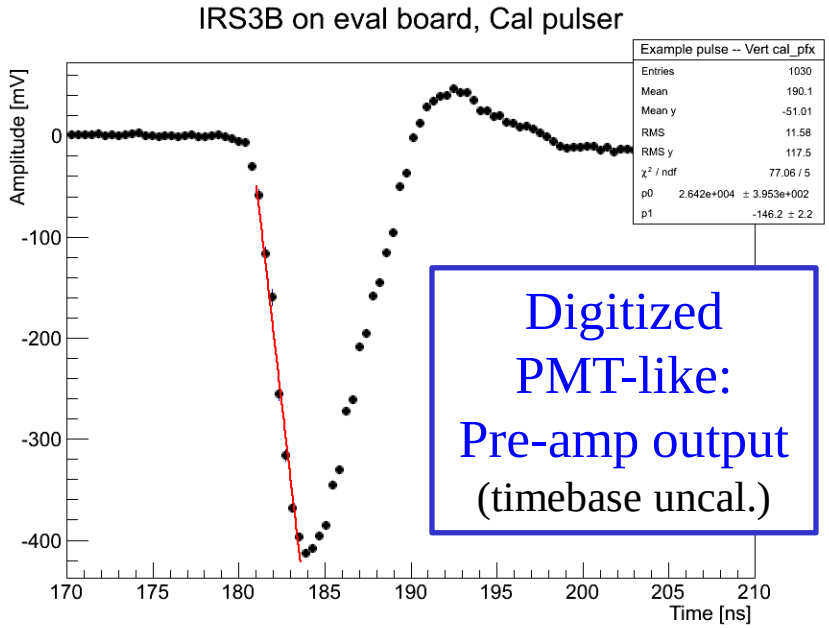
• Full TOP module worth of readout delivered for installation in Fuji Hall this week; integration with COPPER-based readout

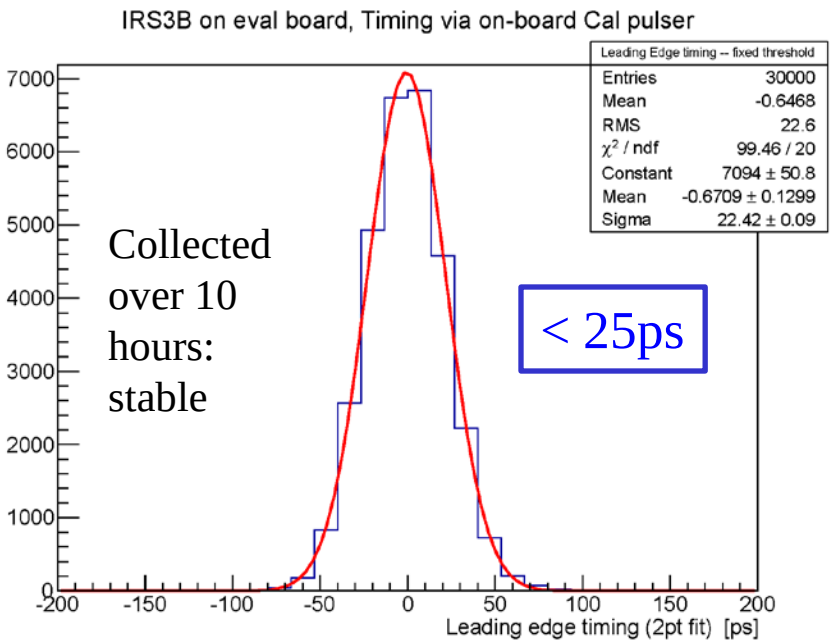
• Meeting March 20-21 @ Hawaii: Final E-O-M

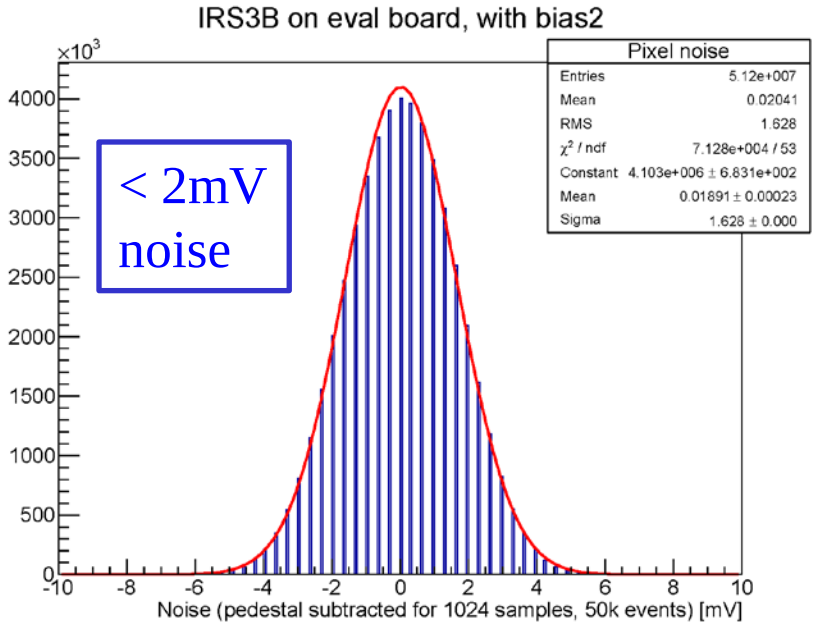
• Firmware piecewise working – needs to be integrated, debugged and commissioned (March)

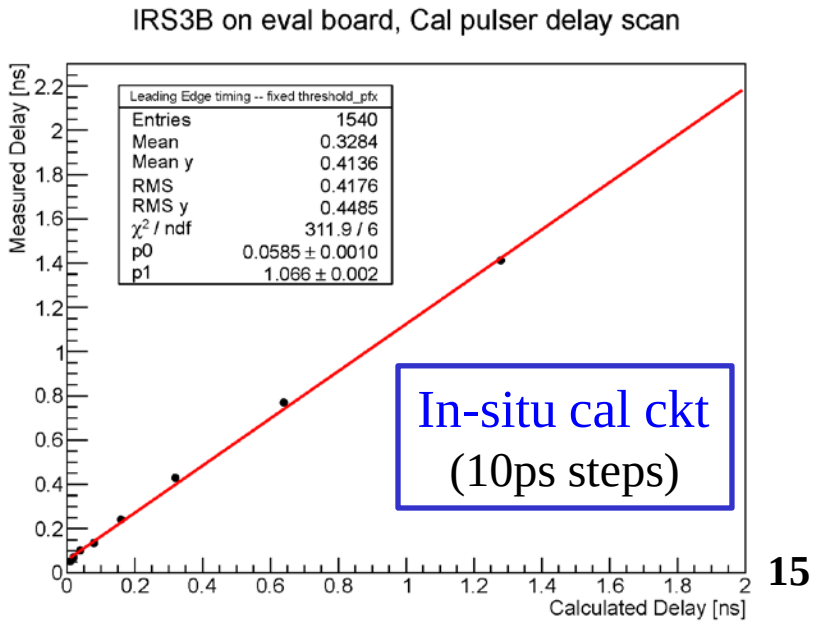
• **On schedule for April Cosmic Campaign Fuji Hall and definitive LEPS beam test in May**

IRS3B and Readout working well









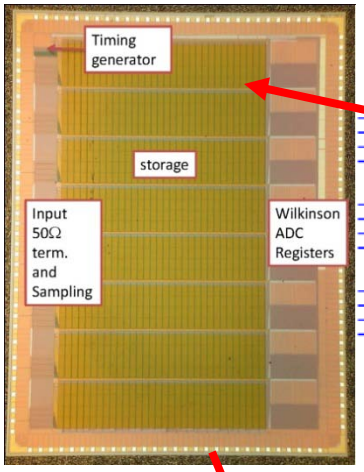
iTOP Readout

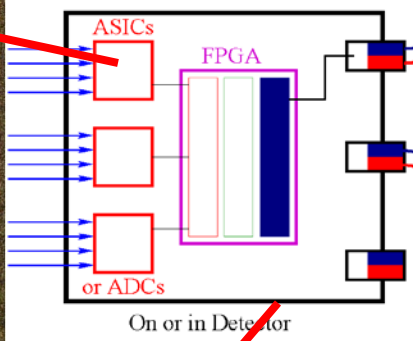
8 COPPER

<= 50ps single photon timing

BLAB waveform sampling ASIC

64 SRM

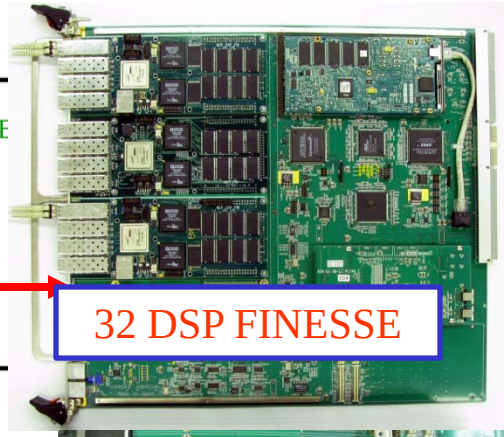




Giga-bit Fiber Transceiver Links

COPPER

FINESSE



Global Decision Logic

Clock/Event Timing Distribution

FPGA firmware consists of 3 parts:

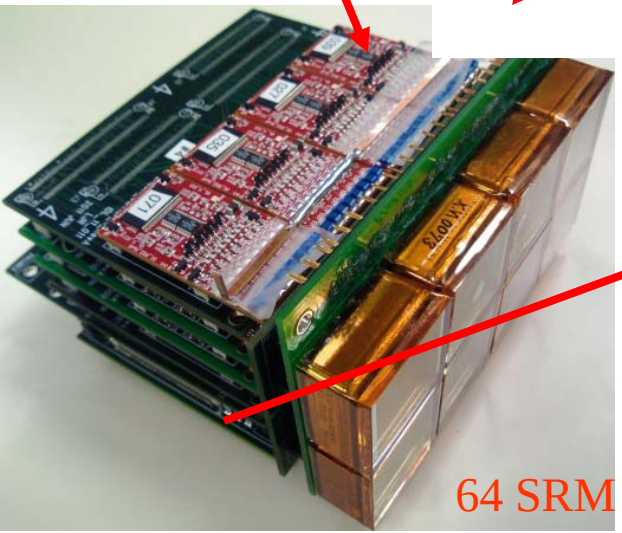
1) ASIC/ADC driver (common)

2) Trigger feature extract (subdet. specific)

3) Unified DAQ transport protocol

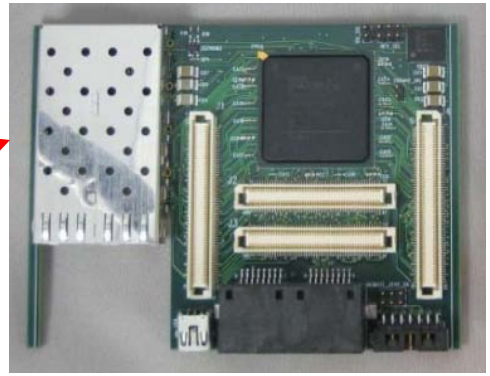
8k channels

1k 8-ch. ASICs



64 SRM

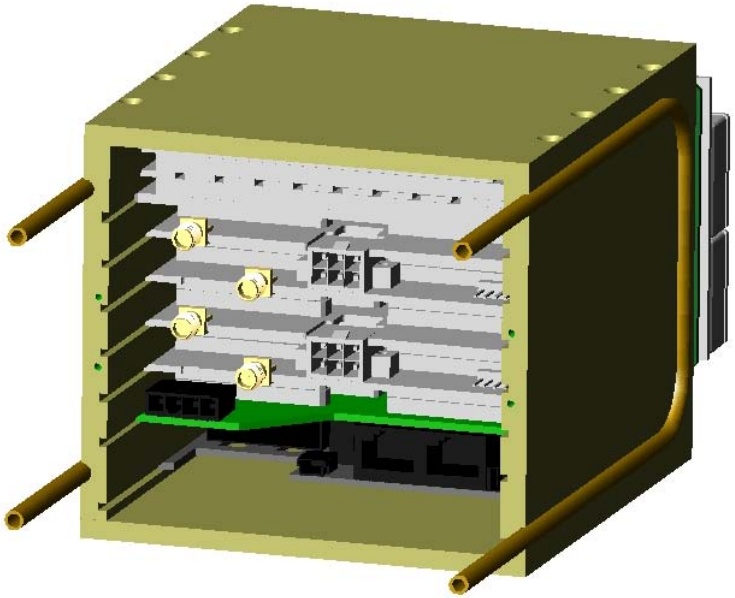
Digital control (SCROD)



FTSW clock, trigger, programming

8 FTSW

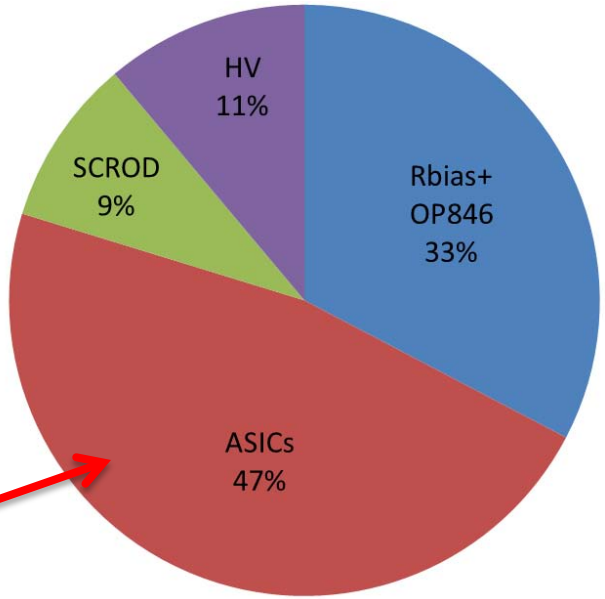
Improved packaging/thermal



About 31W per board-stack module

Full TOP, measured numbers

Rbias+OP846	40	W
ASICs	57.6	W
SCRODs	11.2	W
HV	13.6	W
Total	122.4	W



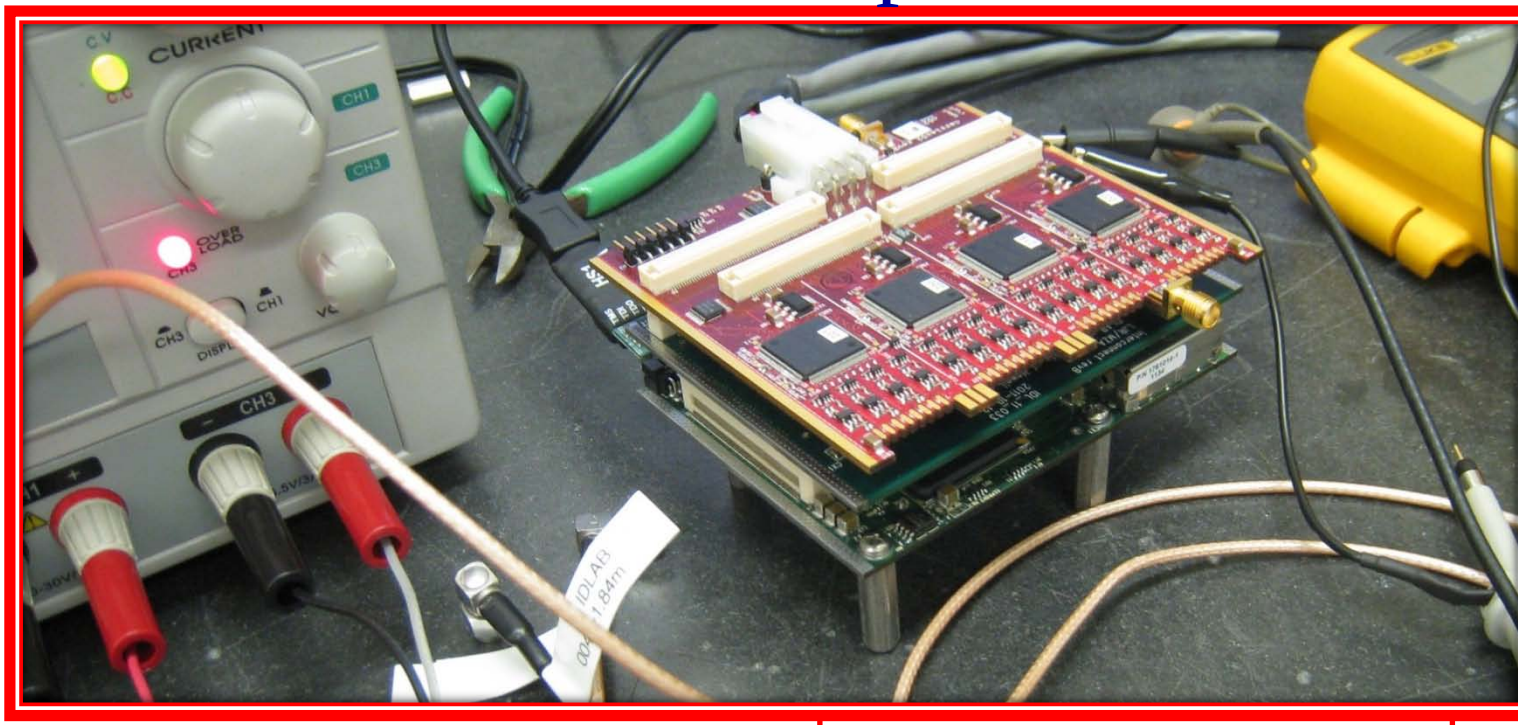
May be possible to tune biases lower

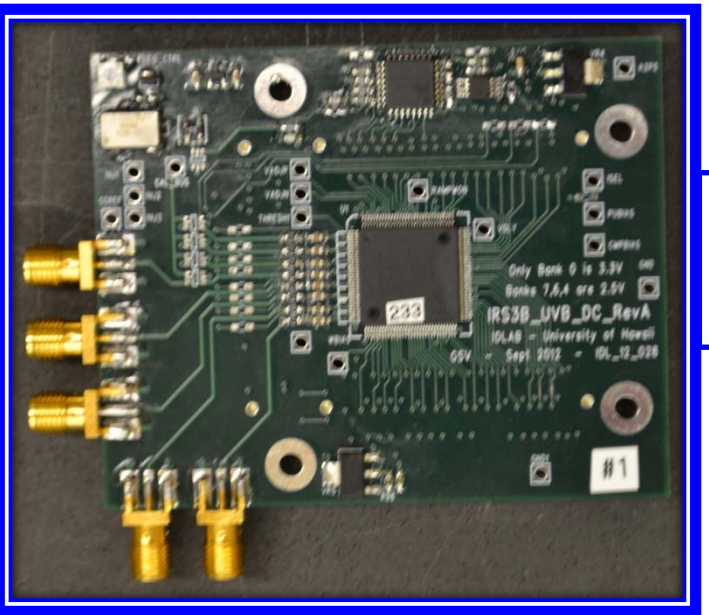
Firmware Development Status

Carrier 02 (top)

Interconnect Rev. A (mid)

SCROD A2 (bottom)



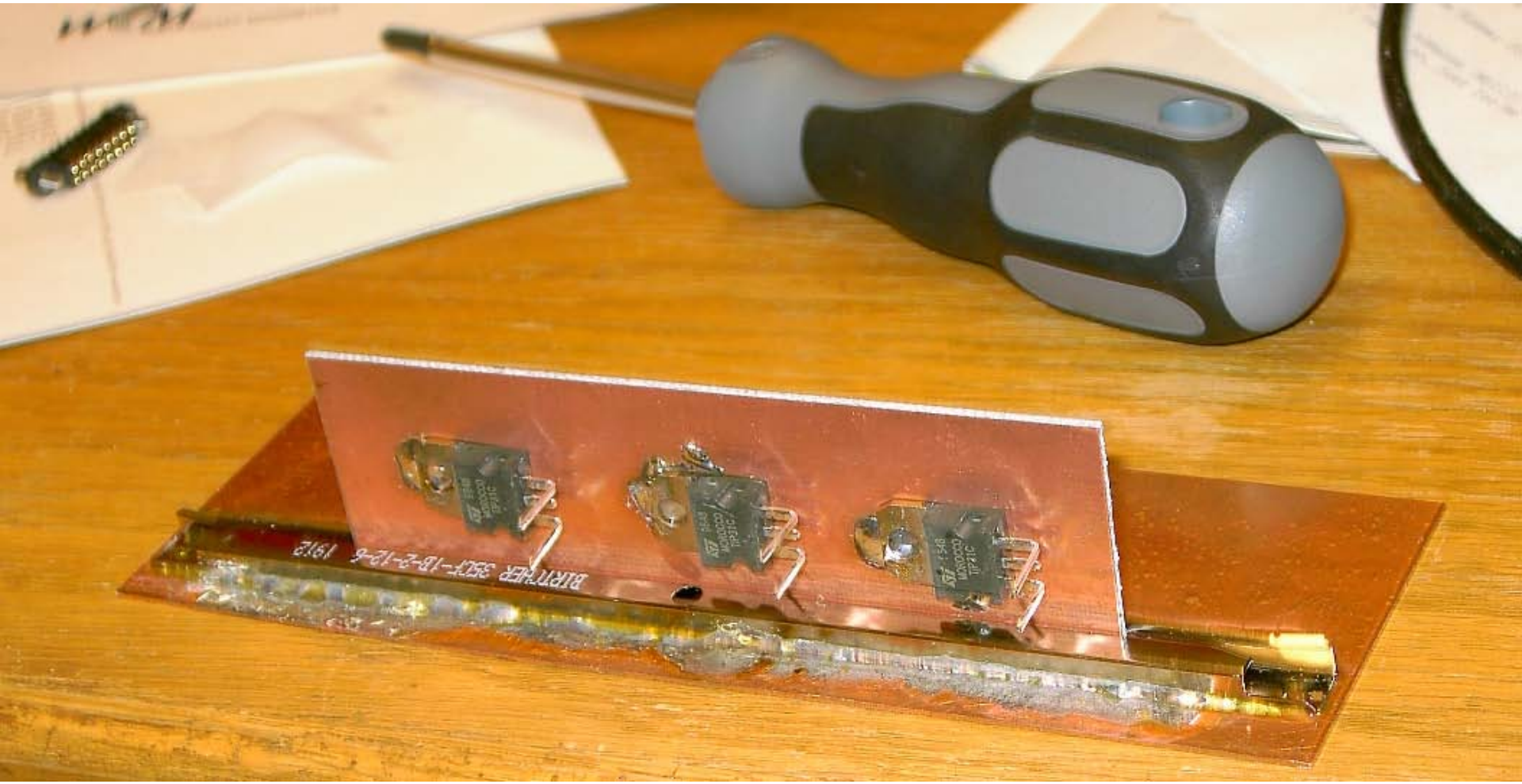


IRS3B firmware (Eval Board)

Firmware v.2 (ROI, full board-stack)

Firmware v.3 (IRS3B, ROI, full board-stack)

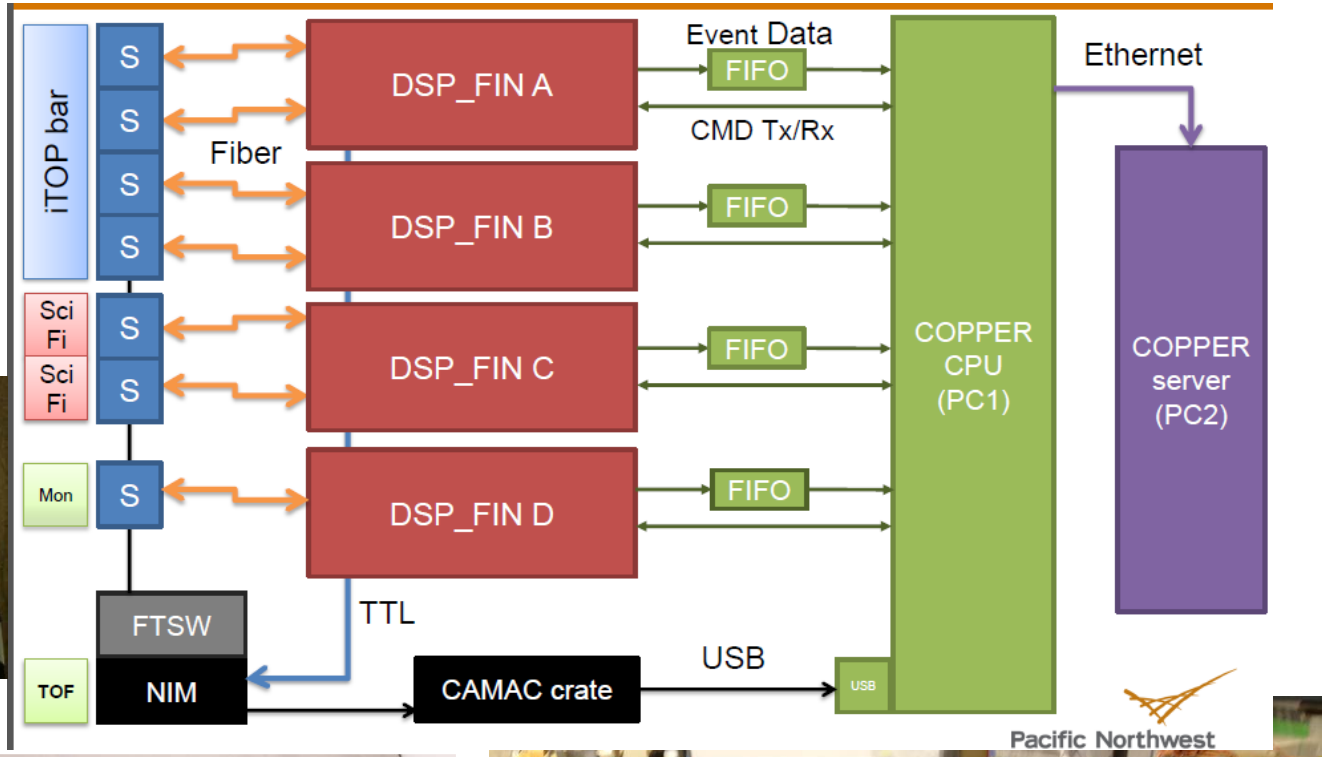
Further Improved Thermal



Standard wedge-locks too thick, but
some type of spring strip might work

4x modules
(512 channels)

Fuji Hall Backend Data Flow



Status of KEK-delivered Readout

- 62 of 64 IRS3B ASICs verified; all channel 1 see calibration input signal (1 AMUX problem? other is likely configuration debug). 512 channels of heat-sink packaged readout in Fuji Hall

- Having programmable control over fine timing adjusts permits automated scans of parameters

- A few minor issues with I^2C addressing and external DAC bypassing – all have straightforward, work-arounds