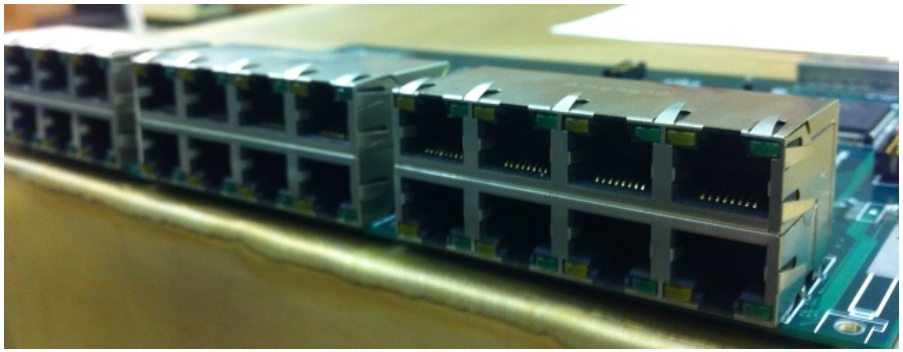


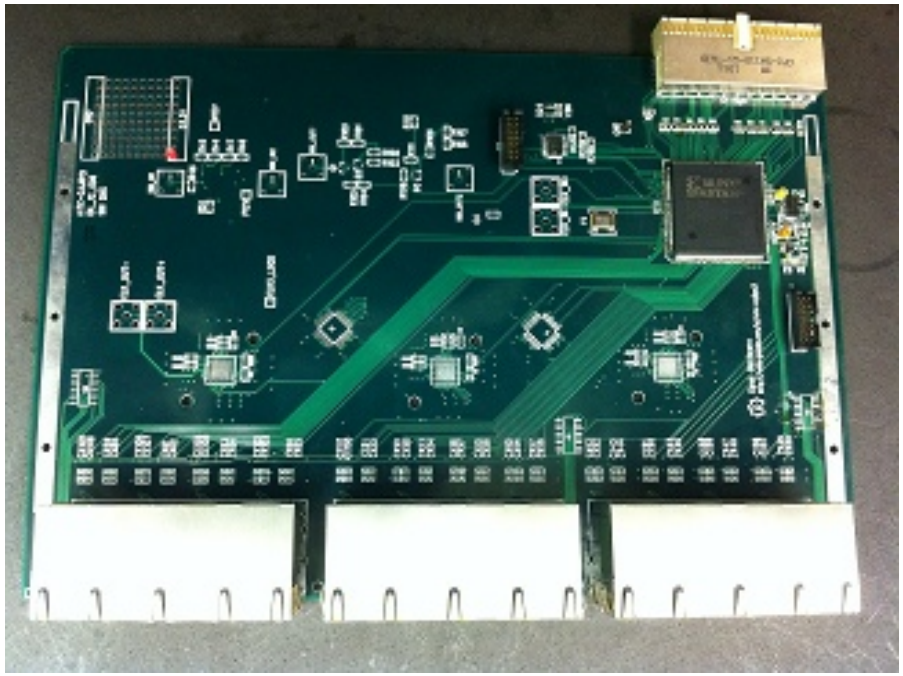
mTC-CAJIPCI

Sergey Negrashov, Stefanie Smith

Phys 476 - UH Manoa Physics department

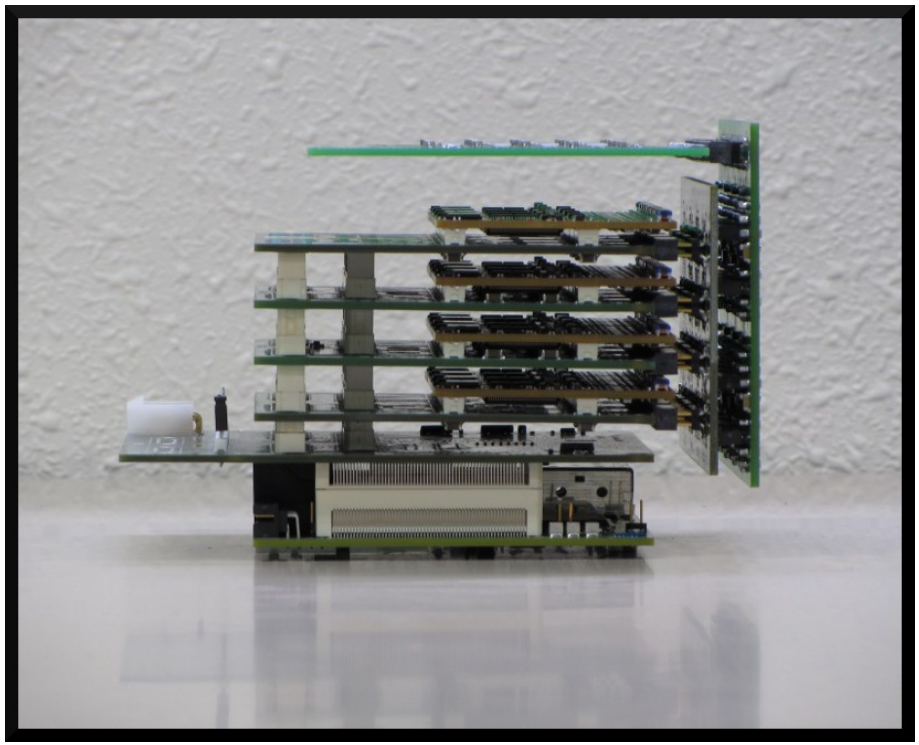
May 8, 2012

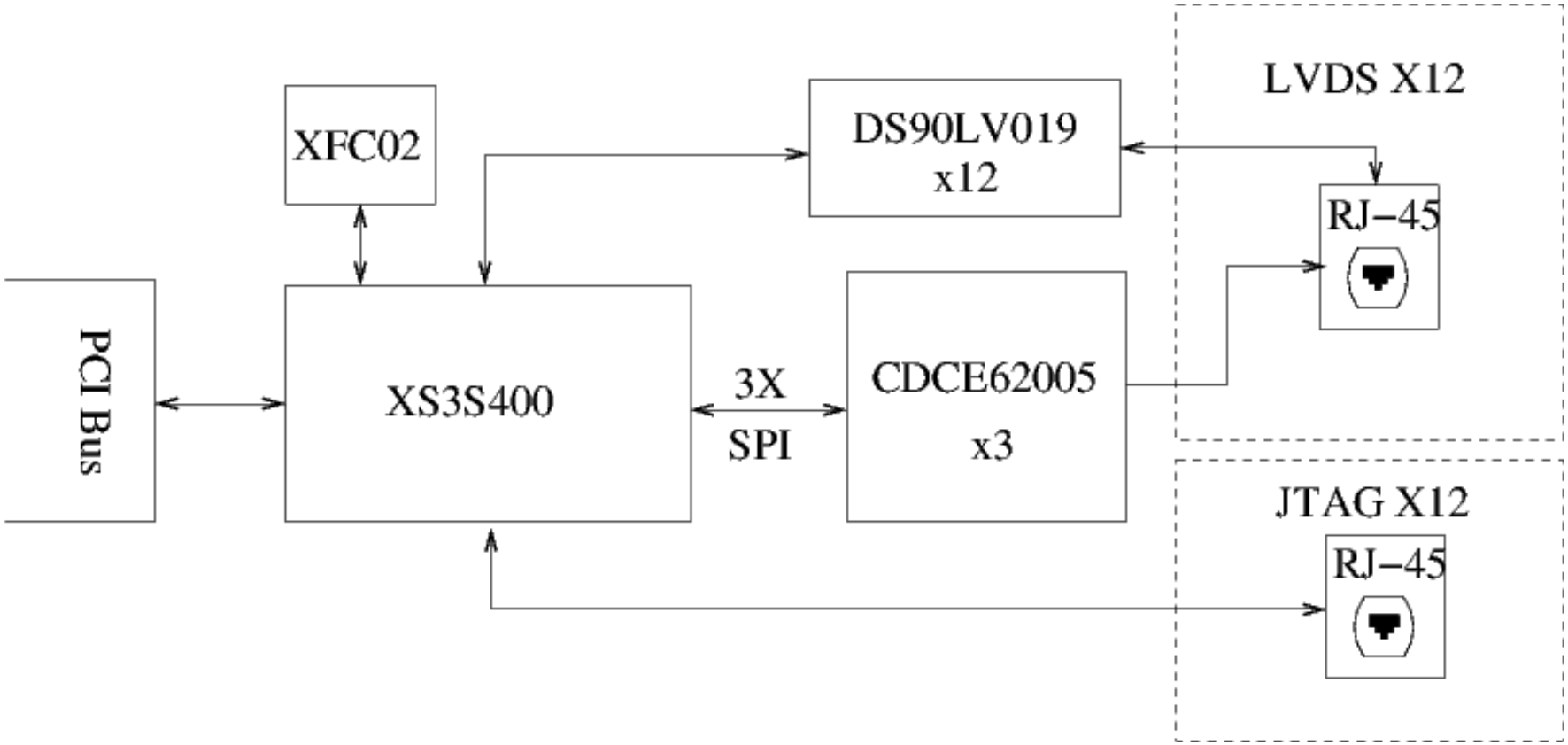
1. Motivation
2. Specifications
3. Board Layout
4. PLL
   - CDCE62005
   - Power Decoupling
   - Impedance Matching
   - Loop Filter
   - Stencil
5. Firmware



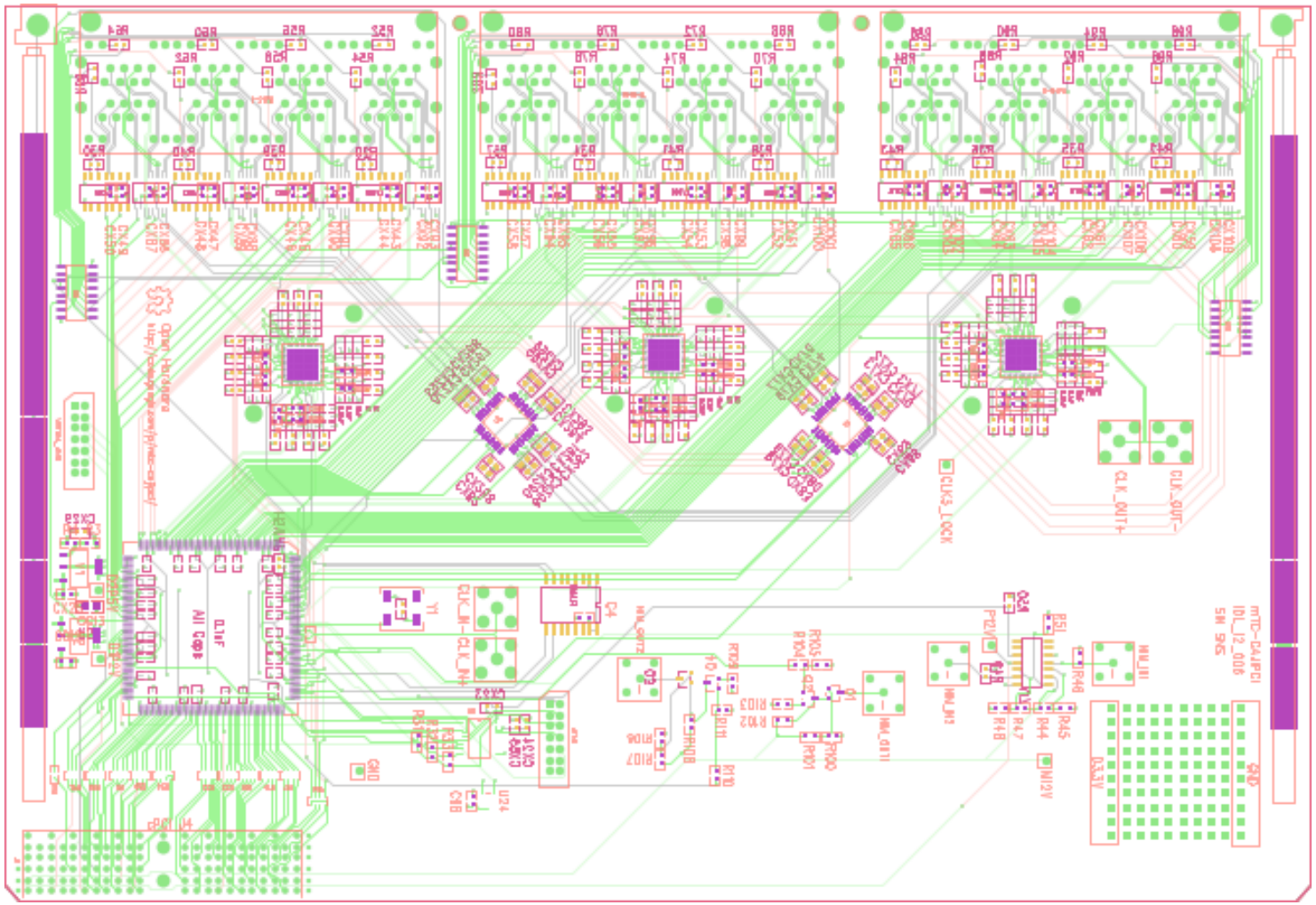
Motivation:

- Provide a sampling clock for the frontend.
- Simplify debugging of the frontend.
- Act as a level two trigger and allow for external trigger.

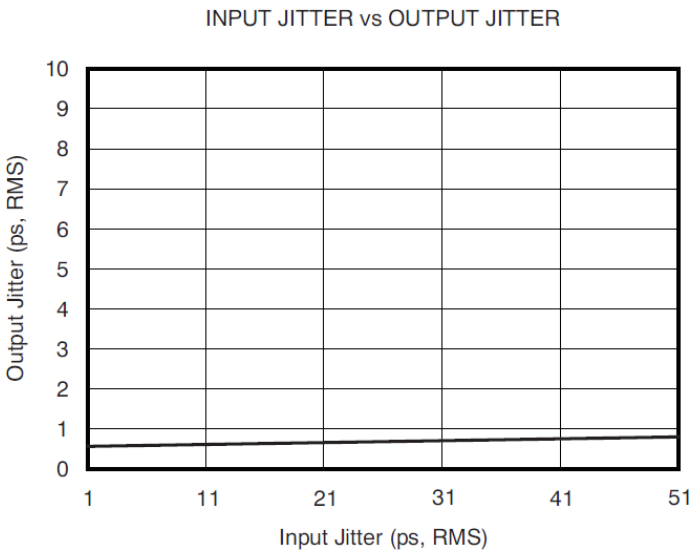




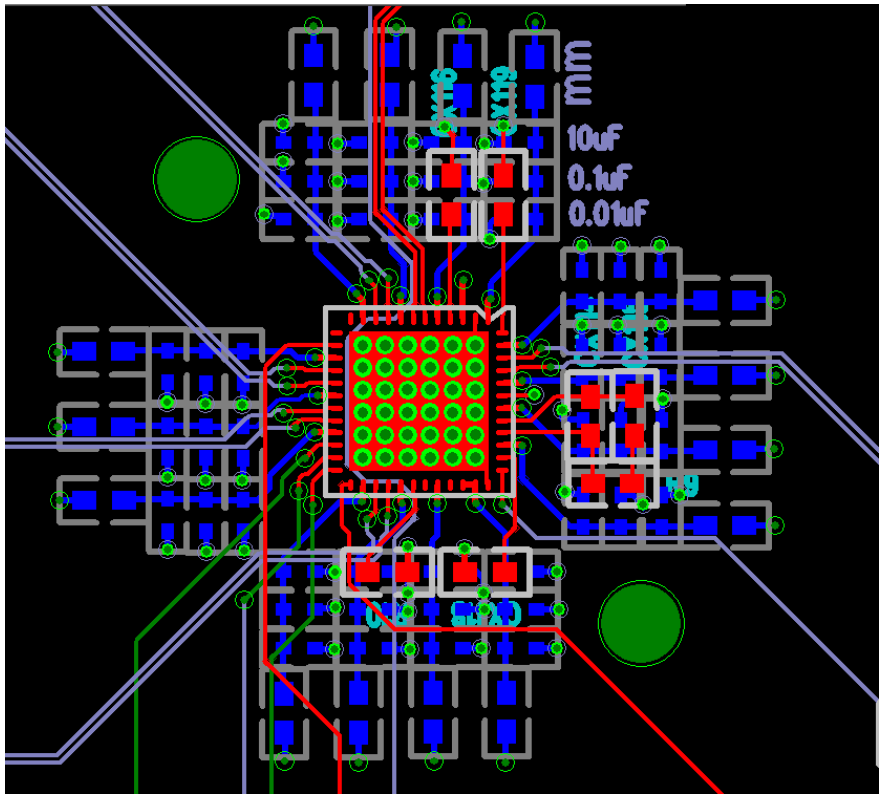
mTC-CAJIPCI Block Diagram.

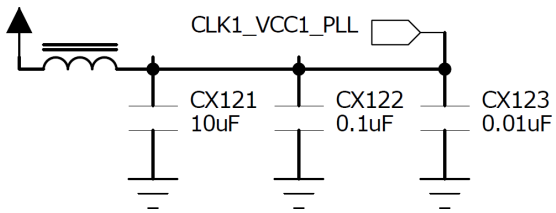


- 5 outputs, 2 inputs.
- up to 1.175 GHz output frequency.
- simple control via SPI bus.

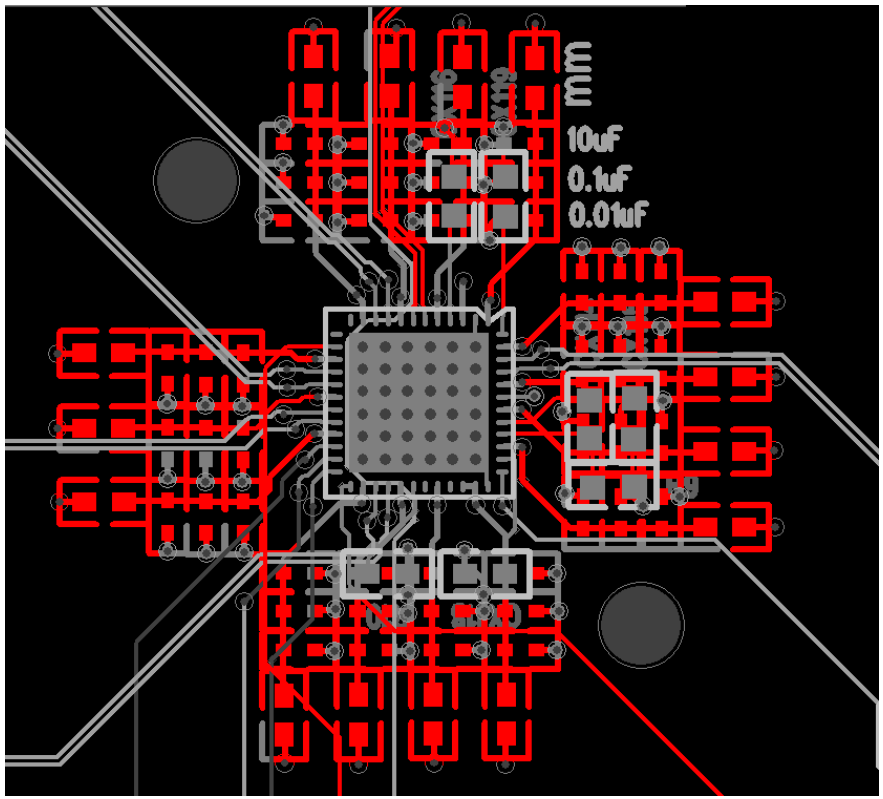


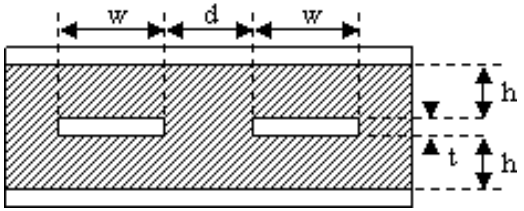
128Mhz HS-LCPECL Output





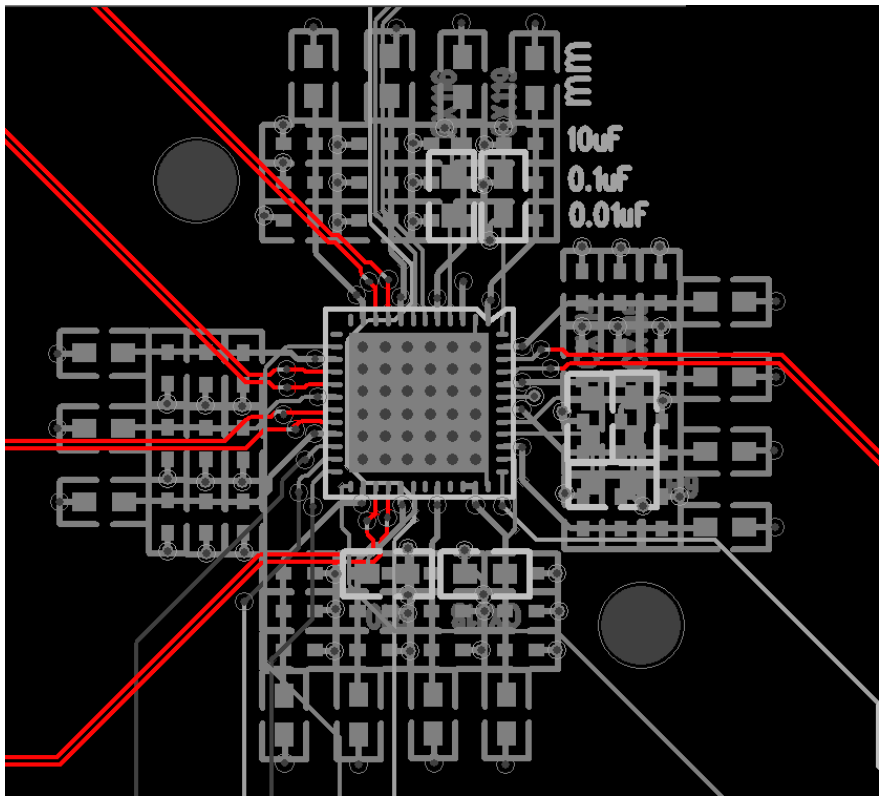
300 mA power draw per channel.

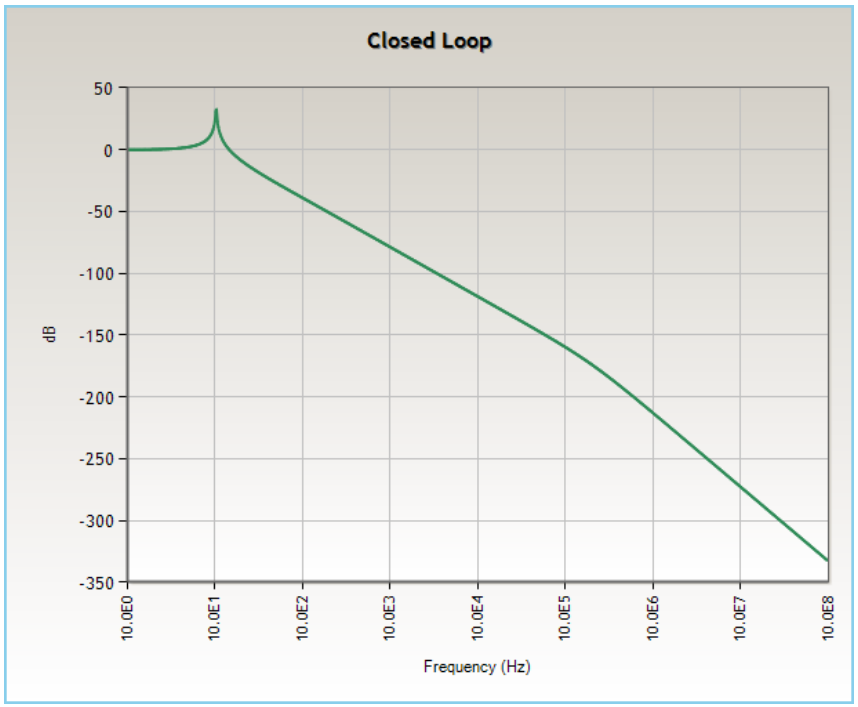




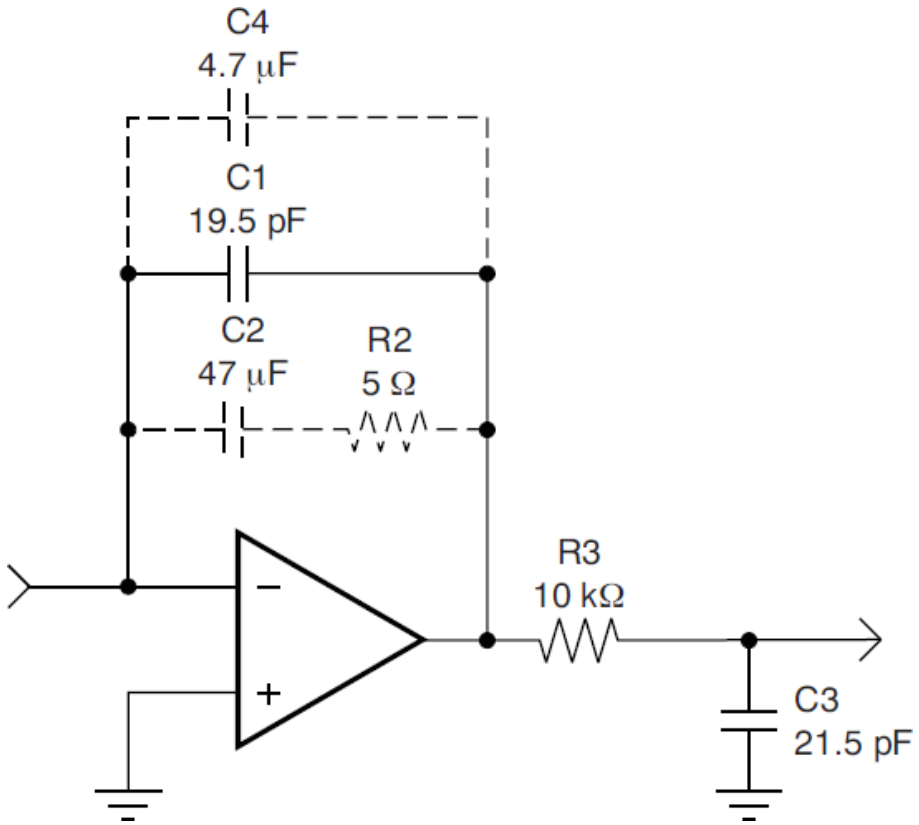
$$Z_d = \frac{120}{\sqrt{\varepsilon_r}} \ln\left(\frac{1.9(2h+t)}{(0.8w+t)}\right)\left(1-0.347\exp\left(-2.9\frac{d}{2h+t}\right)\right)$$

- FR4 insulator
- 1oz copper
- 6 mil trace and spacing
- *h=12 mil*

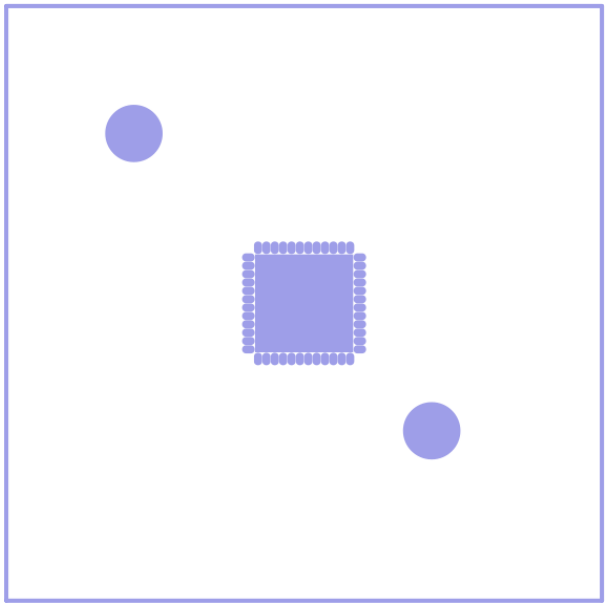


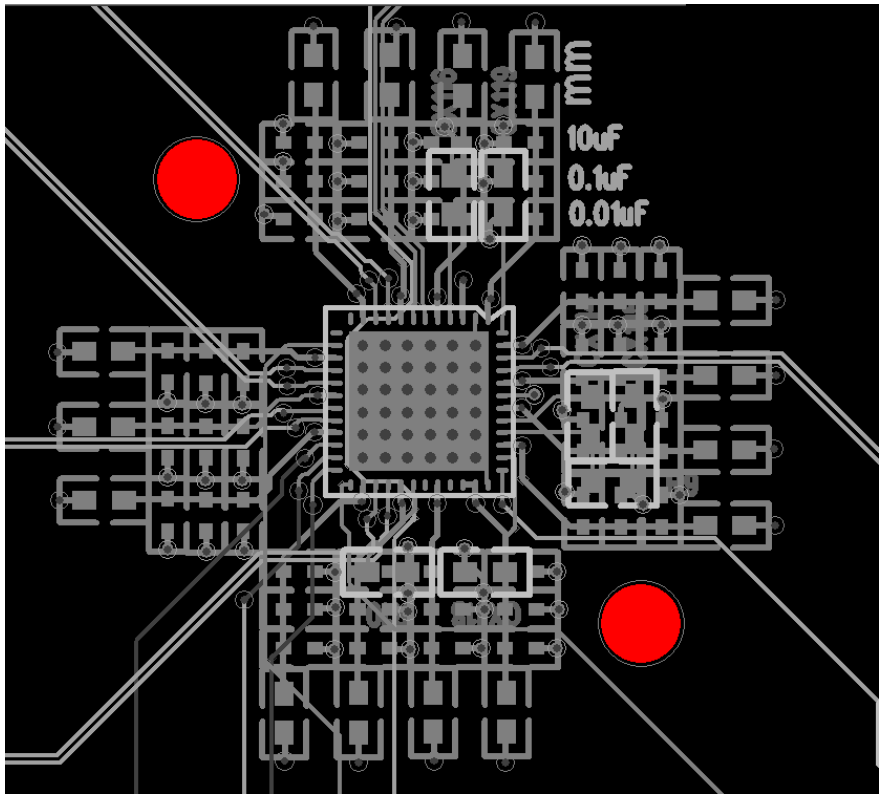


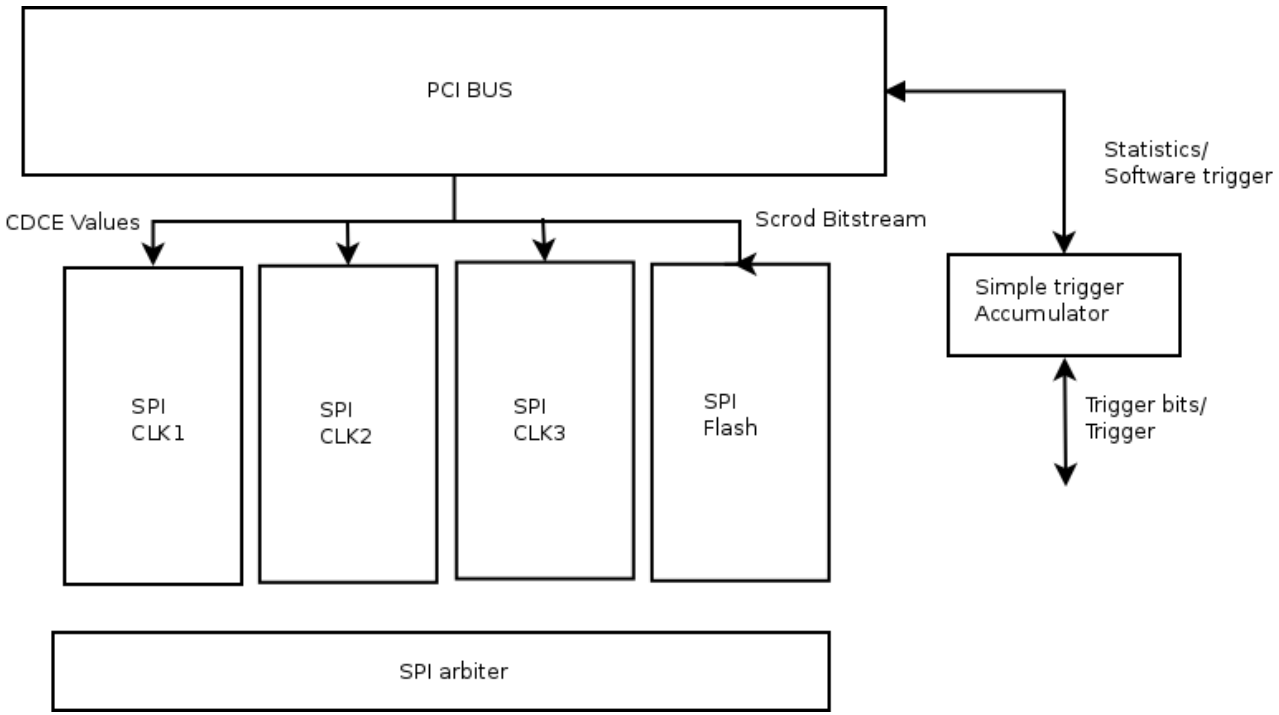
Closed loop filter responce.



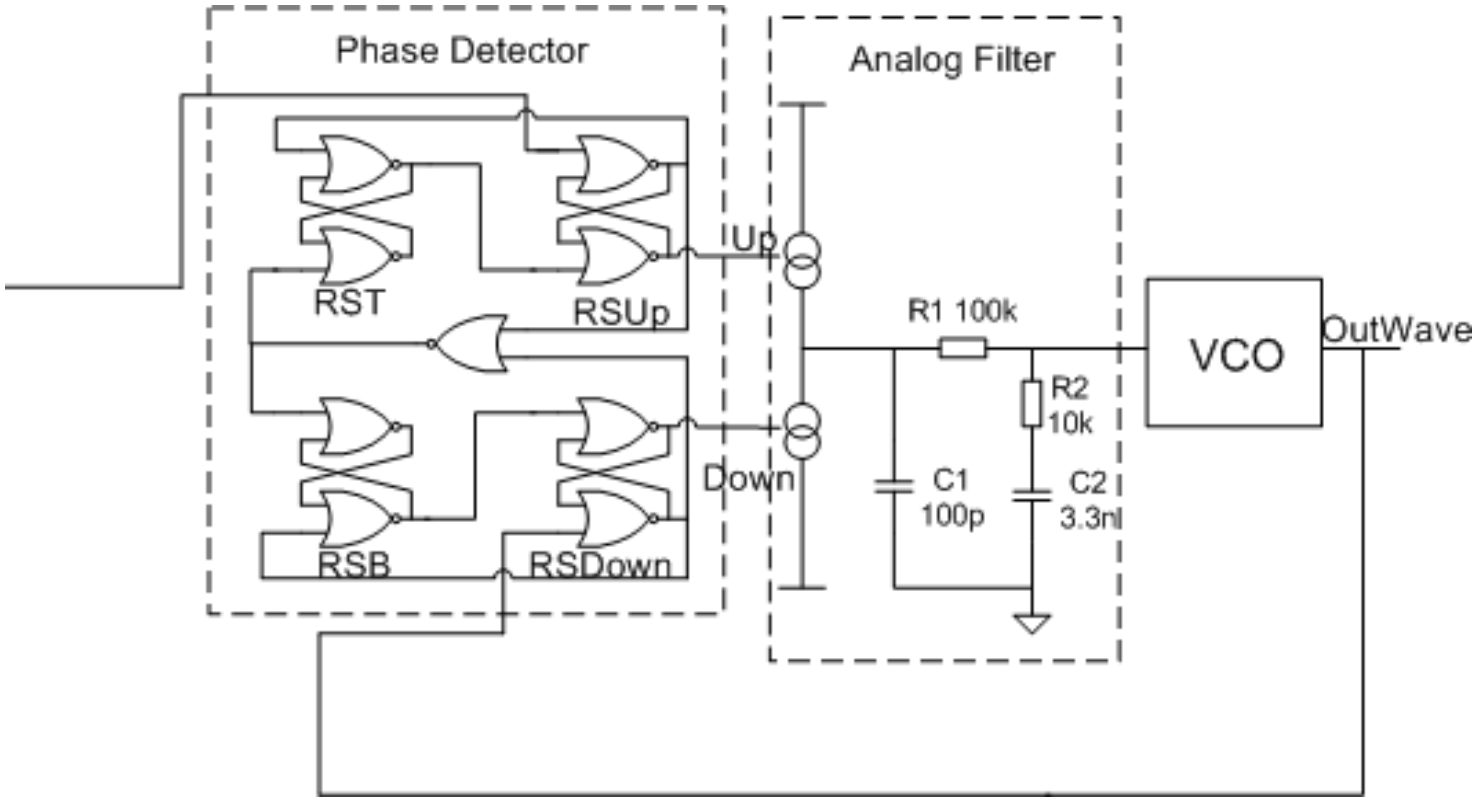
Dashed lines show external components.




mm
10uF
0.1uF
0.01uF


PCI BUS
Statistics/
Software trigger
CDCE Values
Scrod Bitstream
Simple trigger
Accumulator
SPI
CLK1
SPI
CLK2
SPI
CLK3
SPI
Flash
Trigger bits/
Trigger
SPI arbiter

Questions?


Phase Detector
Analog Filter
RST
RSUp
Up
Down
RSB
RSDown
R1 100k
R2
10k
C1
100p
C2
3.3nl
VCO
OutWave