IRS3 Daughter Card Evaluation System

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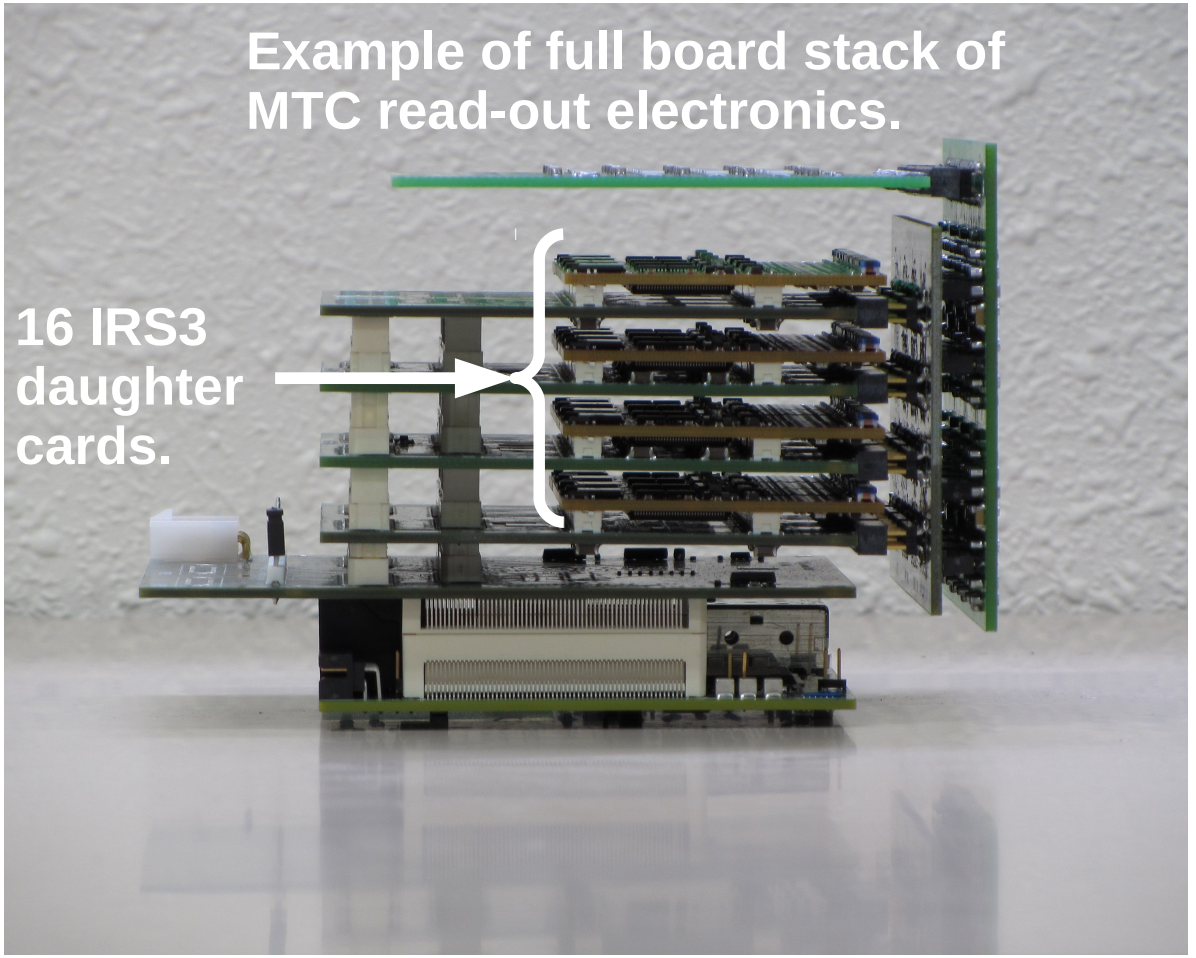
Introduction



Motivation: We want to evaluate and test each IRS3 Daughter Card in a simple and repeatable process before inserting them into full board stack.
→ Build evaluation system for IRS3 Daughter Cards using Universal Eval Board.

Current Issues and Status

- Univ Eval Board Fabrication not yet complete: FPGA, JTAG connector, LEDs.

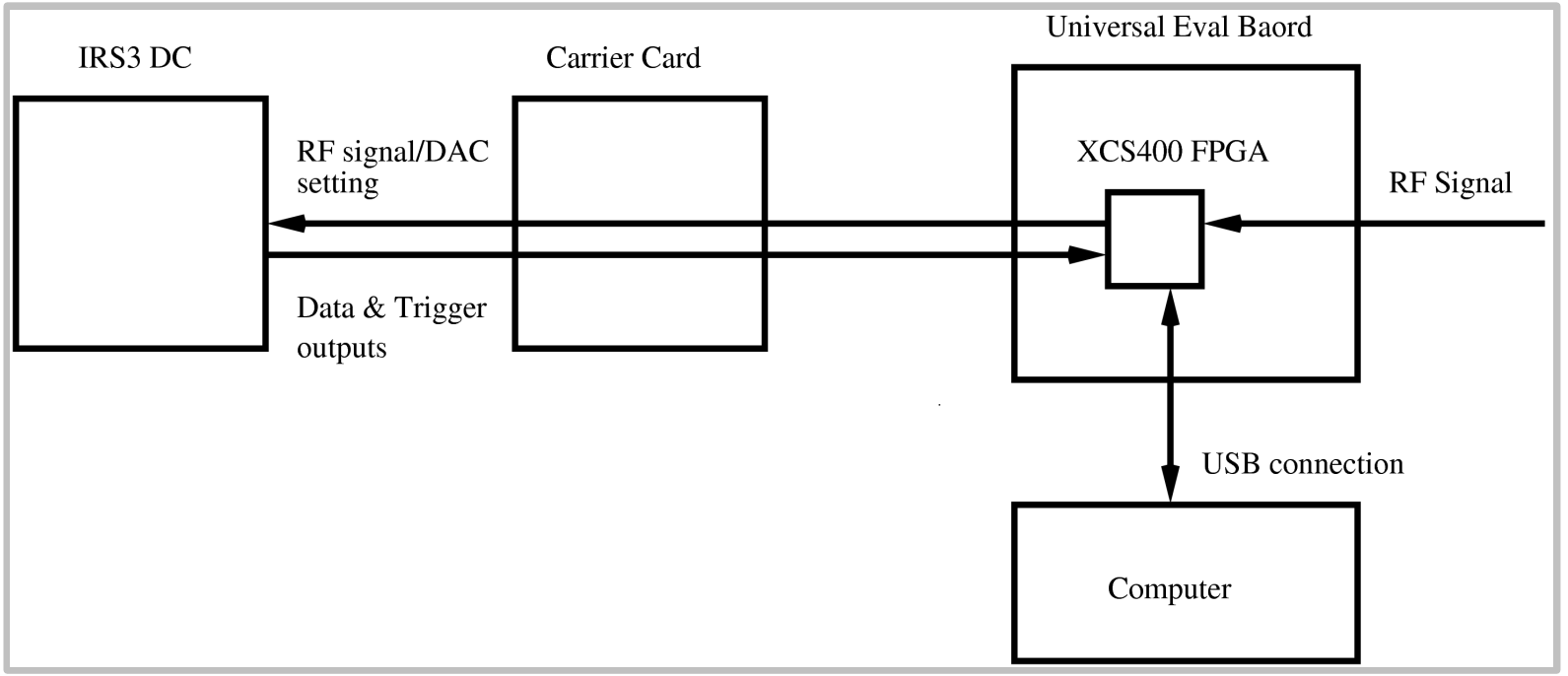
  → Parts have arrived.
- Waiting for DC Carrier Board.

  → Arrives next week.
- Firmware.

  → Will start testing using existing firmware after Univ Eval Board is fabricated.
- Must register Univ Eval board with IDL.

  → Will do this after this presentation.

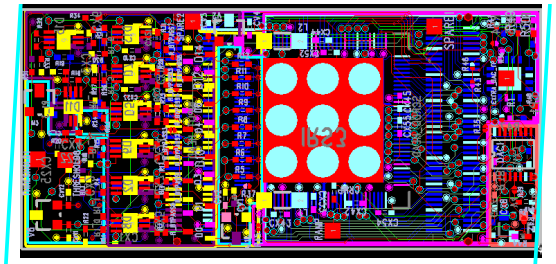
Block Diagram / Specifications

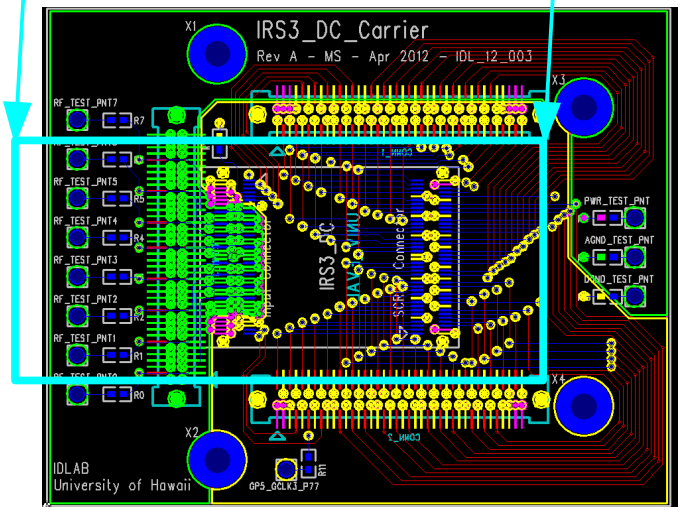


- IRS3 Daughter Card
  8 channel, < 20mW/Channel, 2~4GSa/sec, 100kHz read-out, storage array of 512 banks of 64 cells, Wilkinson Digitization (1kOhm TIA amp)
- Universal Eval Board
  XCS400 Spartan-3 FPGA

System Layout

IRS3 Daughter Card





Carrier Board

Univ. Eval Board