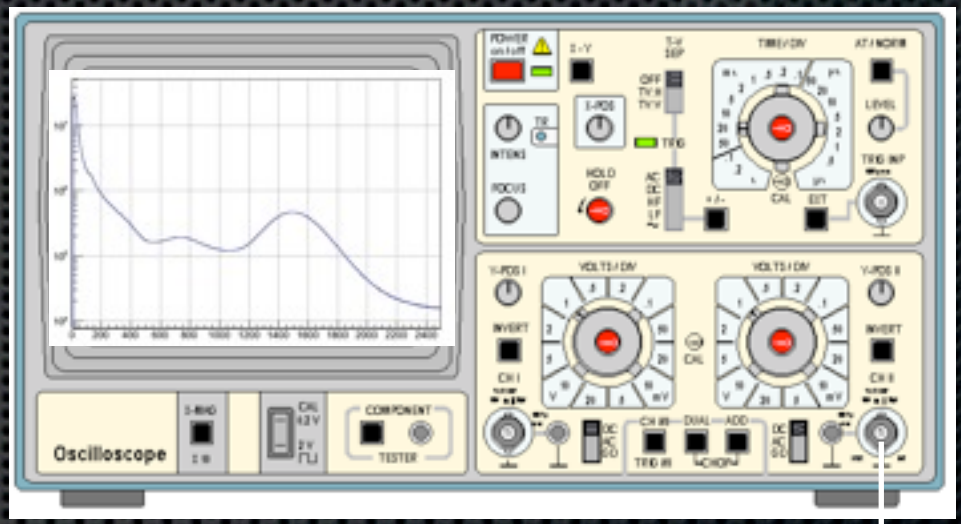
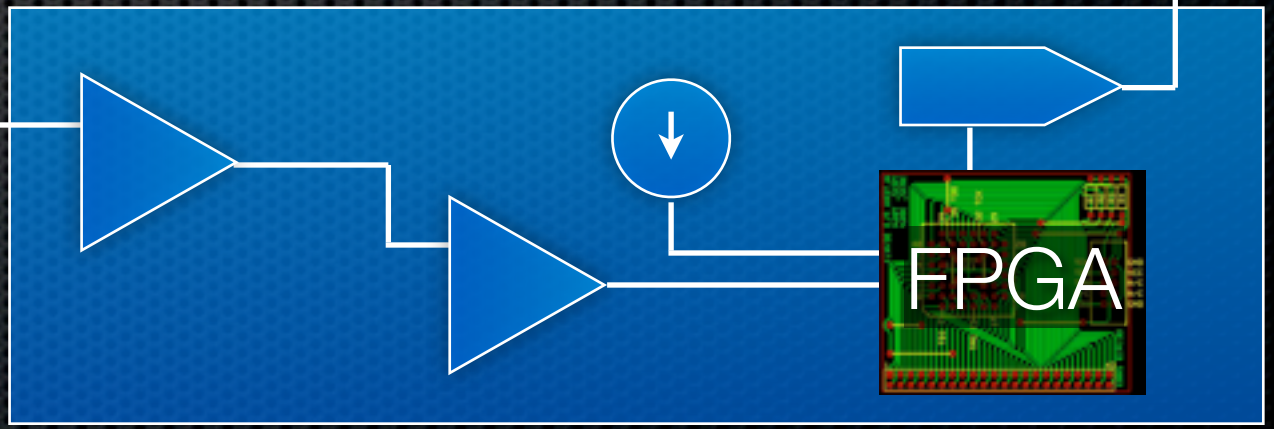
Energy Spectrum to Oscilloscope Project (e-STOP)

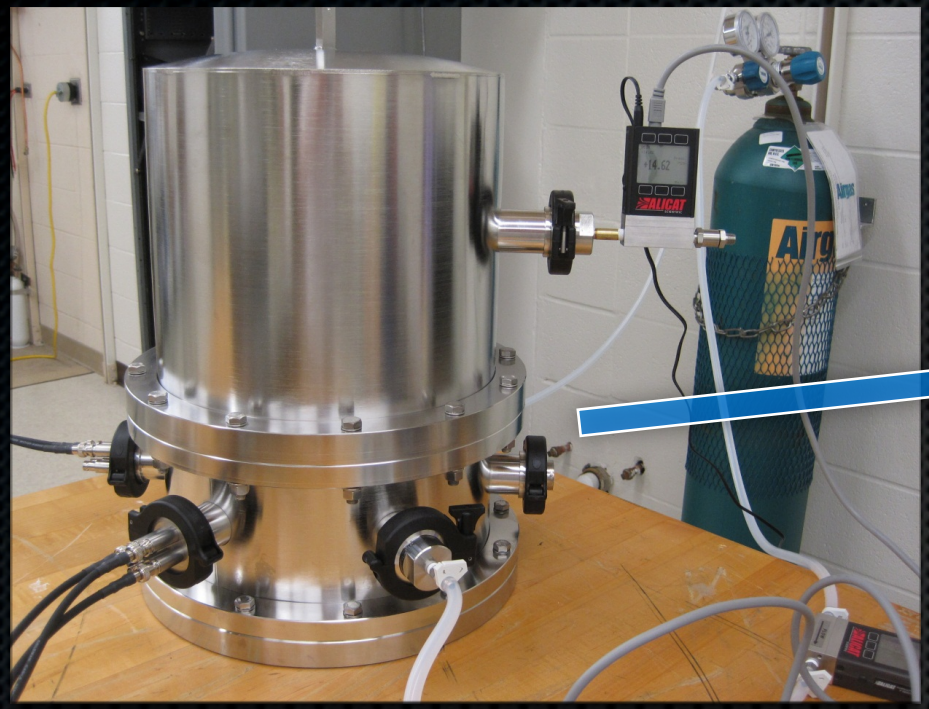
Igal Jaegle
Jared Yamaoka

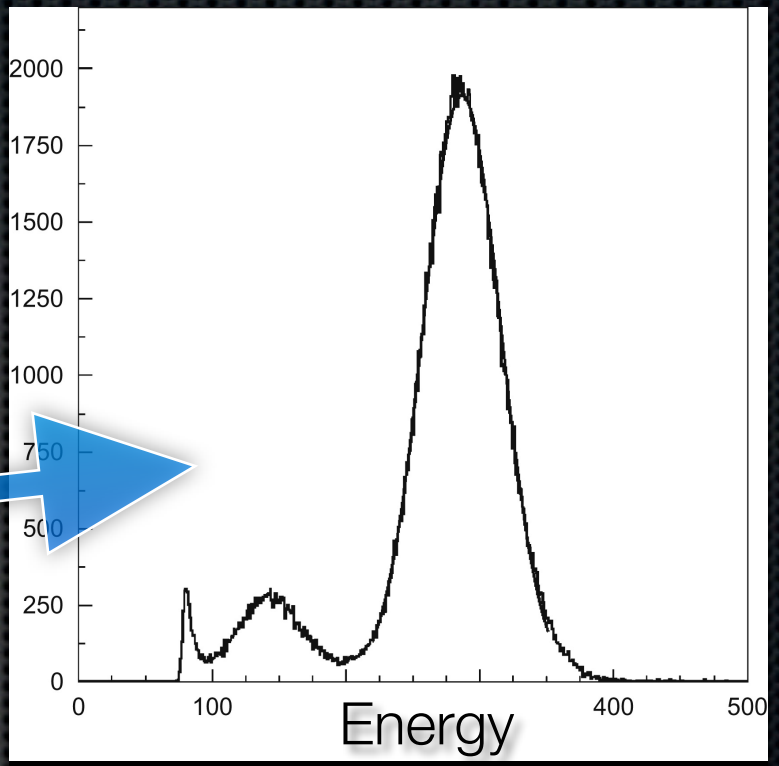




8 Dec. 2011

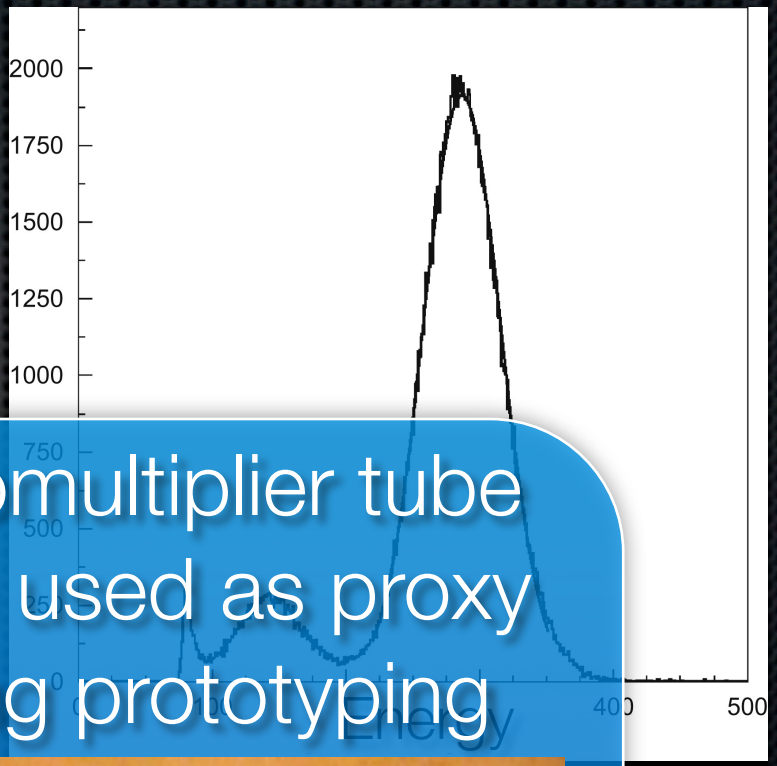
D^3 micro





- **Pulse hight spectrum** caused by radio active decays to **characterize detector** (pulse hight $\propto$ energy)
  - **Detector Gain**
  - **Energy Resolution**
- Move from commercial to **custom (e-STOP) system**.
  - PC free system

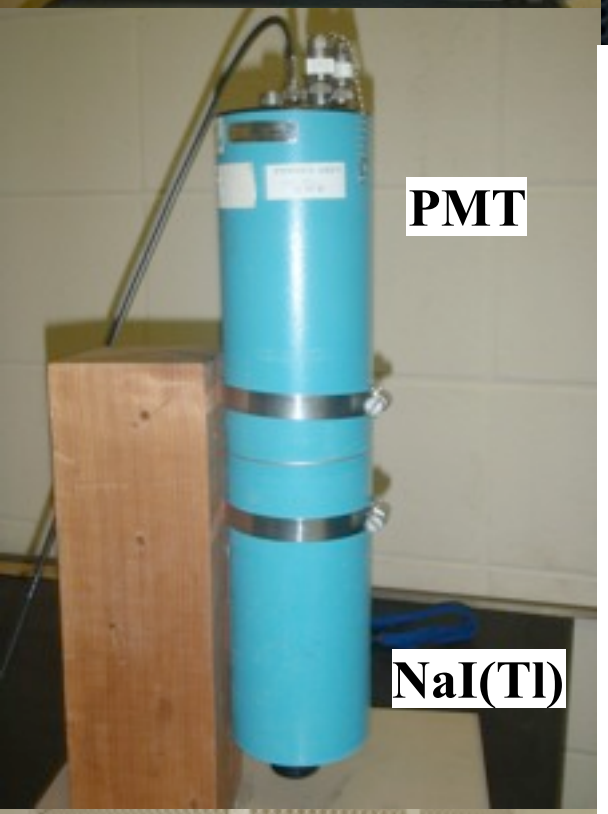
D^3 micro

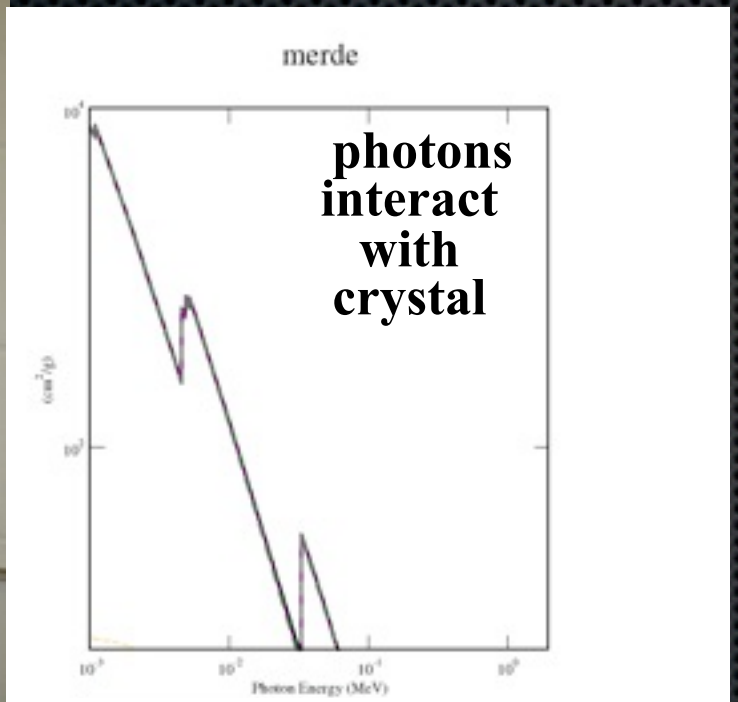


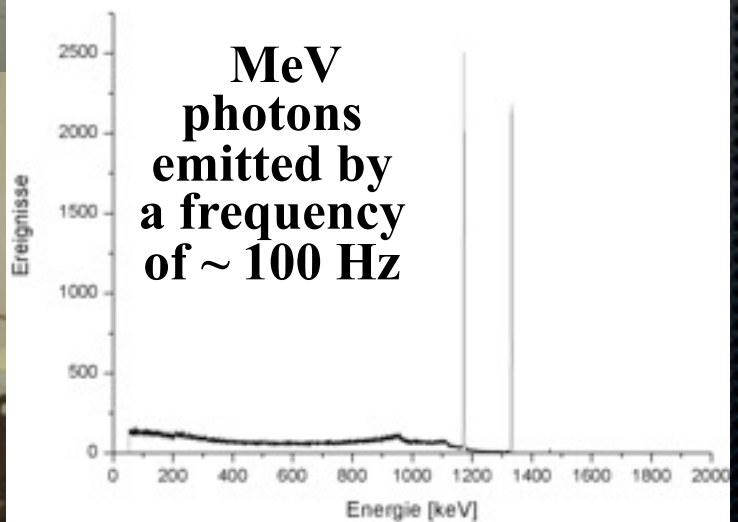
Photomultiplier tube (PMT) used as proxy during prototyping

- **Pulse hight spectrum** c ays to **characterize detecto** (p
  - **Detector Gain**
  - **Energy Resolution**
- Move from commercial to m.
  - PC free system

Detector





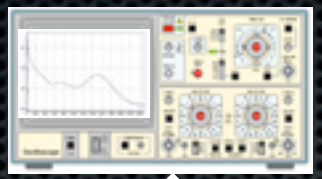


- eV photons collected by a photon convertor with a certain QE
- electron signal amplify by 10's of 1000 times

Specification

- Scintillator Info: NaI(Tl)
  - Pulse width **~1 μs**
- Amplify the **PMT output**
  - Photon eff.
  - PMT Pulse Height **~400 mV**
  - Digitize voltage **~10 V**
- **Event Rate: ~100 Hz**
- **Desired energy resolution < 10%**

Components



Amp

Sample /Hold

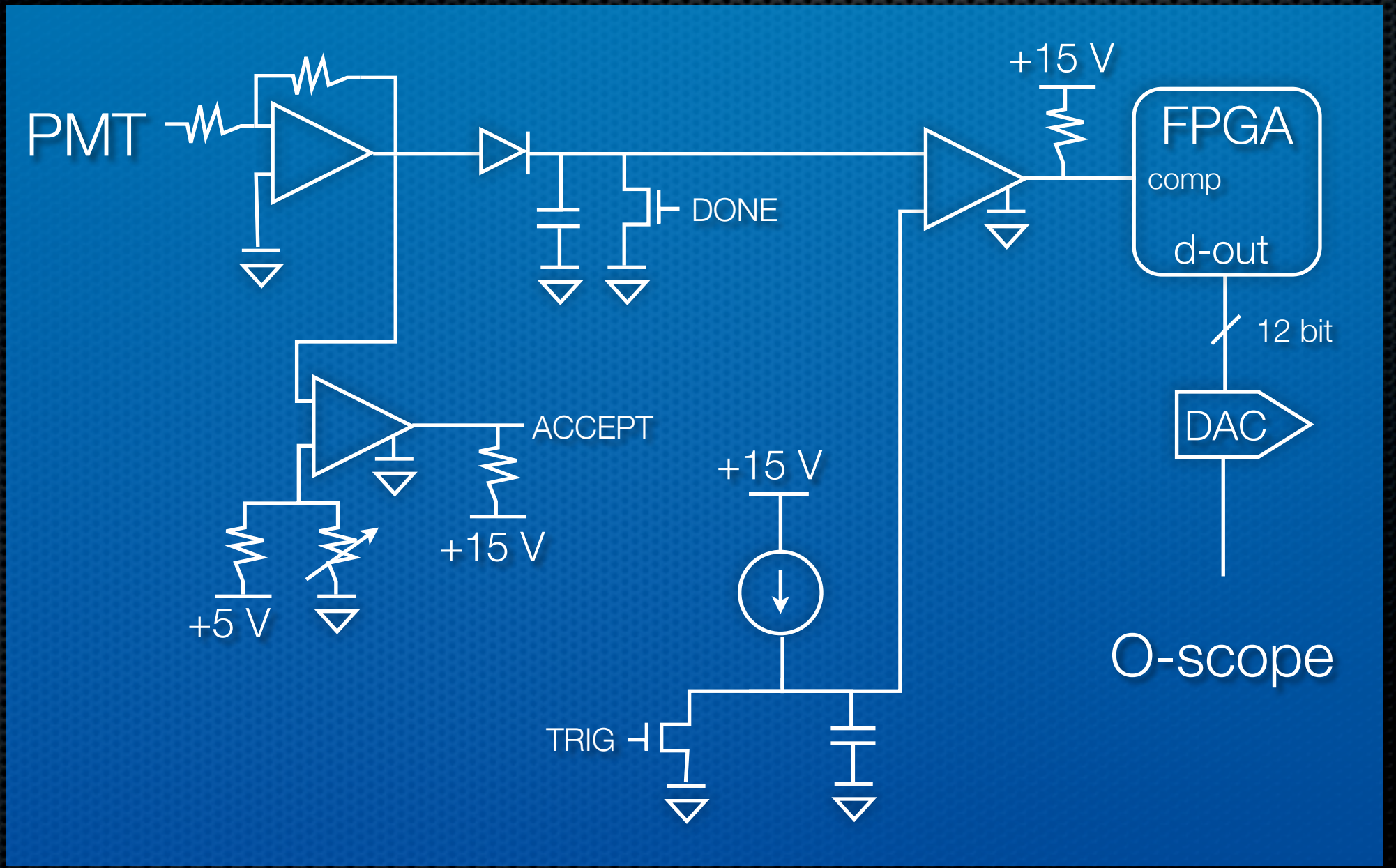
Volt. Ramp

DAC

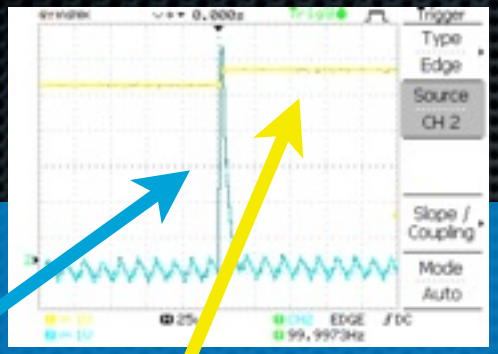
FPGA

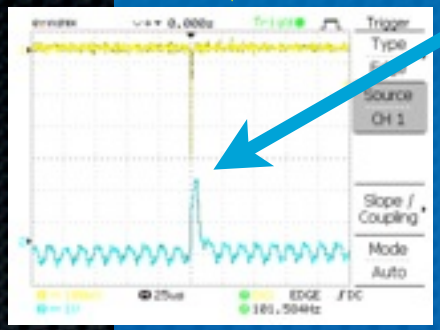
- **Wilkinson ADC (12 bit)**
  - S/H stores the **peak value of pulse**.
  - Ramp time counted with FPGA clock
- **Hardware Histogram (12 bit)**
  - Each ADC value mapped to one memory address. (ie **Each memory address is one "bin"** and its value is incremented for each instance.)
- **Read out** all addresses **periodically** to DAC.

Schematic


PMT
DONE
+15 V
FPGA
comp
d-out
12 bit
DAC
O-scope
ACCEPT
+15 V
+5 V
+15 V
TRIG

Schematic





PMT

DONE

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FPGA

comp

d-out

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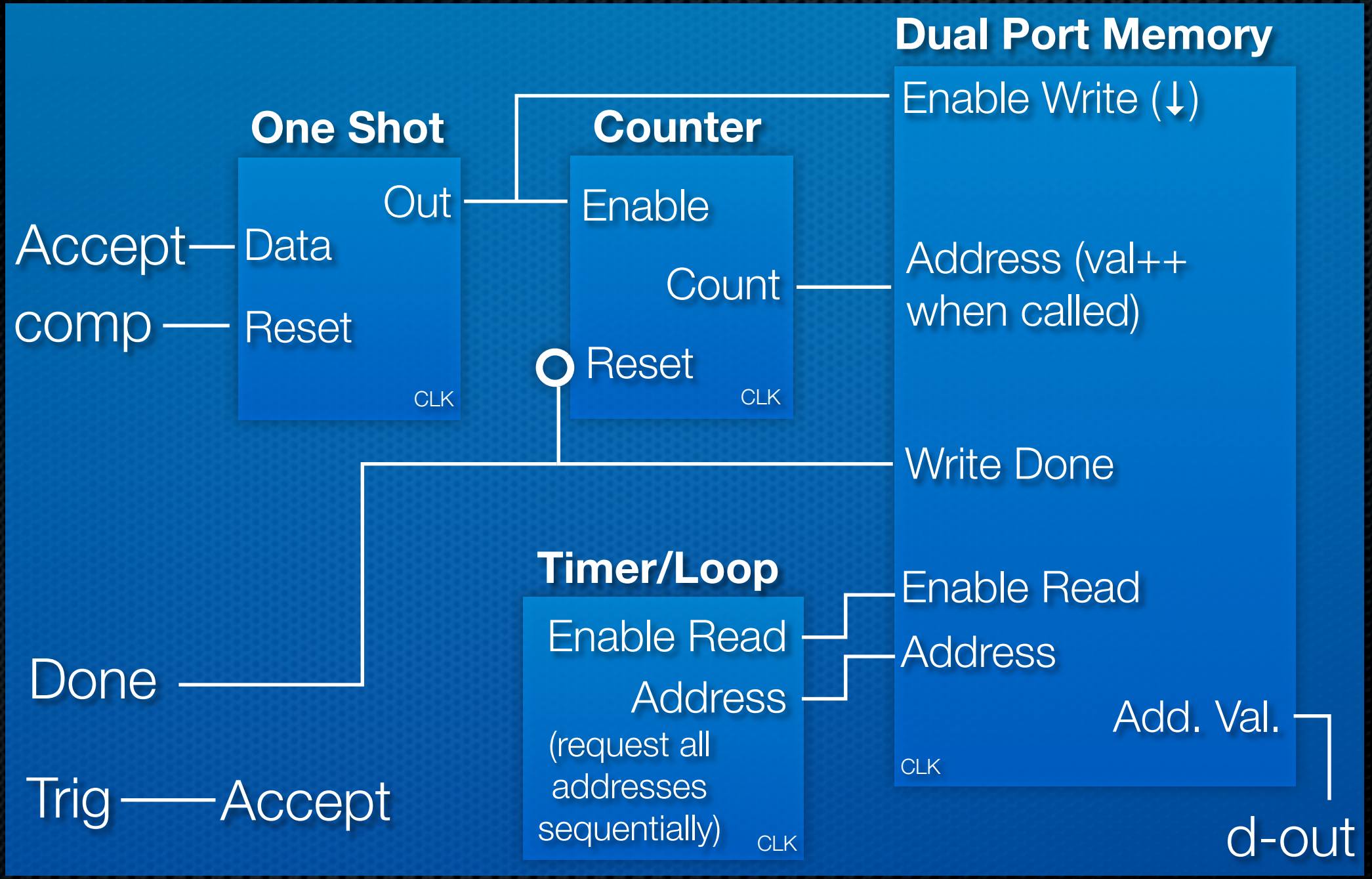
FPGA


Dual Port Memory
Enable Write (↓)
One Shot
Out
Accept
Data
comp
Reset
CLK
Counter
Enable
Count
Reset
CLK
Address (val++ when called)
Write Done
Timer/Loop
Enable Read
Address
(request all addresses sequentially)
CLK
Enable Read
Address
Add. Val.
CLK
Done
Trig
Accept
d-out

Summary

- Cool project, learned a lot
- Analog part works fine.
- FPGA firmware still needs work
- Need to implement DAC/Oscilloscope.
- Finish Soon.