BLAB3A Trigger Evaluation for Mini Time Cube

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December 9, 2011

Abstract

This document outlines the first evaluation of the self-triggering mechanism of the 3rd generation Buffered Large Analog Bandwidth Recorder And Digitizer with Ordered Readout (BLAB3A) Application Specific Integrated Circuit (ASIC). A mock photomultiplier tube pulse signal was used to test the trigger of a single channel of the BLAB3A.

Motivation

The authors of this report are currently working on a project to build a portable neutrino detector named the Mini-Time Cube (MTC) [1]. We are interested in the self-triggering and digitization capabilities of the BLAB3A because it is our candidate front-end read-out electronics for the Planacon multi-channel plate (MCP) photomultiplier tubes employed in the MTC design [1].

The MTC consists of a solid block of scintillating plastic doped with 5% natural boron. The dimensions of the scintillating block is a cube with all edges being 13cm in length. The polymer base of the plastic is polyvinyltoluene. Fig. 1 shows the process of inverse beta-decay where an incoming neutrino induces a positron and a neutron to be produced in a pair. The positron immediately annihilates with an electron in the medium while the neutron undergoes a thermalization process in which it loses most of its kinetic energy to eventually be captured on a proton or some sort of neutron capturing dopant material mixed into the detector material. Approximately 19.9% of the natural boron employed in the MTC is boron 10 and this particular isotope gives us a high cross-section for neutron capture. Neutron capture is an important feature of this detector because we hope to distinguish the direction from which the neutrino came from before the thermalizing neutron looses too much of its directional information by capturing the neutron as fast as possible.

The MTC uses a total of 24 MCP's where each set of 4 MCP's are placed on a single face of the scintillating cube. Each BLAB3A module will serve as the read-out electronics for one pair of MCP's (Fig. 2).

Fig. 3 shows a couple of sample images of the MCP photomultiplier tubes that are currently ready to be deployed. The photosensitive surface is composed of an array of 8×8 photocathode pixels. The back-end of the photomultipliers have several arrays of output pins that each have a maximum current output of 3μA.

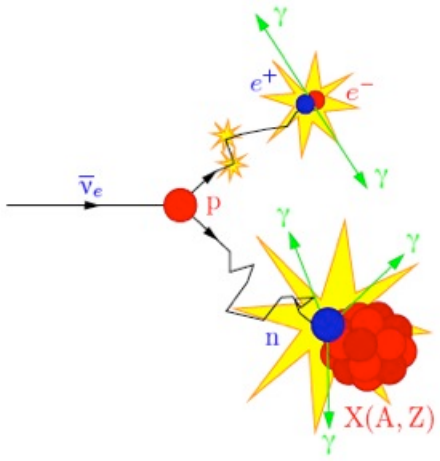


Figure 1: *Diagram of the inverse-beta decay process that is used for neutrino detection by the Mini-Time Cube. When an incoming electron anti-neutrino undergoes charged current interaction with a proton in the medium, a positron and a neutron is produced. The positron immediately annihilates with an electron in the medium releasing two back-to-back gammas of 0.911 MeV each. The neutron gets "captured" on a proton or some other neutron capturing dopant material after some characteristic thermalization time on the order of several $\mu s \sim 100 \mu s$. The neutron capture process also releases some energy and gammas. [2]*

1 BLAB3A and Self-Triggering

The 3rd generation Buffered Large Analog Bandwidth Recorder And Digitizer with Ordered Readout (BLAB3A) Application Specific Integrated Circuit (ASIC) is a low-power, O(10 picoseconds) timing resolution, 10-bit waveform recorder and digitizer for reading out a 16-anode array of the Hamamatsu Micro-Channel Plate (MCP) Photomultiplier [3]. The BLAB3A is intended for detector applications which require data sampling rates of around 2∼4 Giga-samples per second (GSa/s).

Figure 4 shows a block diagram of the BLAB3A ASIC. Dedicated discriminators on each input channel provide a triggered readout rate of up to 100kHz. Each channel can store samples in 512 banks of 64 storage cells. It has a fast data conversion rate of $< 2\mu s/512$ samples and random access to the individually stored samples is possible, as well as having multi-hit buffering capability. The input sampling is done in a "ping-pong" style mechanism where a set of 64 samples are acquired while another set of 64 samples are transfered to the storage array.

Figure 5 shows a schematic drawing of the self-triggering system of the BLAB3A. There are four DAC parameters that can be set arbitrarily to control the triggering properties. These are TGRthresh, TRGbias, SGN, Wbias. Currently on the BLAB3A the trigger threshold is set globally and so there is only one threshold value for all 8

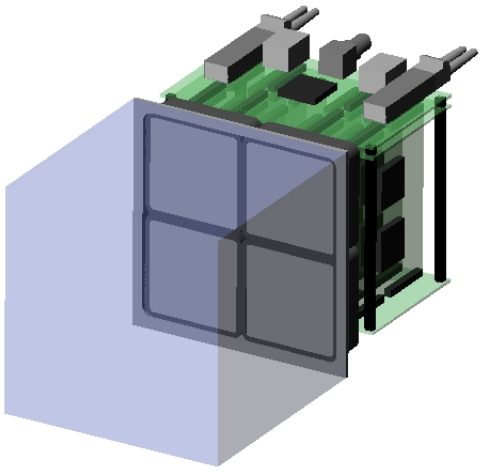


Figure 2: *This diagram shows a CAD rendering of the Mini-Time Cube neutrino detector. A 13 cm plastic scintillating cube is surrounded by 24 Micro-Channel Plate photomultiplier tubes that are sensitive to photons that are produced by the scintillating material. Only one of the six sides are populated in this figure for better visualization.*

channels. The TRGbias is a bias current to set the Comparator. SGN is the bit used to set whether the trigger will register on a down going signal edge or an up going signal edge. Wbias is a signal used to determine the width of the 1-shot that comes from a successful trigger.

Results

We were successful in seeing the first trigger pulses from a single channel of the BLAB3A. The mock signal used for testing purposes was created using square waves from a function generator and sending them through a differentiator. The mock pulse was oriented to be negative and was measured to have a magnitude of 20mV with a width of 50-100ns. The pulse was generated at a frequency of 1Hz.

We used the Chipscope analysis tool from Xilinx [5] to instantiate virtual input/output (VIO) cores in the FPGA firmware of the Standard Control Read-Out, Data (SCROD) board [3] and set it to sample the trigger pulse at 80Hz. Although this is a relatively slow clock speed, this speed was only chosen for initial testing purposes and will be updated to a more reasonable and faster clock speed that will more or less simulate the MCP signals in the near future.

We were successfully able identify the particular carrier board, the daughter-card

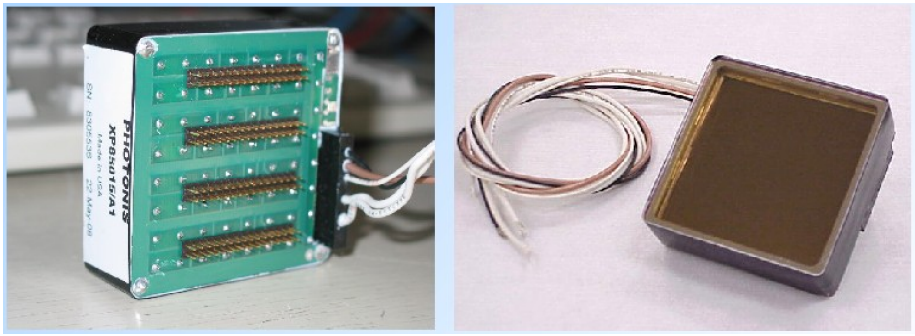


Figure 3: *Sample picture of the Planacon Micro-Channel Plate photomultiplier tubes manufactured by Burle Industries. The right hand image shows the photo-sensitive surface which consists of an 8×8 array of pixels. The left-hand image shows the back side of the module where an array of anode output pins. Each pin outputs a nominal maximum current of* $3\mu A$.

slot of the board stack, and the channel number in the firmware, and adjust the various trigger DAC values with the chipscope tool. Our next immediate task is to do a threshold scan on the channel so that we can gain a better understanding of the noise levels for the input signal.

Summary and Outlook

We were successful in our first test of the self-triggering mechanism of the BLAB3A with a mock MCP signals pulse created in the laboratory. The FPGA firmware for the SCROD board was studied and modified to achieve this result. Also we were able to understand the and operate the ISE Chipscope analysis tool to build our own FPGA cores and monitor the trigger signals from the BLAB3A. Also we were successful in varying the various DAC parameters that control the self-triggering mechanism.

This initial self-trigger testing of the BLAB3A was not conclusive nor thorough enough to fully prepare the BLAB3A readout module for the MTC. However we hope that the knowledge and experience gained through this endeavor will be helpful in further investigation.

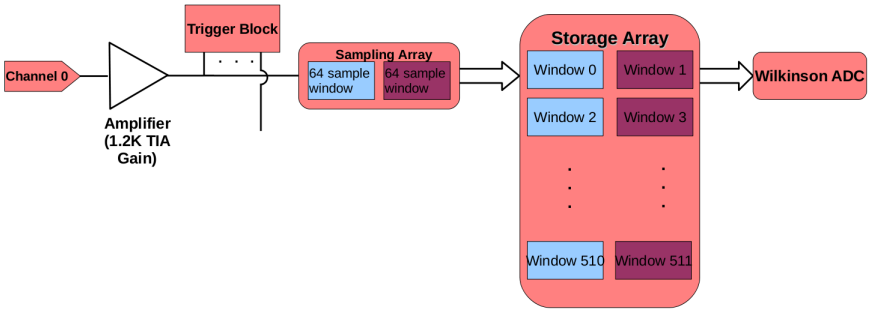
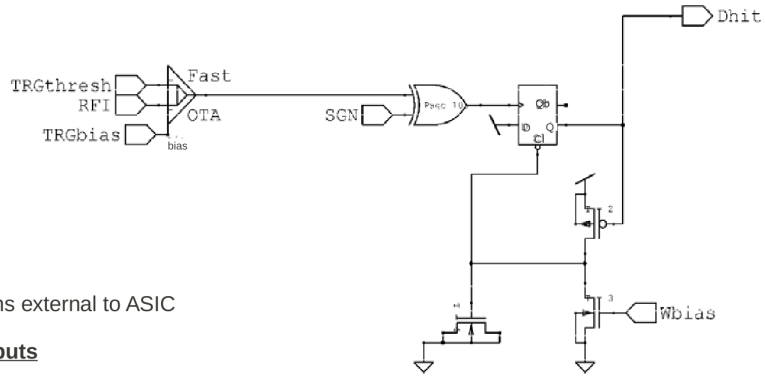


Figure 4: *BLAB3A ASIC block diagram. A total of 8 signal channels are present on a single BLAB3A ASIC. Each signal is sent through a Trans-Impedance Amplifier (TIA) such as the one depicted in this figure and sent to a sampling array of two 64-bit deep sampling windows. The input sampling is done in a "ping-pong" style mechanism where 64 samples are acquired while another 64 samples are transfered to a storage array of 512×64 cells.*



Pins external to ASIC

Inputs

TGRthresh	Trigger threshold (global)
TRGbias	Bias current for Comparator
SGN	Select signal polarity (0 = neg. signal; 1 = positive)
Wbias	1-shot width adjustment

Output

Dhit	Trigger output 1-shot

Figure 5: *This schematic diagram shows how the self-triggering system is designed to work in the BLAB3A. There are four input DAC parameter values that control the triggering mechanism. These are TGRthresh, TRGbias, SGN, and Wbias. Currently on the BLAB3A the trigger threshold is set globally and so there is only one threshold value for all 8 channels. This is something that will be fixed later on. The TRGbias is a bias current to set the Comparator. SGN is the bit used to set whether the trigger will register on a down going signal edge or an up going signal edge. Wbias is a signal used to determine the width of the 1-shot that comes from a successful trigger. The Dhit 1-shot trigger pulse is ultimately routed back through the FPGA to signal the Wilkinson ADC to start digitizing the signals inside the 512 $\times$ 64 sample window storage arrays.*

References

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