Physics 475: Electronics for Physicists

Final Project Write-Up

BLAB3A Trigger Evaluation for the mini-Time Cube

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December 12, 2011

Introduction & Motivation

For my project this semester I collaborated with Michinari Sakai in assessing the triggering capabilities of the third generation Buffered-Large Analog Bandwidth Recorder and Digitizer with Ordered Readout (BLAB3A) application specific integrated circuit (ASIC). Our motivation for choosing this project stems from a larger project known as the mini-Time Cube (mTC).[1] The mTC is a prototype neutrino detector designed to detect the inverse beta decay process caused by the interaction of an electron anti-neutrino and a proton (figure 1). This type of "decay" occurs when an anti-electron neutrino interacts with a proton to create a neutron and positron. The signature of this interaction is a "prompt" signal (release of photons) from the positron annihilating with an electron, followed some 10's of microseconds (depending on the energy of the incident anti-neutrino) later by a "delayed" signal from the neutron being captured on a nucleus.[2] This process has been widely utilized by physicists as a way of detecting and studying neutrinos and their properties.[3][4][5] What is novel about the mTC is its size and portable nature. Most detectors built to study neutrinos consist of a large volume (kiloton range) of scintillating material. The pay off of having such a large detector is that you are much more likely to 'see' a neutrino, and given the neutrino's minuscule mass, and the fact that it only takes part in weak interactions, this turns out to be a a rather difficult thing to do. However, a pressing issue in neutrino physics has to do with how the neutrinos oscillate between three flavors (electron, muon and tau) of neutrinos as they propagate through space and it is here that the mTC is uniquely capable of making some very interesting discoveries. Given its portable nature we will be able to place the mTC at varying locations from a neutrino source (nuclear reactor) and make precise measurements of the neutrino oscillations. Furthermore, its small size (scintillating volume is 13cm^3) should allow us to resolve the oscillations on a scale not previously achievable.

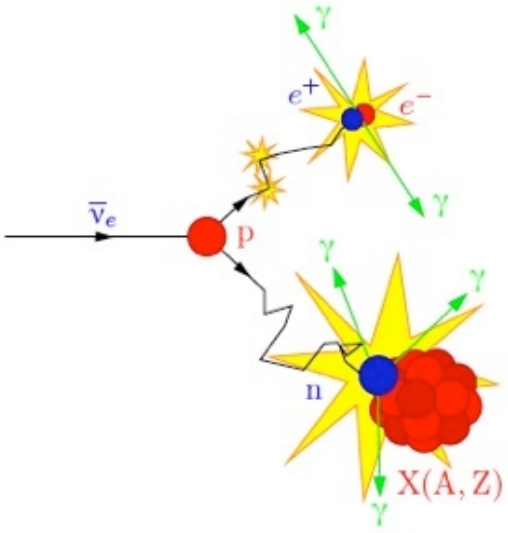

Figure 1: Schematic representation so the inverse-beta decay process. Currently the mTC's scintillating volume is doped with Boron-10 which is represented by the 'X' nucleus that capture the neutron.

mini-TimeCube

The mTC is constructed using a boron doped plastic scintillator cube (~2 liter volume) as the target for incident neutrinos. Each of the six sides of the cube are covered by 4 Photonis Planacon micro-channel plate photomultiplier tubes (MCP – PMTs)[6]. These PMTs have a 8x8 anode array, 64 output channels. Typical rise time for the channels is 0.6ns with typical gain of 600k (these number are from the Photonis data sheet and will need to be systemically tested for each channel, and each tube). Since the BLAB3A is an 8-channel digitizer, each PMT will need 8 BLAB3As. A board stack was fabricated to carry these ASICs as well as control the operations of the BLAB3As which consists of a Standard Control and Read-Out and Data (SCROD) board, an interconnect board that will link the SCROD to the four ASIC carrier cards (each carrier card supporting four ASICs) as well as two boards designed to mate directly with the PMTs. (figure 2) The BLAB3As are the first step of the read out process which also involves fiber links to a data acquisition system (DAQ) based on cPCI format. (figure 3)

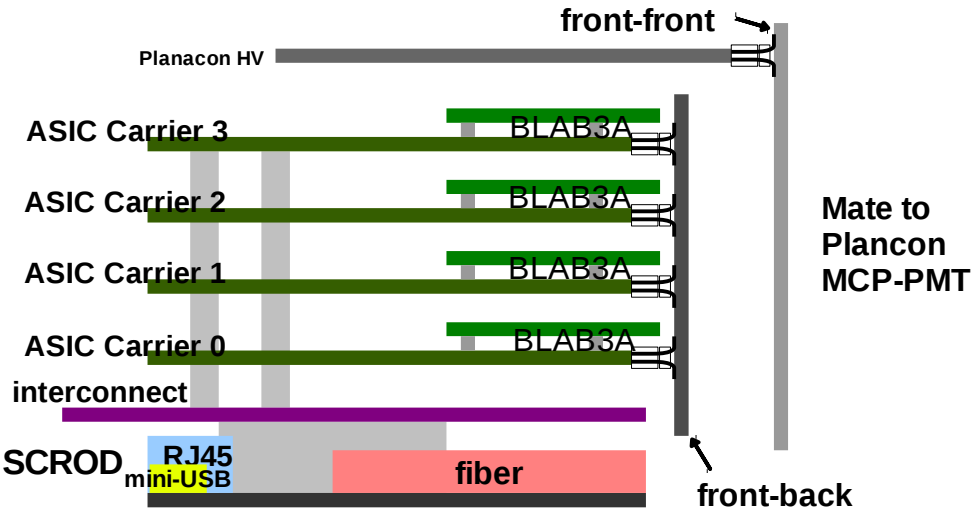

Figure 2: Front end board stack schematic, side view.

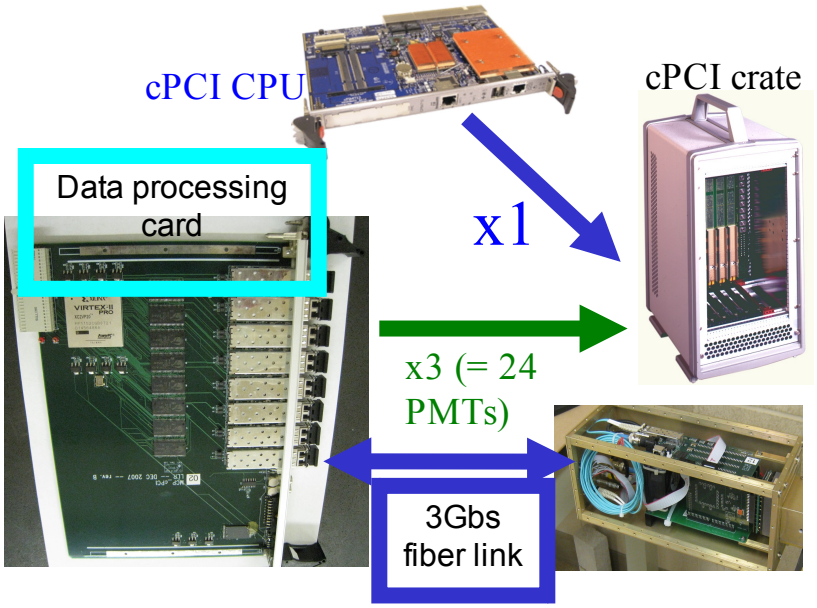

Figure 3: Flow diagram of back end electronics starting from front end board stack readout in bottom right.

BLAB3A

The BLAB3A ASIC is an 8-channel, low-power pico-second timing resolution waveform recorder and digitizer. It is intended for detector applications which require data sampling rates of around 2-4 Giga-samples per second (GSa/s). Triggered readouts rates of up to 100kHz are possible. Internal 1kΩ Transimpedance Amplifiers (TIA) on each input channel are able to sample small amplitude signals. There are two 64 sampling array windows for each channel (these are toggled between so that the BLAB3A can process input signals while writing to the on board storage), as well as 512 64-sampling windows of on board storage which should allow for storage of a complete inverse beta decay signal. Lastly, the signals that are deemed important are digitized, through a Wilkinson ADC architecture, just before being passed on to the back-end electronics for off-line processing and analysis.[7]

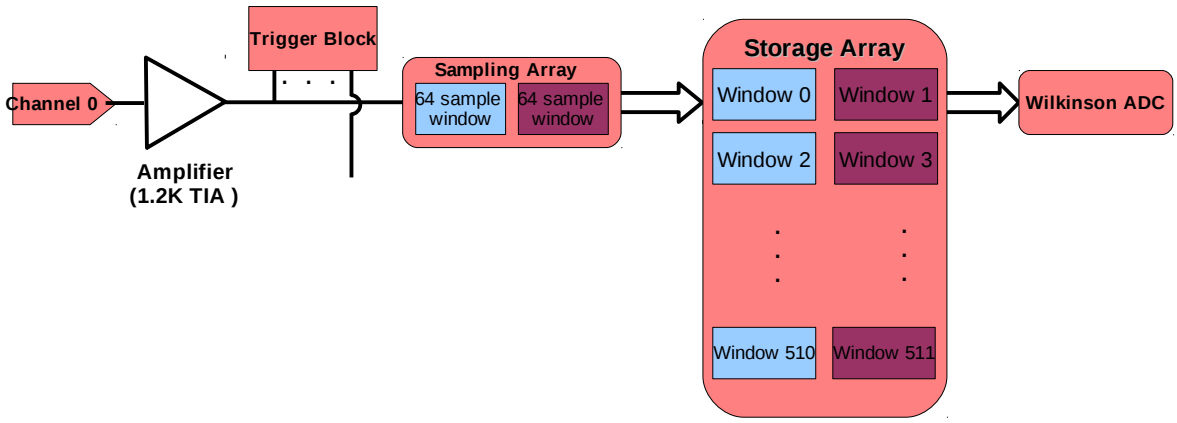

Figure 4: BLAB3A ASIC block diagram. Showing the one of the eight input channels, the internal amplifiers, 64 sample windows, 512 banks of 64 storage cells and finally, Wilkinson analog to digital converter (ADC) for each channel.

The Trigger

Our goals for this project was a necessarily modest given the large scope of the mTC project. We attempted to feed a mock PMT pulse and 1) see that a trigger signal was sent to the an FPGA on the control board, SCROD and 2) familiarize ourselves enough with the firmware to adjust the inputs to the trigger block (figure 5), both in the firmware code itself, and via the virtual input/output (VIO) core through the use of Chipscope. Chipscope is a basically a virtual oscilloscope that allows one to probe internal node of an integrated circuit.

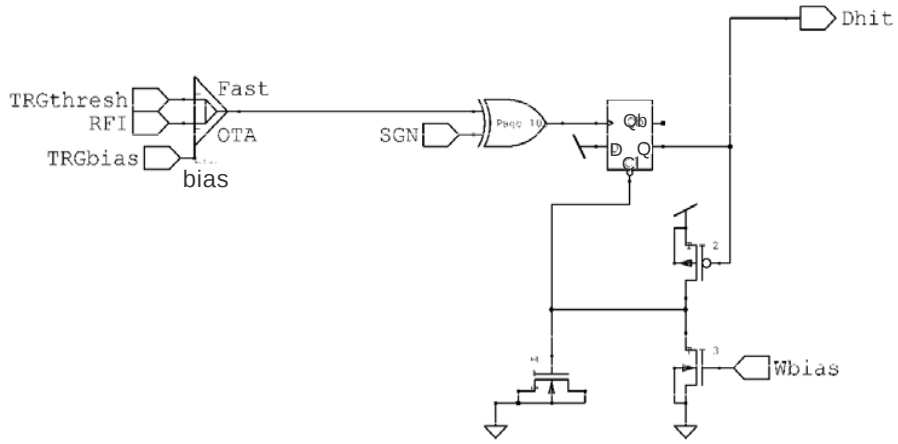

Figure 5: Trigger block schematic, showing the four inputs external (TRGthresh, TRGbias, SGN, Wbias) to the ASIC that are set by DAC voltage levels and one output signal (Dhit).

Outcomes

After obtaining a board-stack with one BLAB3A, a copy of the firmware code, a JTAG programmer and Xilinx's ISE, we first needed to reassign pins in the programs user constraint file since the version of the code we had was designed for a slightly different ASIC, the IRS2, and not the BLAB3A. This proved more difficult then expected since the schematics from the BLAB3A as well as the digital analog converters did not directly relate to what was used in the code.

We are able to adjust the various trigger signals (trigger threshold, input bias, one-shot width, and signal polarity) both in the firmware code and through the VIO core.

What we did see was a trigger signal that switched on and off, which was encouraging at first. However, under closer examination we realized that the frequency that this trigger signal switched was not actually correlated with frequency of our input signal. So ultimately our results were inconclusive.

Since Mich and I are both new to the world of firmware we were still encouraged by the progress we were able to make, namely: greatly improve our understanding the working of the BLAB3A (and consequently the IRS2, which will be useful if we do eventually end up having to switch to this ASIC) the SCROD and the DAC that control analog signals to the ASIC, we are both more capable of working with ISE in identifying and adjusting necessary firmware code, and finally in generating Chipscope cores in the firmware that allow us to probe inside the ASIC. And though our work not conclusive we feel that the work we have done has put us in a good position to make real progress next semester when we will be studying modern electronics.

References

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