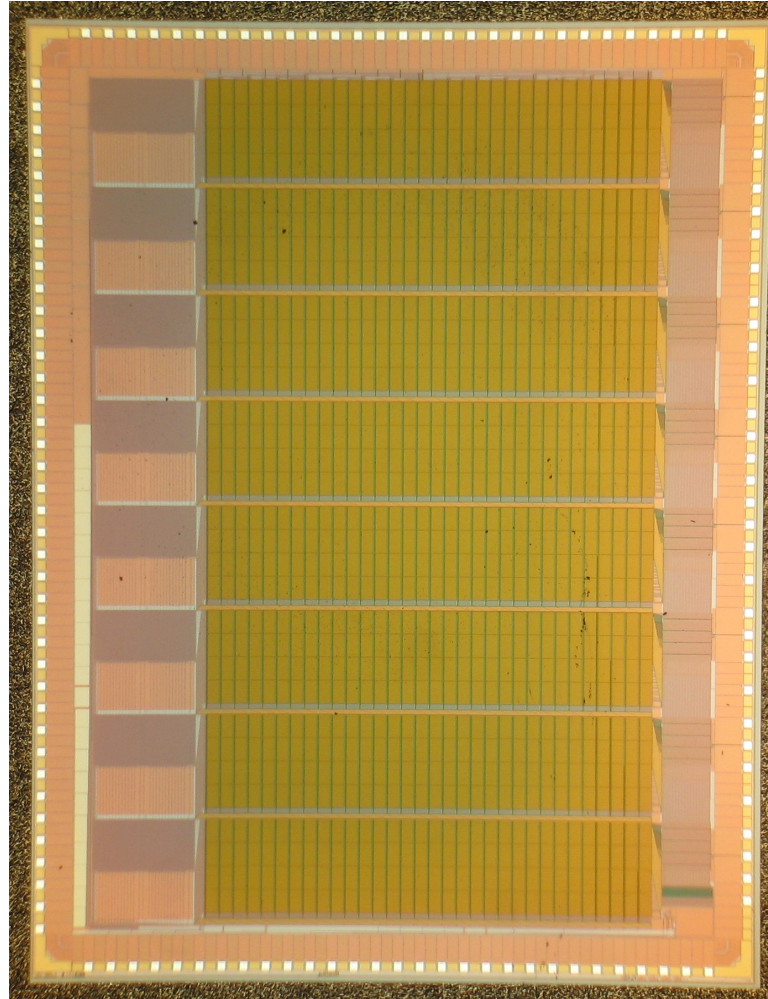


# BLAB3A Trigger evaluation for mini-Time Cube

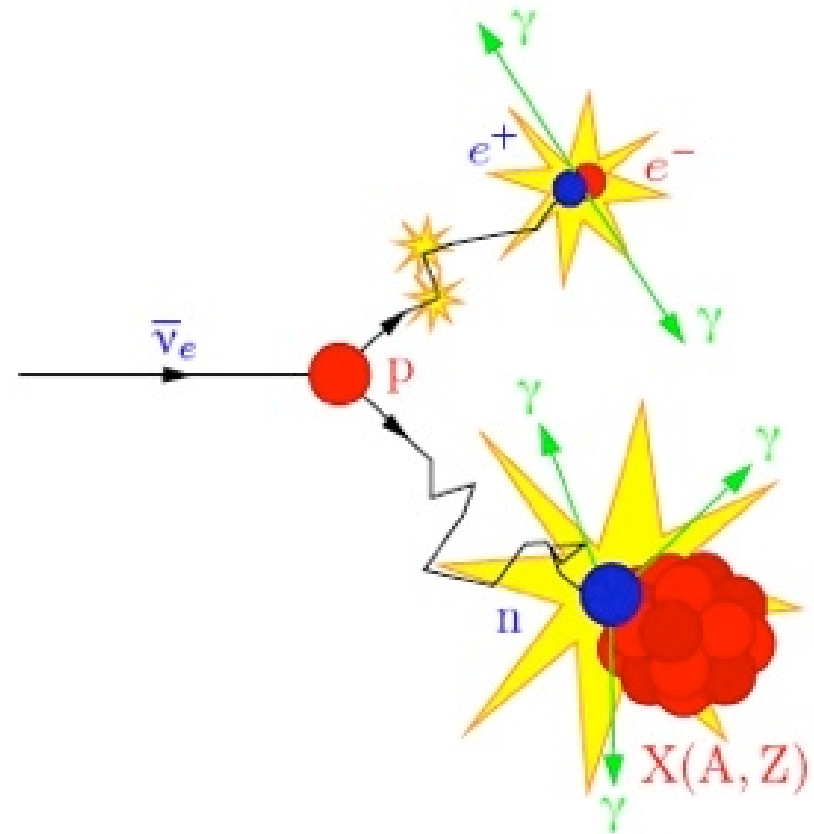


Michinari Sakai & Joshua Murillo

December 8, 2011

# Detecting Neutrinos

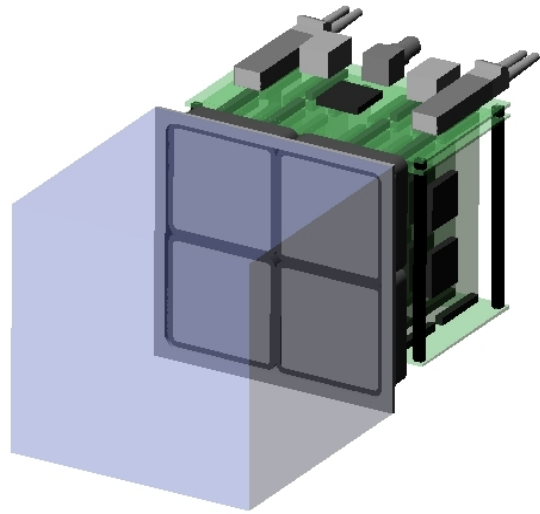
- In most modern neutrino experiments the anti-neutrinos are detected through the inverse-beta decay process using a technique known as “delayed coincidence”
- Coincidence time is on the order of  $\mu\text{s}$



Inverse beta decay schematic

# mini-Time Cube

- mTC is a prototype neutrino detector, designed to detect inverse-beta decay interactions caused by (anti)neutrinos.
- The BLAB3A is our candidate front-end read out digitizing ASIC for the mTC.

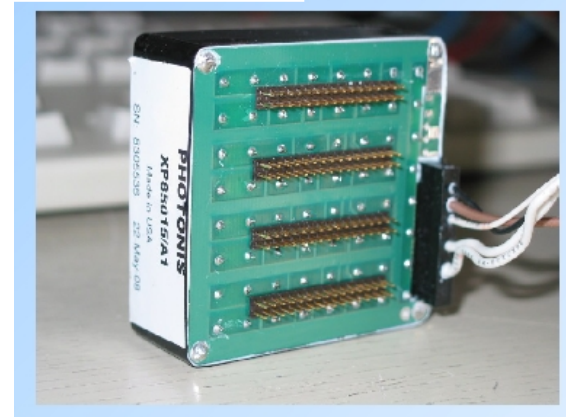
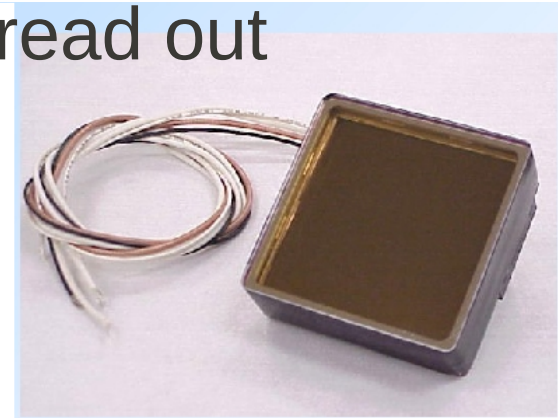


mTC with read-out electronics on one face

Dimensions:

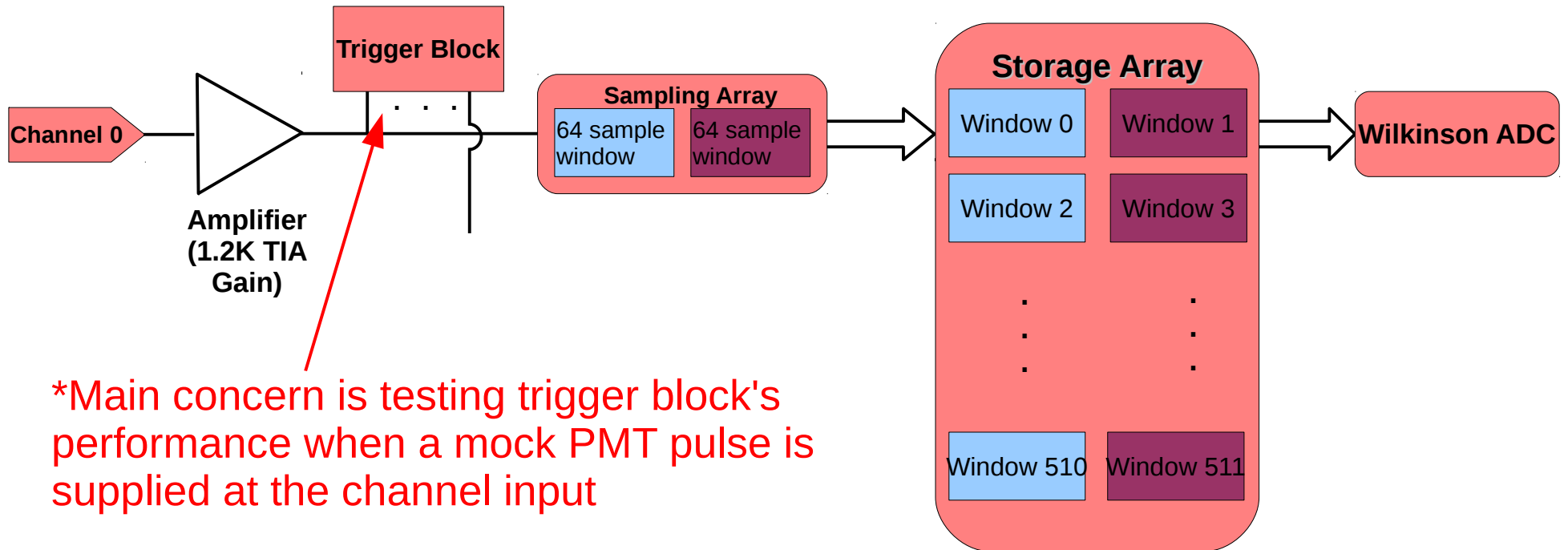
Scintillating cube -  $13\text{cm}^3$

Populated with PMT's and read-out electronics -  $\sim 38\text{cm}^3$



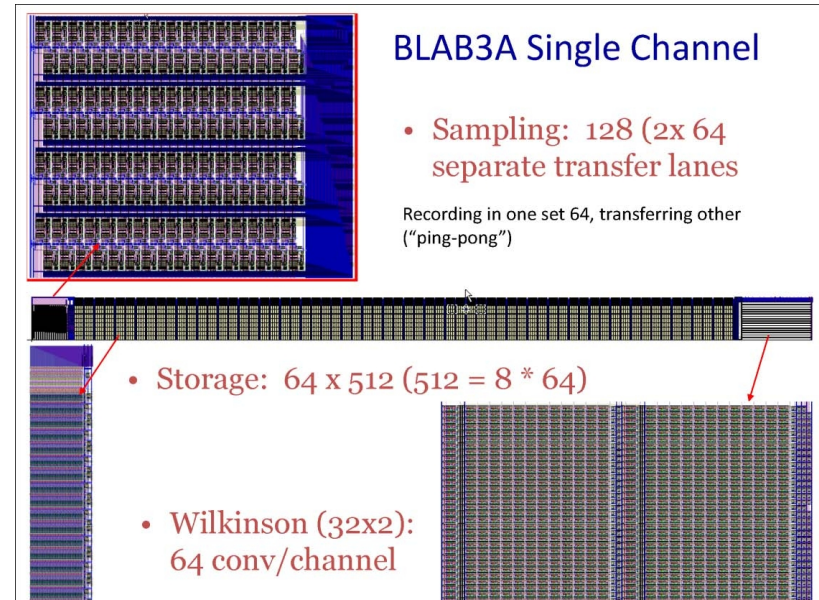
8X8 anode structure  
Burle Industries  
micro-channel plate photomultipliers.

# BLAB3A single channel block diagram

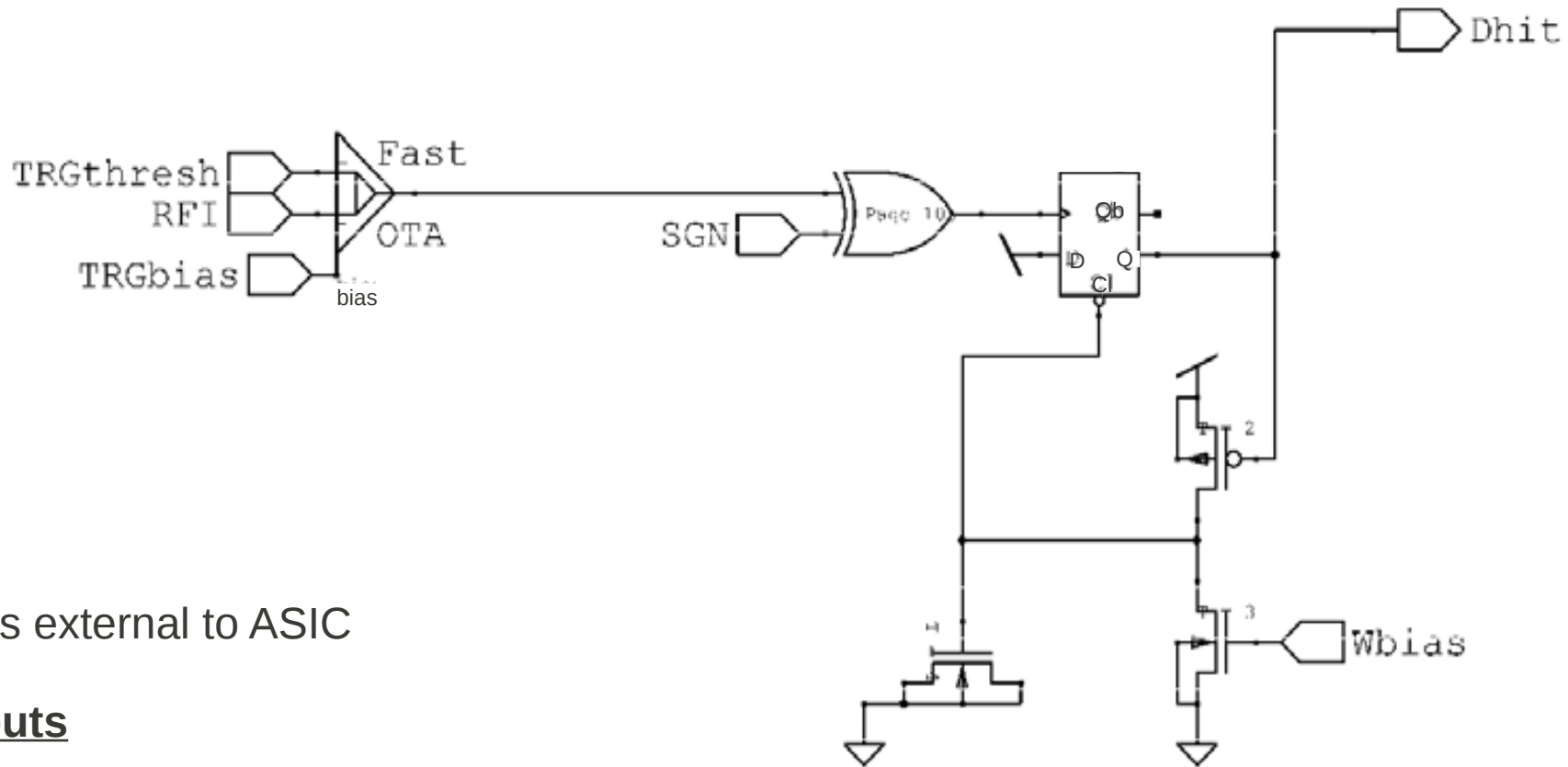


## Specifications

- # of channels: 8
- Power: 20mW/channel
- Sampling Speed.: 2~4 Giga-samples per second
- Readout rate: up to 100kHz
- Amplification: ~1.2kOhm (measured) TIA on each channel



# Trigger Schematic



Pins external to ASIC

## Inputs

- TGRthresh** Trigger threshold (global)
- TRGbias** Bias current for Comparator
- SGN** Select signal polarity (0 = neg. signal; 1 = positive)
- Wbias** 1-shot width adjustment

## Output

- Dhit** Trigger output 1-shot

# Preliminary Outcomes

- What we were able to do
  - Make mock pulse is negative: width 50-100ns, height ~20mV.
  - Identify channel 1 of 0~7 channels, row 0 of 0~3 rows, column 0 of 0~3 columns, via Chipscope.
  - Adjust trigger values (TRGthresh, TRGbias, SGN, Wbias) via Chipscope using virtual input output (VIO) core or simply set nominal values in VHDL code.

# Demonstration

# Outlook

- This project was a great way to “get our feet wet” and we both learned a substantial amount about:
  - 1)BLAB3A, as well as the workings of the board stack (SROD, carrier boards, DAC's)
  - 2)VHDL code and ISE
  - 3)Generating cores via Chipscope for debugging
- Our testing of the BLAB3A was not conclusive in identifying whether or not this ASIC will work for the mTC project.

**This work will continue in spring semester.**