R&D of Thinned CMOS Pixel Sensors for the ILC Vertex Tracker

Ben Hooberman[1*], Marco Battaglia[1], Devis Contarato[2], Kristen Flowers[2], Lindsay Glesener[1], Leo Greiner[2], Piero Giubilato[3], Howard Wieman[2]

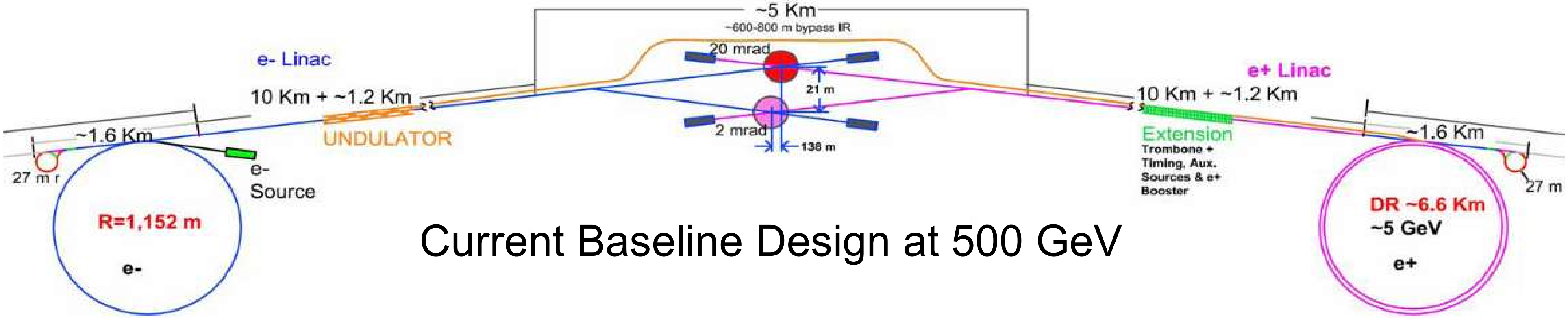
- [1]University of California at Berkeley and Lawrence Berkeley National Laboratory
- [2]Lawrence Berkeley National Laboratory
- [3]Lawrence Berkeley National Laboratory and INFN, Padova

*benhooberman@berkeley.edu

special thanks to Robert Foglia, Aptek Industries

Table of Contents

The International Linear Collider



Current Baseline Design at 500 GeV

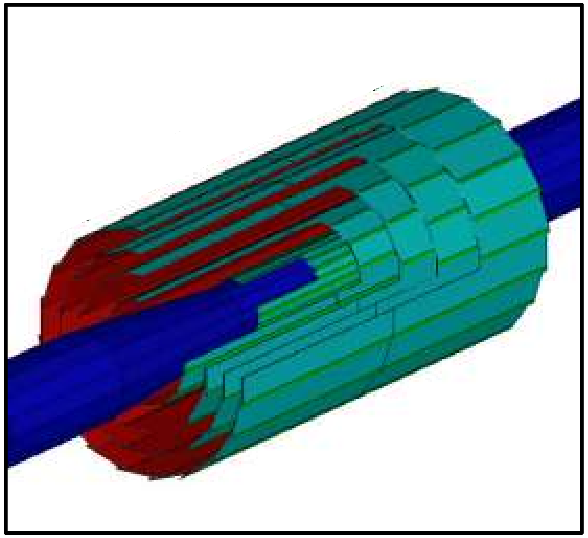
- e^+e^- collider proposed for construction ~2010
- Tunable E_{cm} up to 0.5 TeV, upgradeable to 1.0 TeV
- ILC/LHC complementarity
- Precision physics in TeV regime

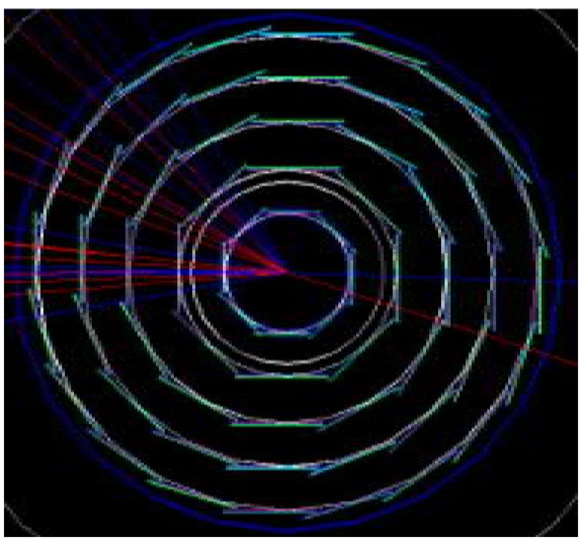
	LHC	ILC
particles	pp	e^+e^-
E_{cm}	14 TeV	tunable 0.5-1.0 TeV
geometry	circular	linear
role	discovery	precision measurement
advantages	high E_{cm}	tunable energy low background

Physics Program

- Measure Higgs couplings and quantum numbers
- Probe physics beyond SM and its relation to dark matter

The ILC Vertex Tracker





Geometry

- Cylindrical layers (multi-barrel)
- Ladders of silicon sensors

Function

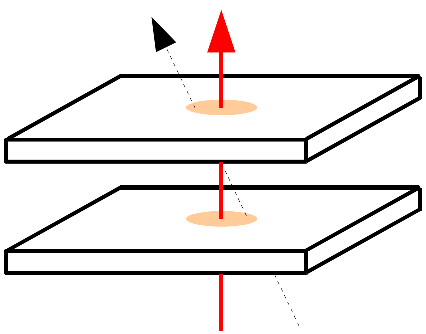
- Extrapolate charged particle interaction point (vertex)
- Primary/secondary particle discrimination
- b/c/τ tagging, vertex charge determination

Layer	Radius [mm]	Length [mm]
1	16.6	100
2	27.6	250
3	39.6	250
4	50.6	250
5	61.6	250

Physics Requirements for VTX

- Impact parameter resolution: [5 ⊕ 10/p $\sin^{3/2}(\theta)$] mm
  - Spatial extrapolation resolution: $\sigma < 4$ mm →
  - Multiple scattering: $X/X_0 < 0.1\%$ per layer →
- High granularity (high background) →
- Radiation tolerance, fast readout

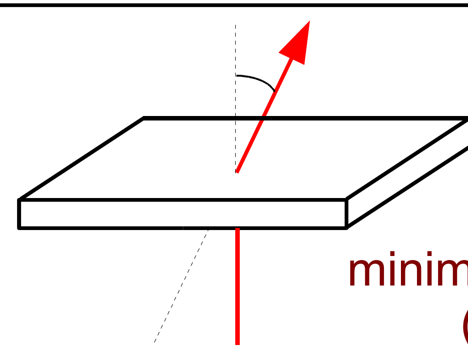
Monolithic Pixel Sensors



$$\sigma_{EE} \sim \frac{\sigma}{R}$$

maximize spatial res,
maximize lever arm

Extrapolation Error



$$\sigma_{MS} \sim \frac{1}{p}\sqrt{\frac{X}{X_0}}$$

minimize detector thickness
(material budget)

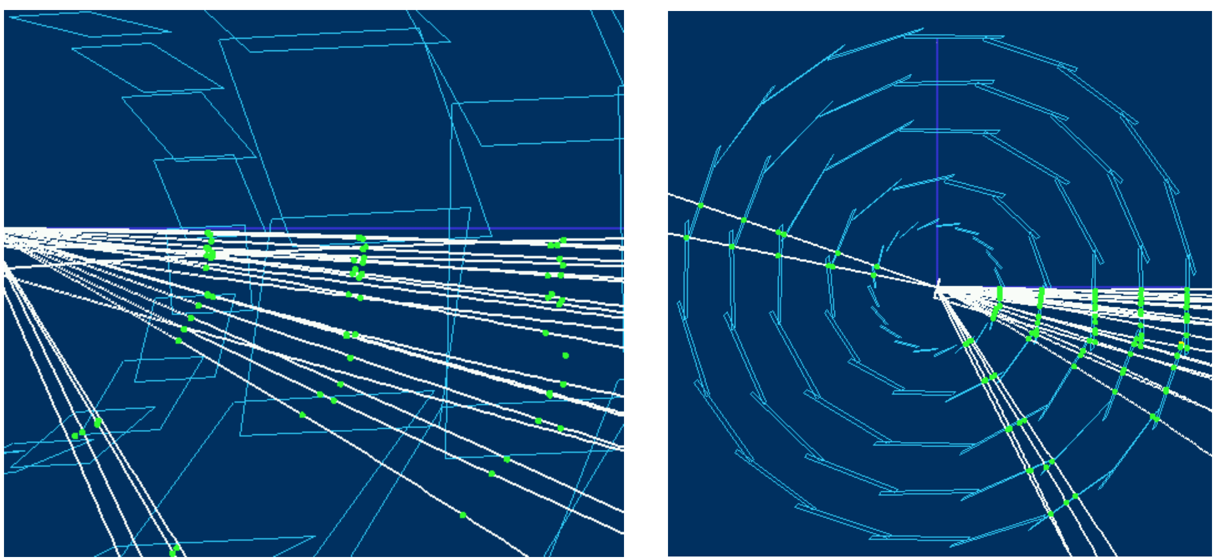
Multiple Scattering

Ben Hooberman
DPF2006

Full VTX Simulation and Reconstruction

Pythia/Guinea Pig physics/pair background event generation	→	**GEANT4/Mokka** full detector simulation	→	**Marlin** reconstruction/ data analysis	←	**real data from telescope/chips**

HZ → $b\bar{b}$ Marlin Event Display



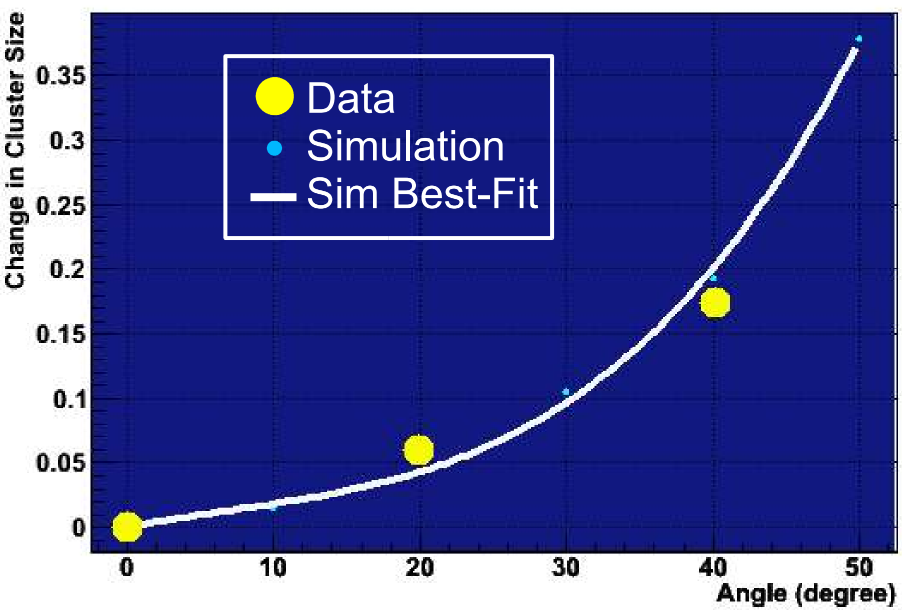
Reconstruction for ILC VTX in Marlin framework developed at LBL, including:

- Pixel simulation
- Cluster reconstruction
- Pattern recognition
- Track-fitting
- Jet-flavor tagging

Validation and Optimization

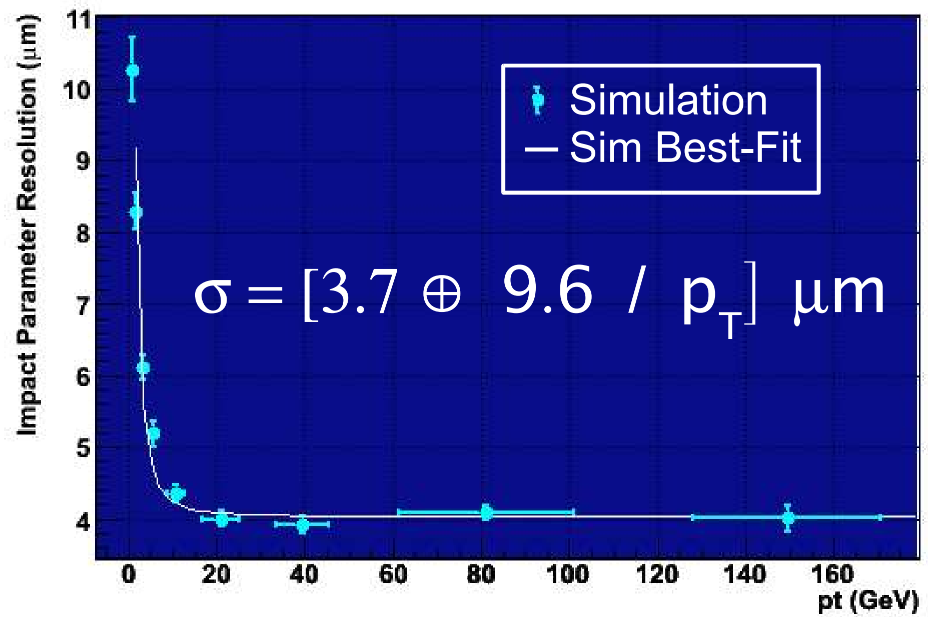
Mokka + Marlin Simulation vs. 1.5 GeV e^- Data

- Relative cluster size as a function of incidence angle
- Validate simulation/reconstruction with beam test data

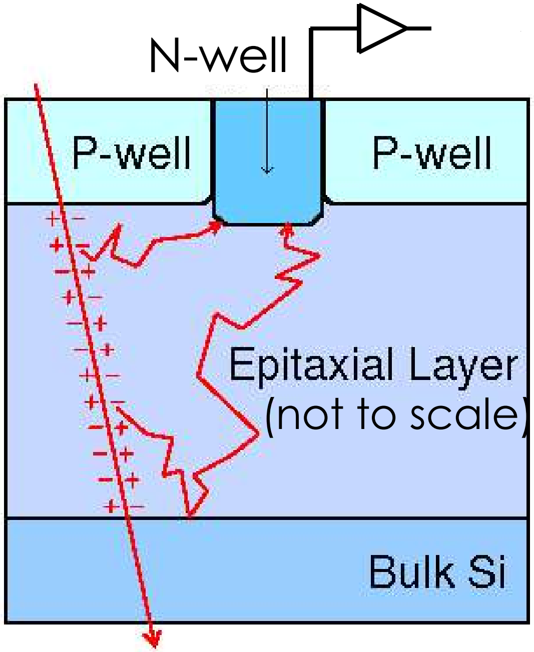


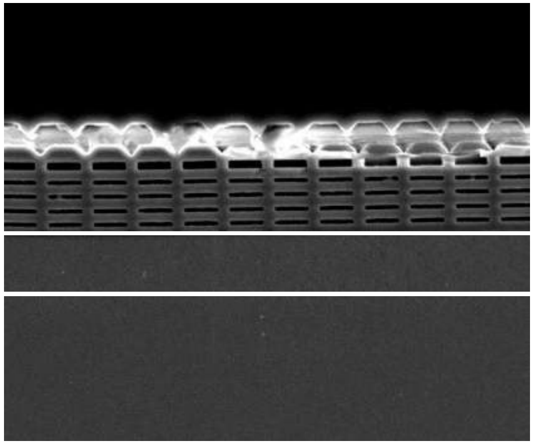
Mokka + Marlin Simulation

- Determine impact parameter resolution over p_T range
- Determine performance for various sensor designs/detector configurations



CMOS Pixel Sensors





Principle of Operation

- Ionizing particle generates electron-hole pairs in silicon
- Electrons → collection diodes via thermal diffusion (no applied E-field)

Structure: 3 integrated layers

- ~10 μm electronics layer: read-out and logic/data processing
- 10-20 μm epi-layer: P-type sensitive volume, low resistivity, undepleted
- 300-500 μm bulk SI: structural support/substrate

Advantages of CMOS:

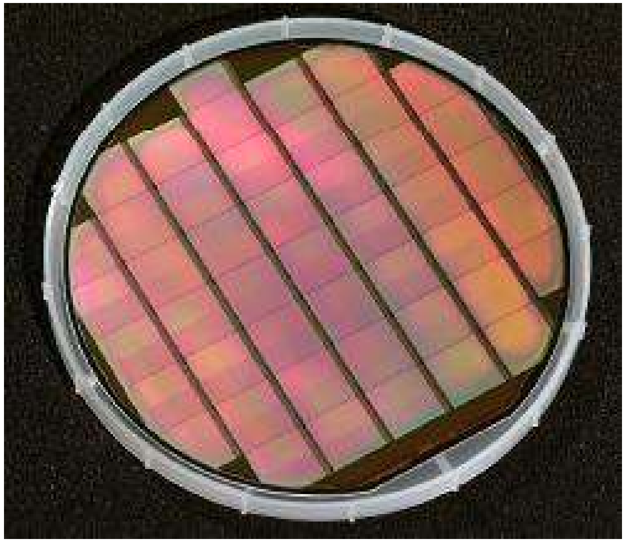
- Integration of readout/logic electronics on single substrate
- Small feature size allows pixels of small pitch
- Widely available, cheap commercial process

CMOS R&D @ LBL supported by 3-year LDRD grant

Back-Thinning: Motivation and Strategy

- Vertex Tracker at ILC requires 0.1% X_0 / layer (< 50 µm Si)
- CMOS Sensors: sensitive layer thickness 10 – 20 µm and ~400 µm bulk Si
- Perform back-thinning: remove majority of bulk Si by mechanical grind process
- Aptek Industries capable of grinding single chip to minimum thickness 25 µm
- Strategy: characterize individual diced chip before and after thinning to study effects on charge collection
- Some degradation observed in earlier studies with back-thinned CMOS sensors
- Goal: demonstrate CMOS sensors can be thinned without sacrifice in performance

The MimosaV Prototype Chip



- produced at IPHC, Strasbourg 0.6 μm AMS CMOS
- > 1 million pixels, 1.7 x 1.7 cm^2 active area (large)
- 14 μm epi-layer, 17 μm pixel pitch, 450 μm thick
- 4 independent sectors of 512 x 512 pixels
- analog output

Characterization Procedure

Step 1: Characterization

- Use 5.9 keV peak in ^{55}Fe spectrum to measure charge-to-voltage conversion gain
- Probe charge generation in epitaxial layer with 850 nm laser
- 1.5 GeV e^- test beam at Advanced Light Source at LBNL

Step 2: Back-Thinning

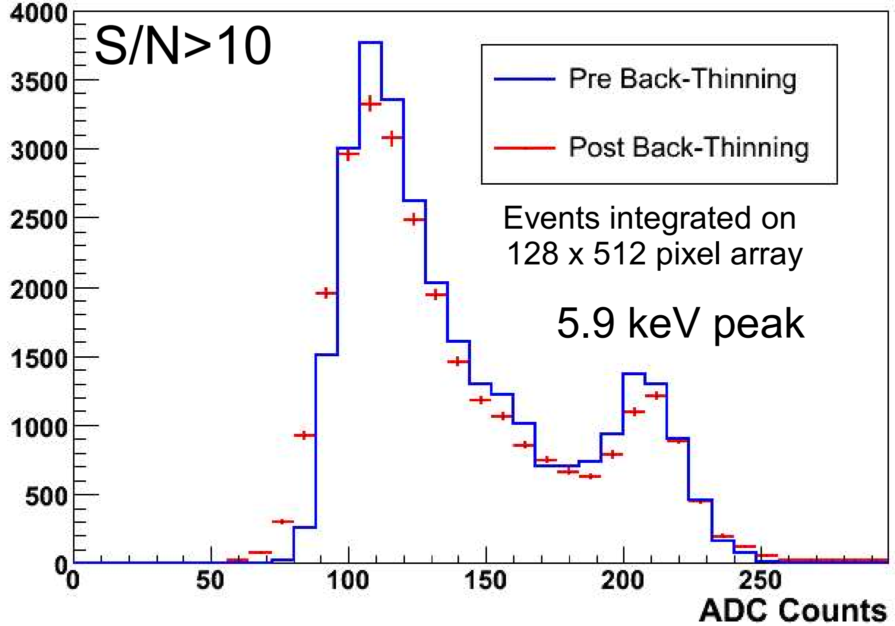
- Chip is mounted to grinding plates, wet grind process
- Achieve arbitrary thickness down to 25 μm with flat back surface

Step 3: Re-characterization

- Repeat testing procedure and compare with prior results

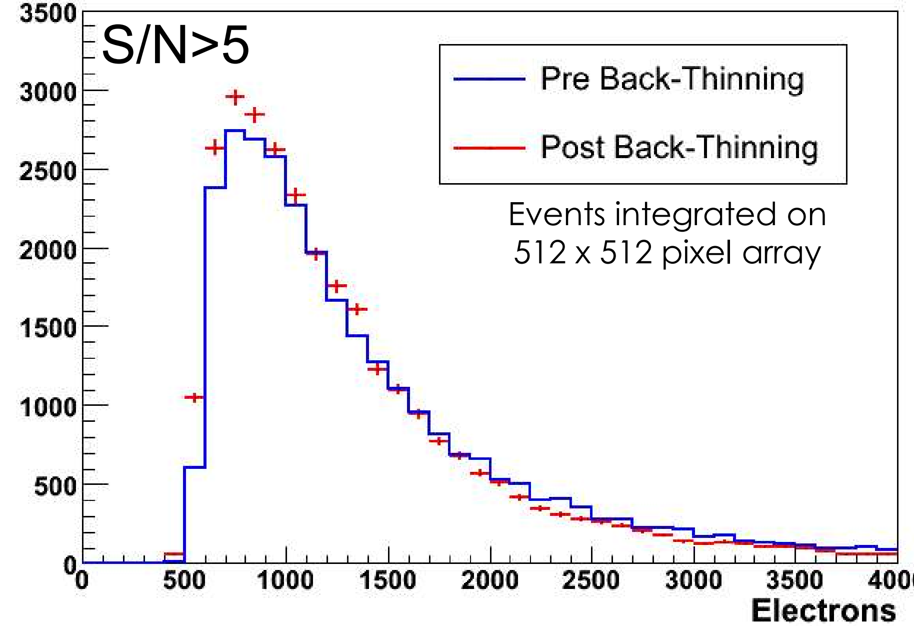
Results for Thinning to 50 μm

Sample ^{55}Fe Spectra



- Fit gaussian to 5.9 keV peak pre/post-thinning to measure change in gain
- Results for multiple sectors of 1 chip: [7±8]% decrease in mean of Gaussian best-fit
- **No significant change in gain observed**

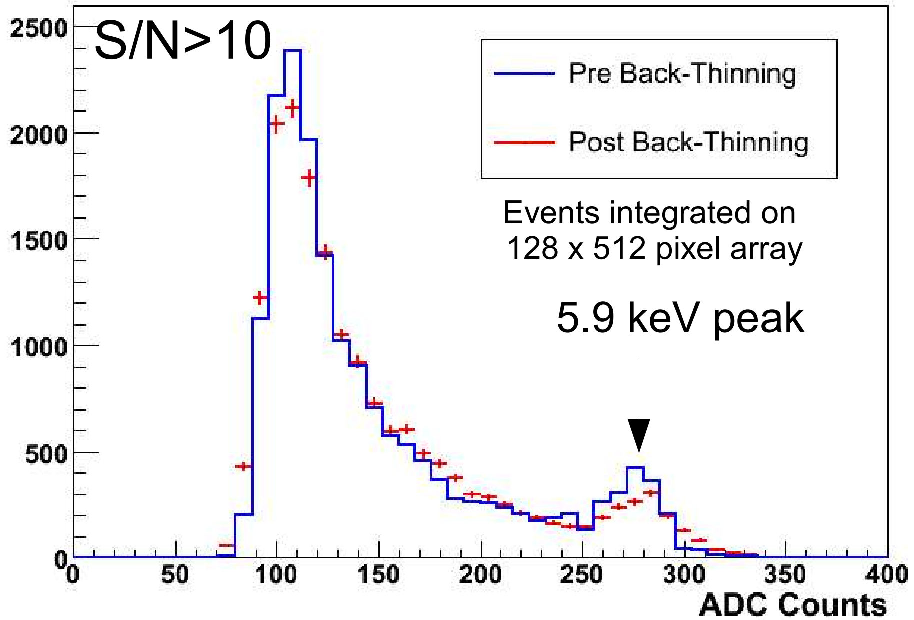
Sample 1.5 GeV e^- Spectra



- Fit Landau function to 1.5 GeV e- spectrum to measure change in collected charge
- Results for multiple sectors of 1 chip: [9±7]% decrease in MPV collected charge
- **No significant change in collected charge**

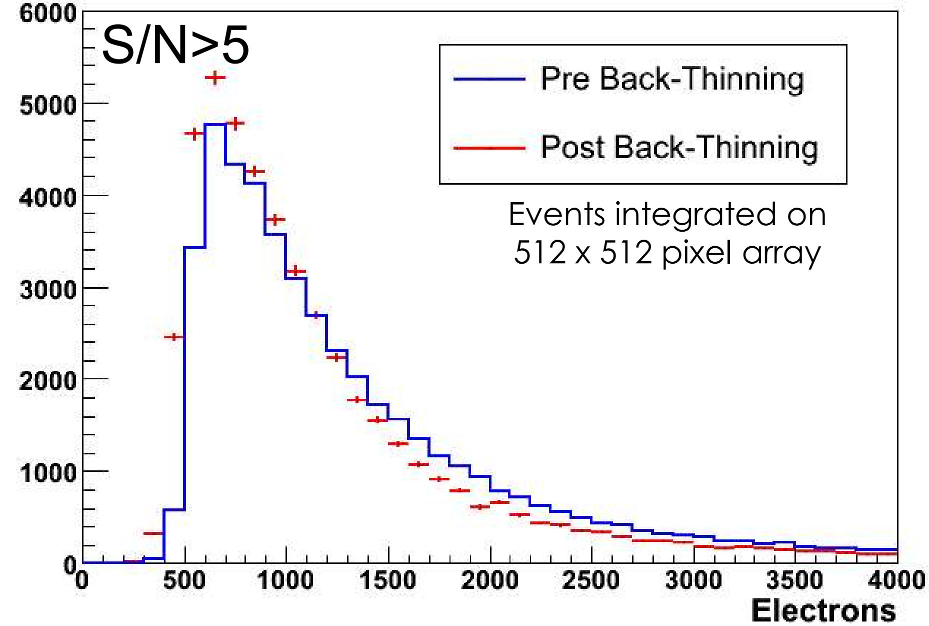
Results for Thinning to 40 μm

Sample ^{55}Fe Spectra



- Fit gaussian to 5.9 keV peak pre/post-thinning to measure change in gain
- Results for multiple sectors of 1 chip:
  [2±2]% decrease in mean of Gaussian best-fit
- **No significant change in gain observed**

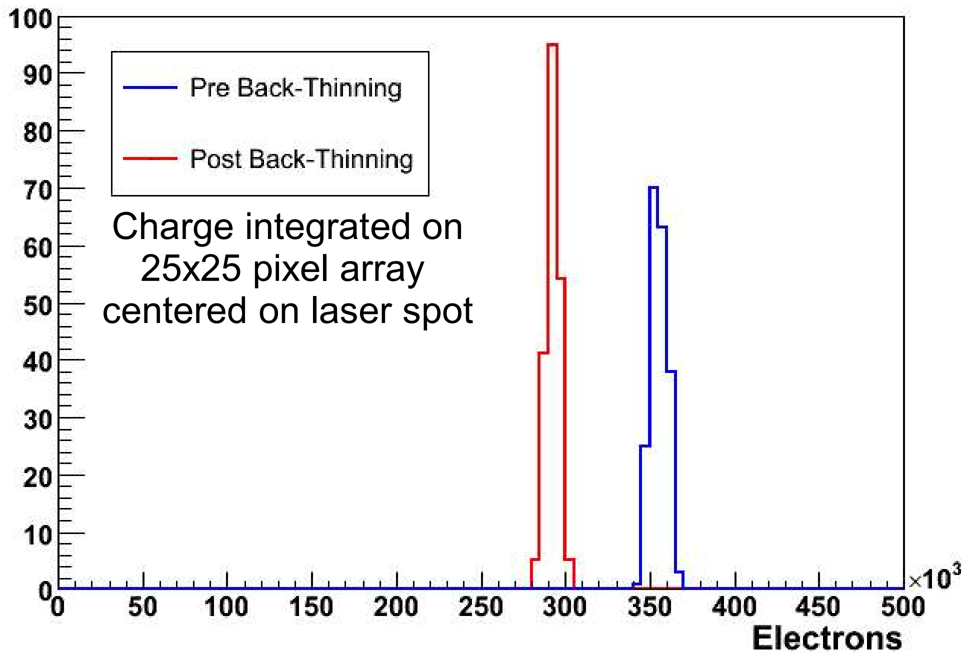
Sample 1.5 GeV e^- Spectra



- Fit Landau function to 1.5 GeV e- spectrum to measure change in collected charge
- Results for multiple sectors of 1 chip:
  [2±4]% increase in MPV collected charge
- **No significant change in collected charge**

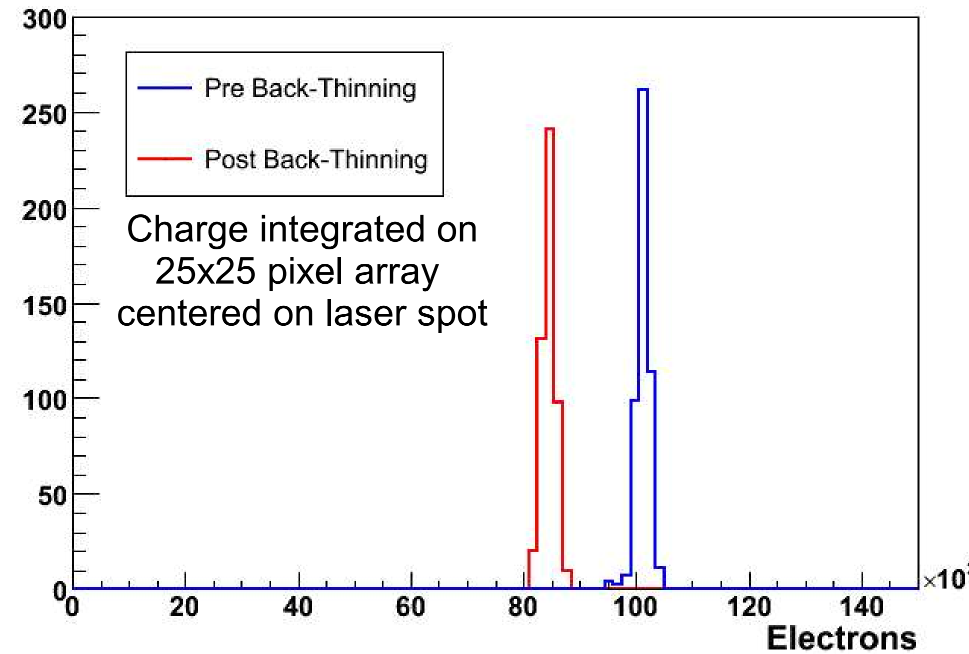
850 nm Laser Results

Chip Thinned to 50 μm



- Results for multiple sectors of 1 chip: [16±6]% decrease in collected charge
- **Some evidence of signal loss**

Chip Thinned to 40 μm



- Results for multiple sectors of 1 chip: [10±6]% decrease in collected charge
- **Some evidence of signal loss**

Ben Hooberman
DPF2006

Summary of Results

Thickness	1-pix Noise	Fe-55	850 nm	1.5 GeV e^-	1.5 GeV e^- S/N
50 μm	+3±7	-7±8	-16±6	-9±7	**-1±1**
40 μm	+8±13	-2±2	-10±6	+2±4	**-1±3**

Results equal $(R_{after} - R_{before})/R_{before}$ x 100%, refer to multiple sectors of CMOS sensor

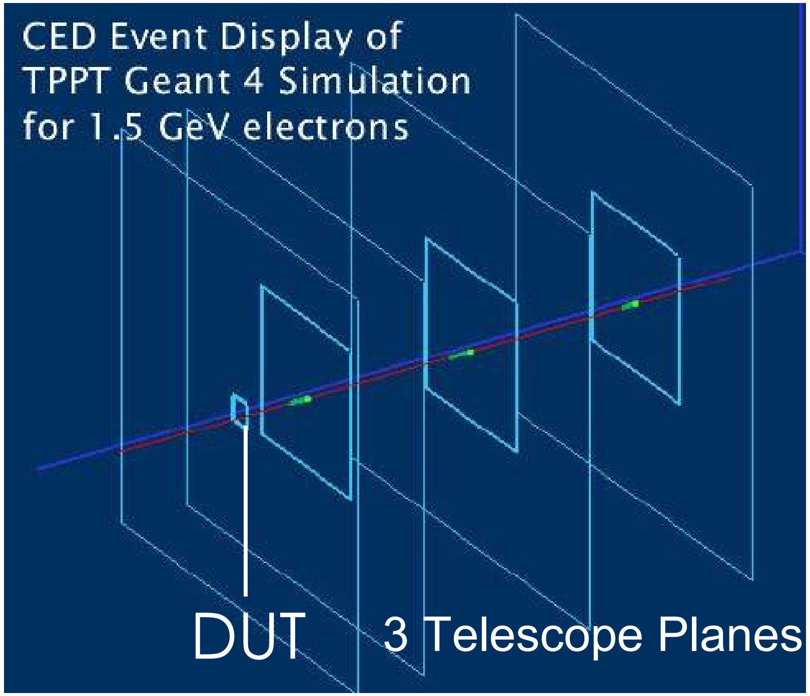
- Slight increase in single pixel noise
- Charge-to-voltage conversion gain not significantly affected
- Some signal loss for 850 nm lasers
- Total charge collected for 1.5 GeV e^- not significantly affected
- **No change in cluster S/N at 1.5 GeV e^- beam detected**

Encouraging results for prospects of CMOS VTX at ILC!

A Thinned Pixel Pilot Telescope (TPPT)

Background

- Build working prototype capable of tracking particles
- Multiple CMOS sensor planes and detector under test (DUT)
- Use ALS 1.5 GeV e^- test beam



Motivation

- Proof of principle of thin CMOS capable of tracking in realistic environment
- Study tracking with tunable track multiplicity, adjustable to expected ILC multiplicity
- Use telescope planes to extrapolate particle position on DUT → measure impact parameter resolution
- Characterize new sensors

Telescope Simulation Effort

Simulation

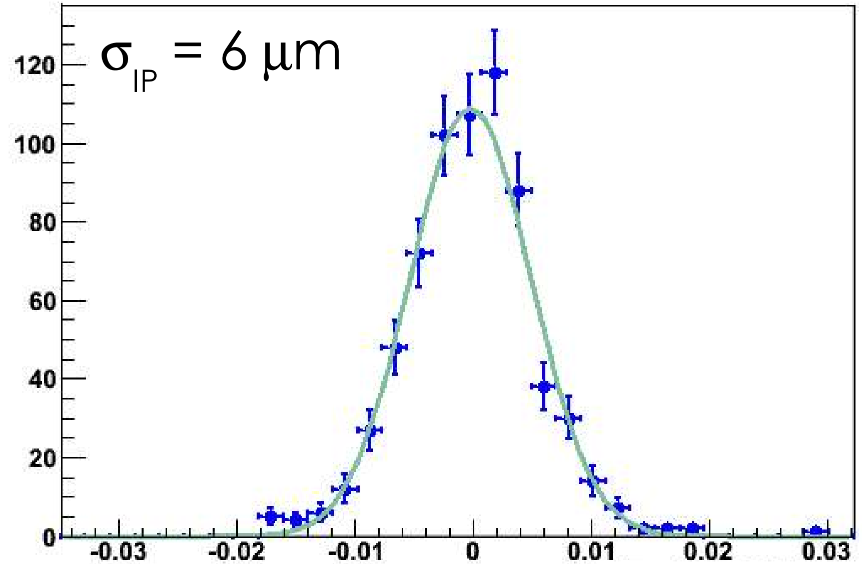
- GEANT4 generation/simulation + Marlin reconstruction
- Full pattern recognition and track-fitting
- Same reconstruction environment as for ILC VTX → validate sim/reco with real data

Sources of Error

- Spatial resolution of sensors
- Extrapolation error
- Multiple scattering

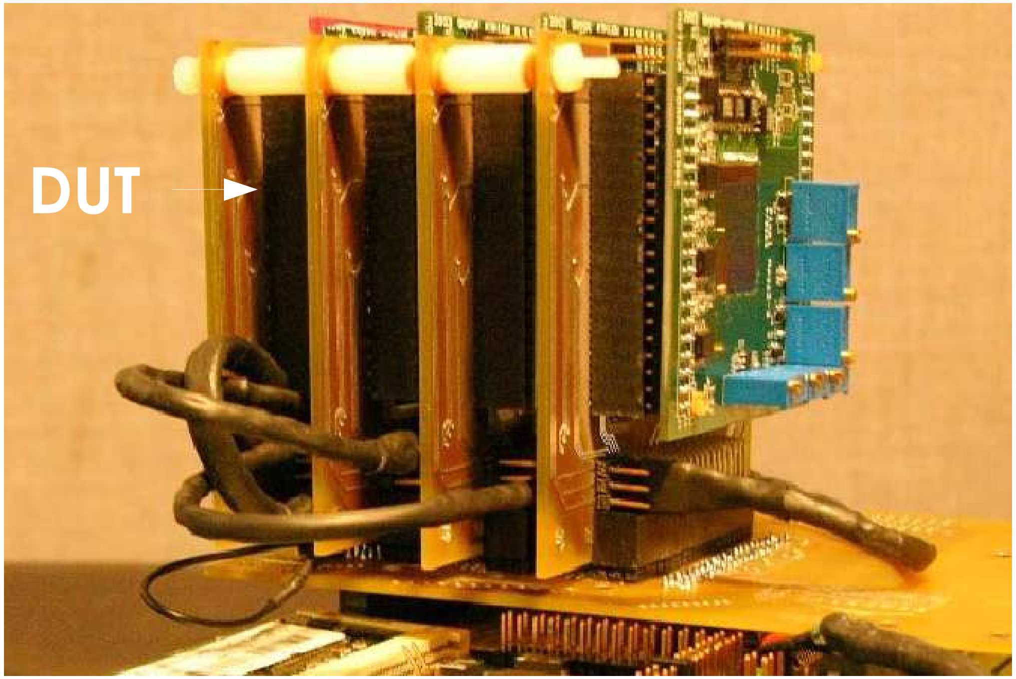
Real data: additional alignment and flatness error

TPPT Mokka + Marlin Simulation



Extrapolated – Measured Position [mm]
for DUT 17 mm from telescope plane

Telescope Experimental Setup



Data Acquisition and Analysis

- Labview: pedestal subtract, noise, CDS, on-line data sparsification
- Marlin: off-line reconstruction/analysis

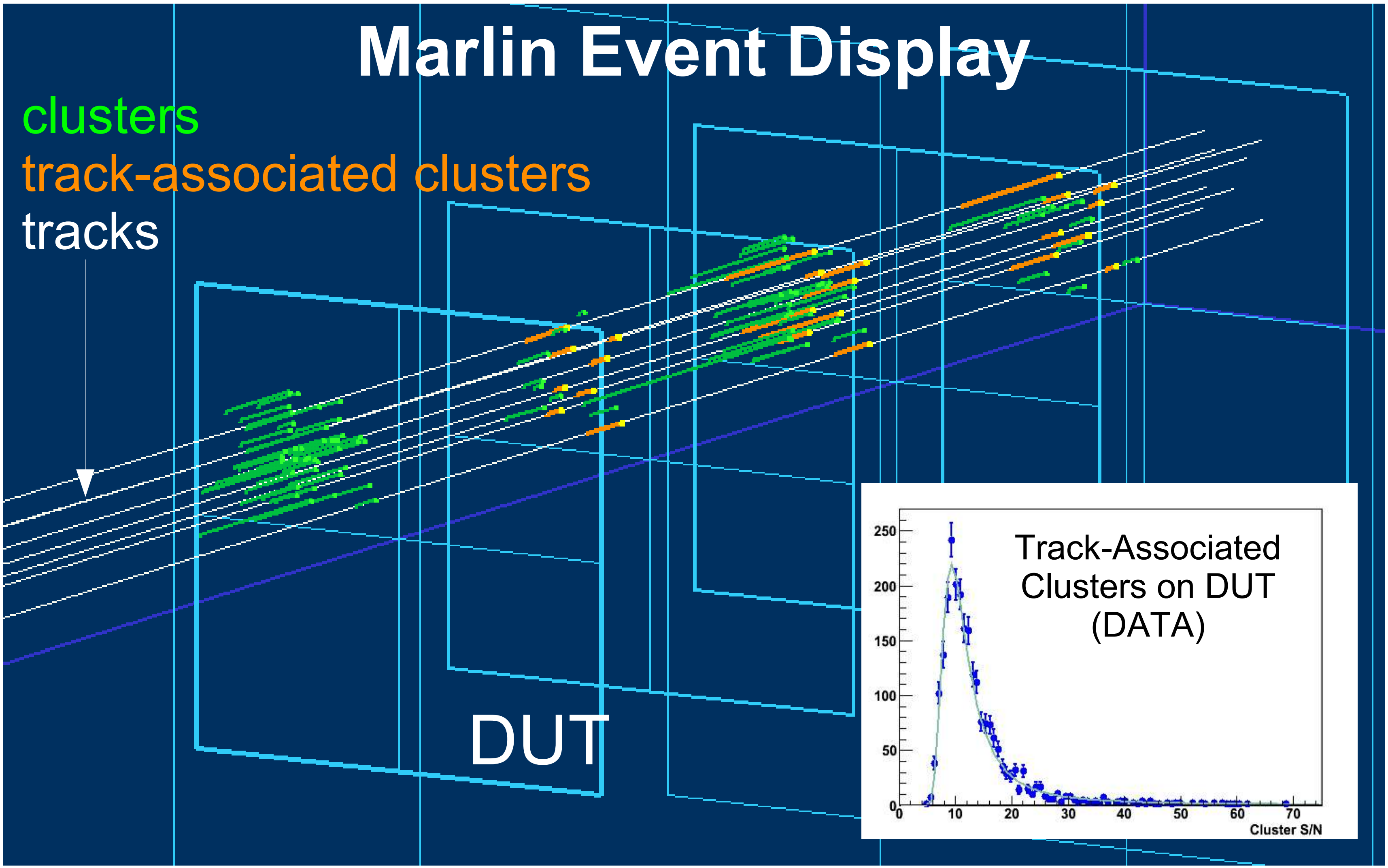
Configuration

- 3 planes of thin Mimosa V sensors (40 μm, 50 μm, 50 μm) + DUT
- Spacing ~17 mm, T = 27°C
- 1.5 GeV e^- test beam at ALS

Readout

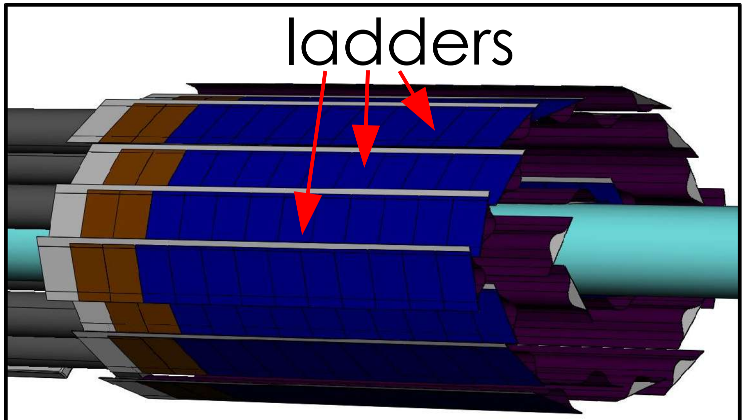
- Custom board (FPGA, 14-bits ADC's)
- Synchronized with 1 Hz extraction cycle
- 2 frames after reset, CDS
- 1 sector/layer (>10^6 pixels/event)

Preliminary Telescope Results



Toward a Low Mass Ladder Detector Module

- **Demonstrated: thin CMOS, tracking OK**
- **Next step: integration into light, stable support structure**



The STAR Heavy Flavor Tracker

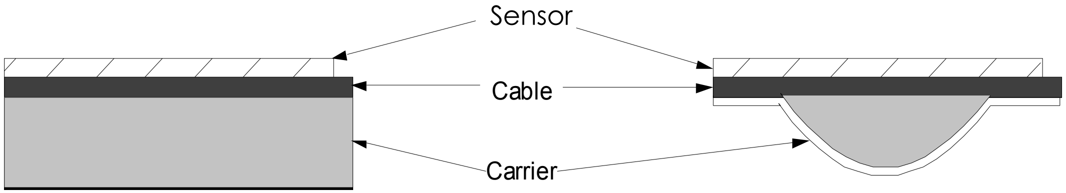
- Template provided by STAR group @ LBL (**S**olenoidal **T**racker **at** **R**HIC)
  - QGP experiment at Brookhaven
  - Heavy Flavor Tagger identifies low p_T secondary particles from charm production in heavy ion collisions→requires ultra-low material budget to minimize multiple scattering
- STAR has chosen thin CMOS on light-weight ladders → achieved lowest material budget ladder structures to date. Use STAR as template, further reduce material budget.

The STAR Detector Module

Component	Thickness (% X_0)
CMOS Sensor	0.053
Adhesive	0.014
Cable	0.090
Adhesive	0.014
Support Carrier	0.110
Total	**0.282**

3 Components integrated in module

- Sensor: thin CMOS
- Cable: data transfer, clock/control, power, ground
- Carrier: RVC/carbon fiber



2 Prototype Designs

- Detector is **< 20%** of module thickness
- STAR has achieved **< 0.3% X_0 / layer**
- **ILC VTX requires factor ~3x thinner**

ILC Ladder Studies Underway

Funding approved for LCRD project

- STAR ladder → prototype meeting ILC requirements
- Reduce material budget of support carrier, eliminate cabling using chip stitching
- Characterize mechanical deformation due to thermal effects from power cycling

Current Design

- Support: beryllium sandwiched around carbon fiber
- Finite Element Analysis (FEA) underway, prototyping next year
- Outlook: integrate thin CMOS chips, test module using telescope at 1.5 GeV e^- beam

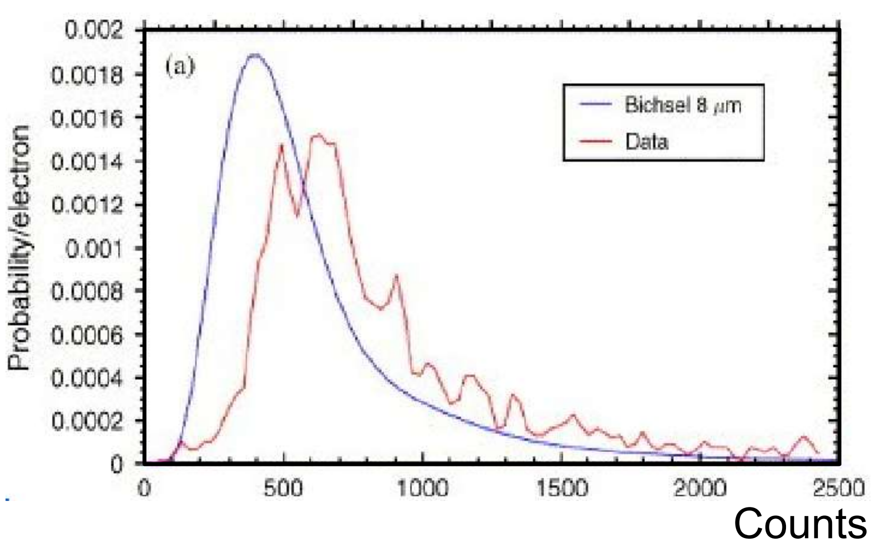
Conclusions and Outlook

- Successful thinning of CMOS sensors to $\leq$50 μm demonstrated with no appreciable performance loss
- Beam telescope with thin CMOS sensors designed, built and commissioned at ALS 1.5 GeV e^- test beam
- Recently approved LCRD funds for vertex ladder engineering, studies underway
- Characterize ladders with pixel telescope
- (generation → simulation → reconstruction) full software chain complete, use in future R&D effort

Previous Back-Thinning Studies***

STAR

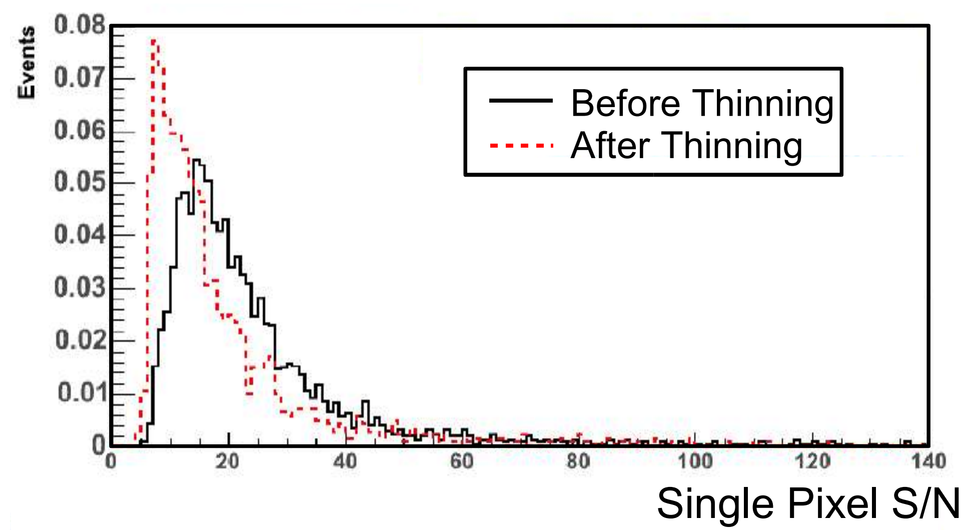
- Compare beam test data with Bichsel simulation assuming 8 μm epi-layer
- Indication of significant signal from bulk silicon



S Kleinfelder *et al.*, NIM A565 (2006),132-138

SUCIMA

- Compare beam test data pre/post thinning to 15 μm (use epi-layer as etch stop)
- Significant signal loss: less reflection at epi-substrate boundary?



W Dulinski *et al.*, NIM A546 (2005) 274-280

Experimental Setup***

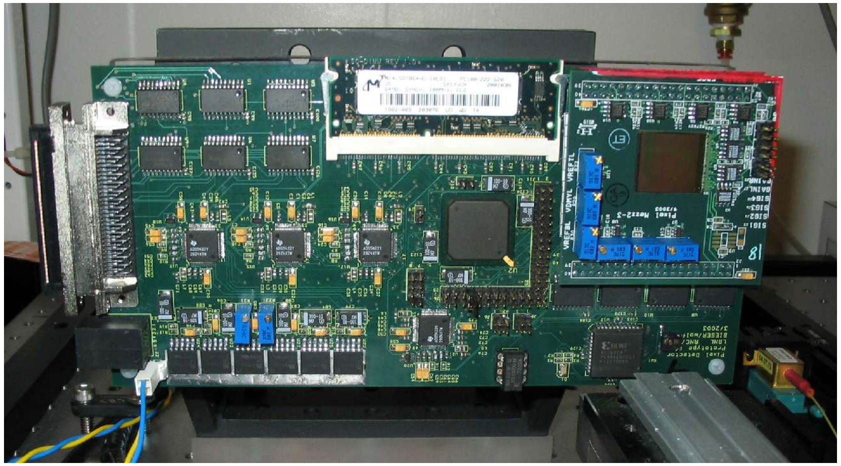
Chip is mounted to mezzanine card, mezzanine card is mounted to motherboard

MimosaV Prototype Chip

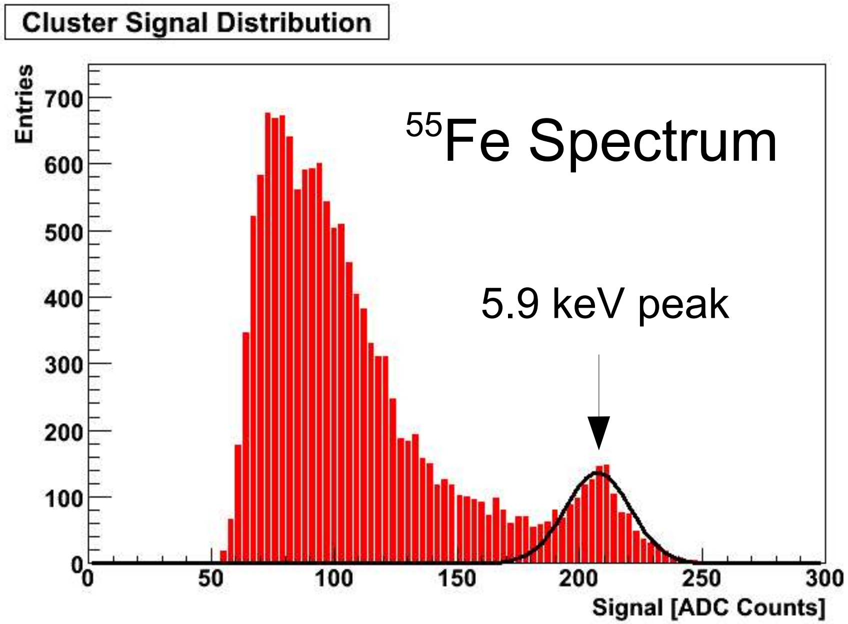
- produced at IPHC Strasbourg w/ 0.6 μm AMS CMOS process
- > 1 million pixels, 1.7 x 1.7 cm^2 active area (large)
- 14 μm epitaxial layer, 17 μm pixel pitch, 450 μm thick
- 4 independent sectors of 512 x 512 pixels, analog output

Motherboad

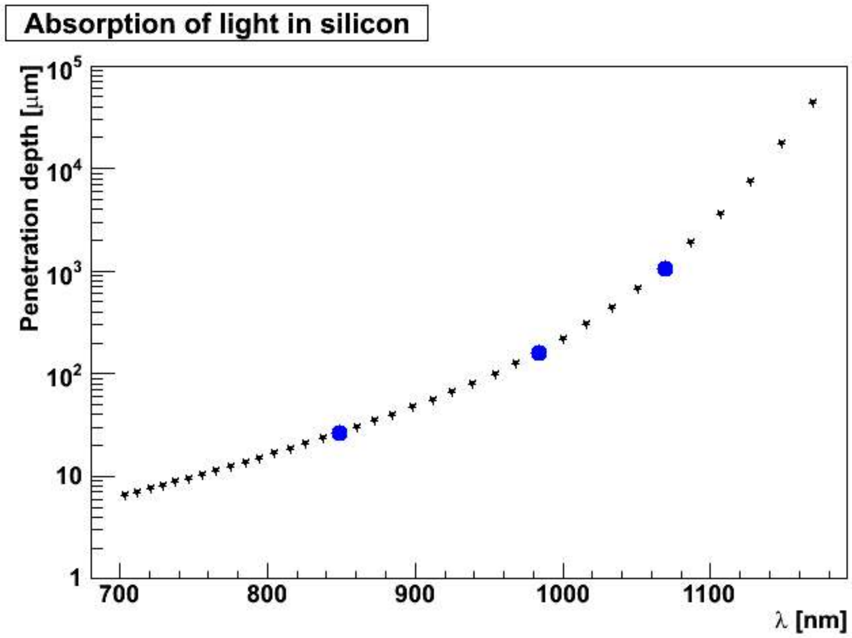
- custom board produced at LBNL
- Programmable Xilinx FPGA
- On-board 14-bit ADC's



Characterization Tools***



- When 5.9 keV X-ray from ^{55}Fe converts in shallow depletion region nearly 100% of generated charge reaches collection diode.
- 5.9 keV / 3.6 eV average ionization energy = 1640 electrons/ X-ray
- 1640 electrons / 207 counts gives calibration of ~8 electrons/ADC count



- Penetration depth of photons in silicon is strongly dependent on wavelength in range 850-1300 nm
- 850 nm: ~10 μm depth probes only epitaxial layer
- 1060 nm: ~1000 μm depth allows photon to pass through entire detector

Back-Thinning Procedure***

Step 1: Attach chip to mezzanine card with removable WaferGrip adhesive (characterize)

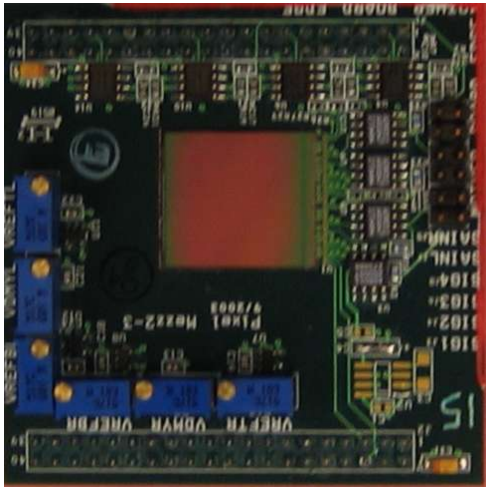
Step 2: Remove glue by placing in heated solvent

Step 3: Back-thinning

Step 4: Re-attach chip to mezzanine card with permanent glue (re-characterize)

Chip	Status	Results
5	thinned to 50 μm	Electrically functional
14	thinned to 50 μm	Not electrically functional (scratch)
16	thinned to 50 μm	Electrically functional, gain changed
15	thinned to 50 μm	4 sectors characterized pre/post thinning
18	thinned to 40 μm	3 sectors characterized pre/post thinning
19	awaiting thinning	4 sectors characterized pre thinning

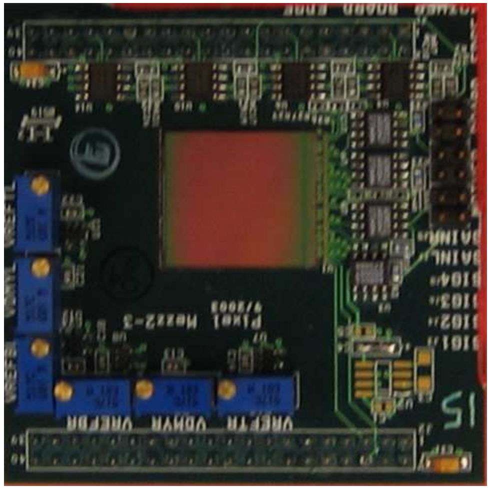
1



2

3

4



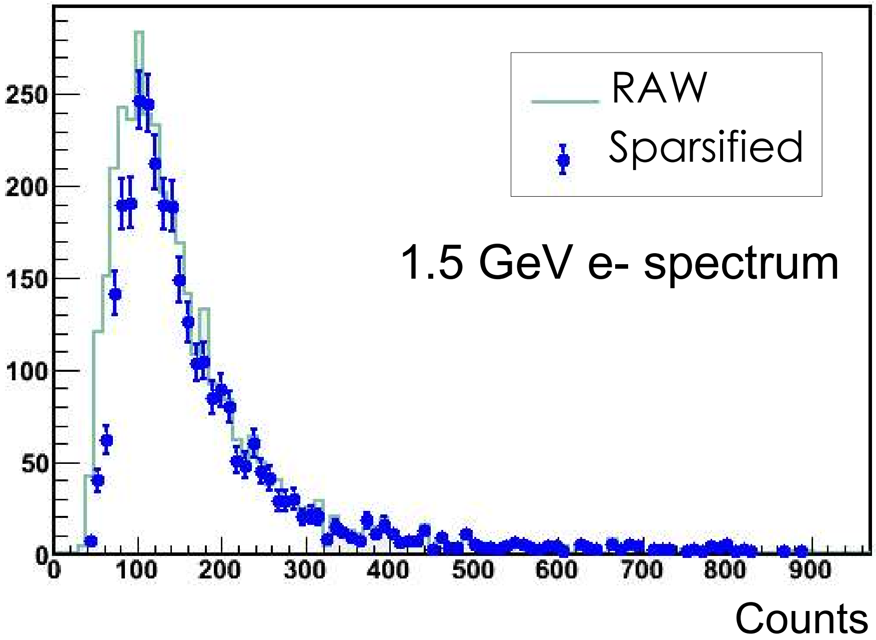
Online Data Sparsification***

Problem

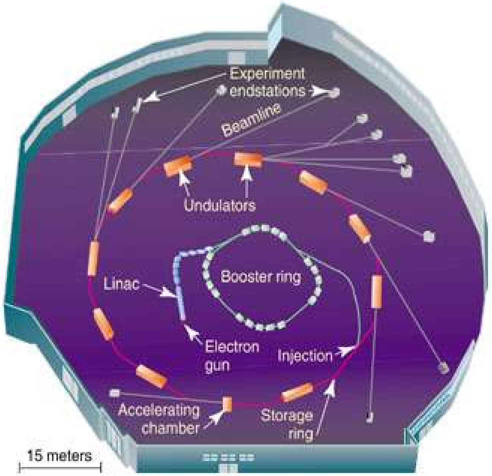
- Current configuration: [1 million pixels/event]×[14 bits/pixel]×[1Hz] = 1.75 Mb/s
- Require 10Hz → **17.5 Mb/s too much**

Solution: Data Sparsification

- Seed threshold + form factor cut + cluster shape cut
- Each cluster: 1 long (32 bits) seed pixel index
  + 9 ints (14 bits each) for signals on 3×3 cluster
- [~100 clusters/event]×[(32+9×14) bits/cluster]×[10Hz]
  ≈ 20 kB/s → **~100x reduction!**
- Currently on-line → on-board FPGA → on-chip
- Comparison of data with and without sparsification gives good agreement

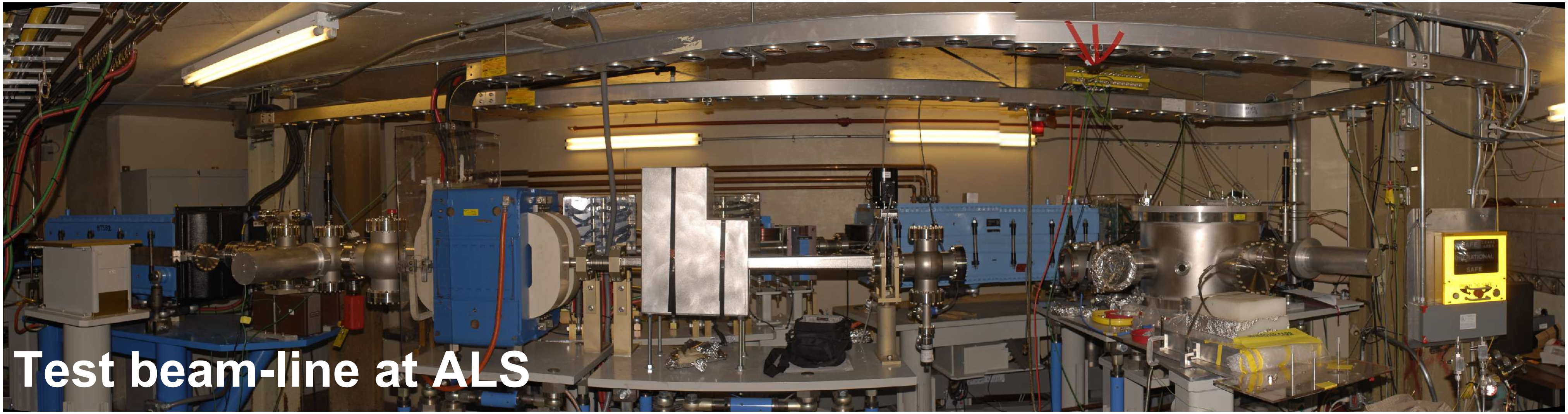


Test Beam Facility***



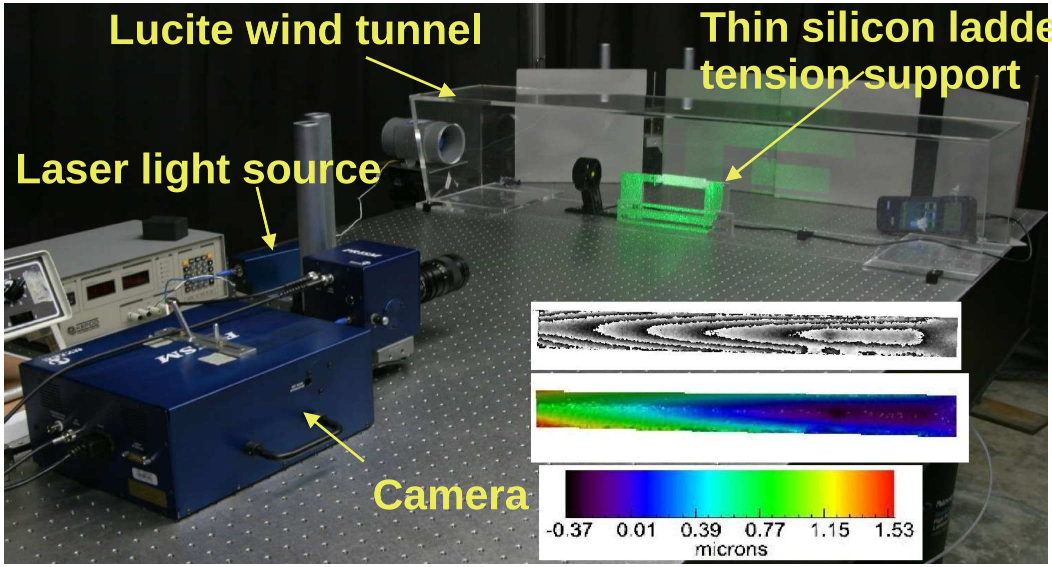
1.5 GeV e^- beam

- Test beam-line extracted from booster ring at Advanced Light Source LBNL
- Data synchronized with 1 Hz extraction cycle
- 2 frames after reset, CDS



Test beam-line at ALS

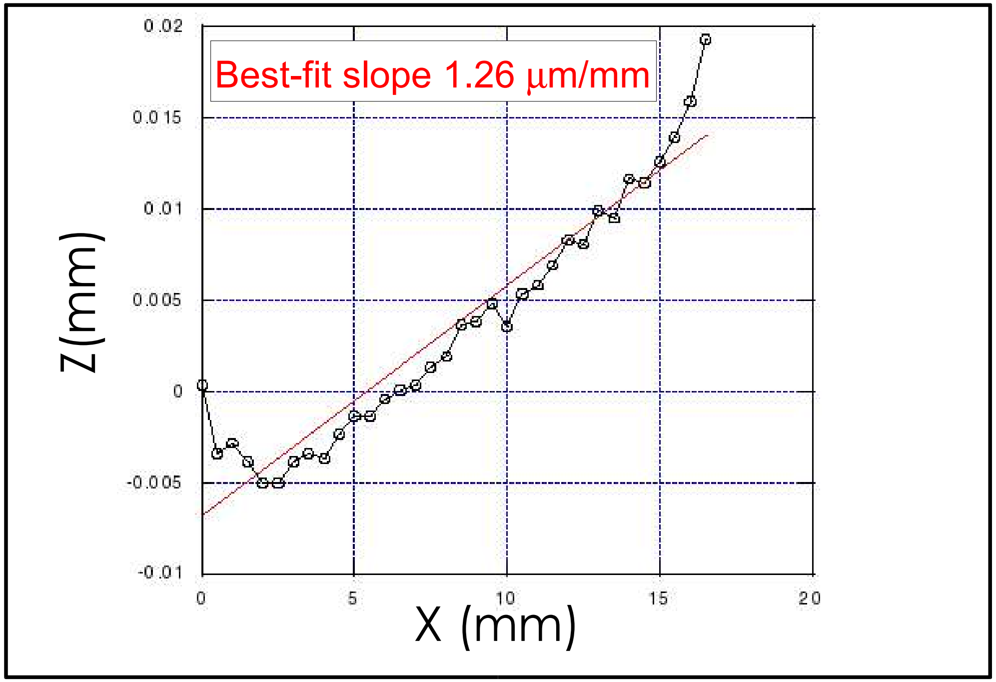
Test Facilities for Ladder Studies***

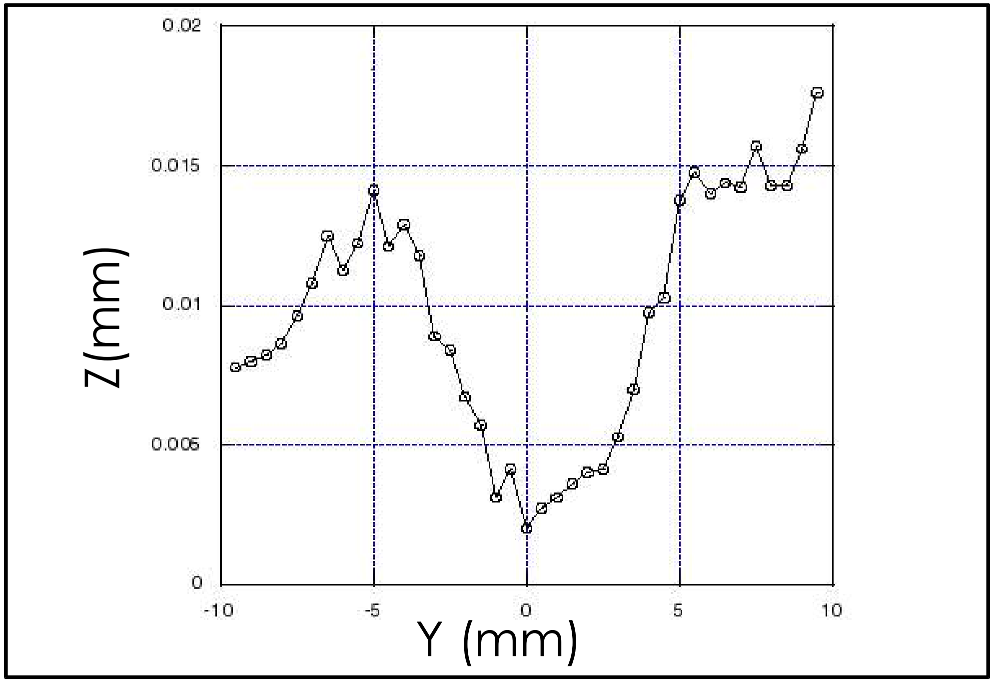


Extensive test facilities

- Environmental chamber (to -70º C): temperature/humidity effects on ladders
- High-res IR temperature probe: thermal properties of ladders
- Laser holography system: spatial distortions with sub-µm resolution
- Capacitive probe: displacements/vibrations
- Composite material lab: fabrication of light structures

Test Results from STAR on Si Flatness



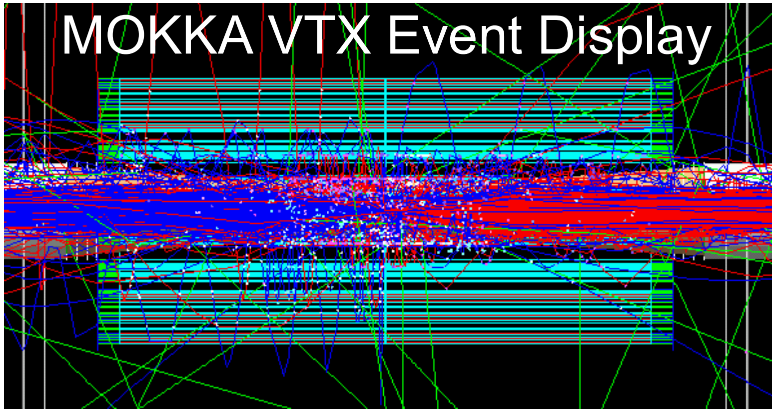


- 50 µm MimosaV chip glued to carrier/cable
- Measure height of chip as function of x, y at LBNL using laser holography
- Variations of 25 µm observed across chip surface
- Use parameterized functions to locate individual pixels

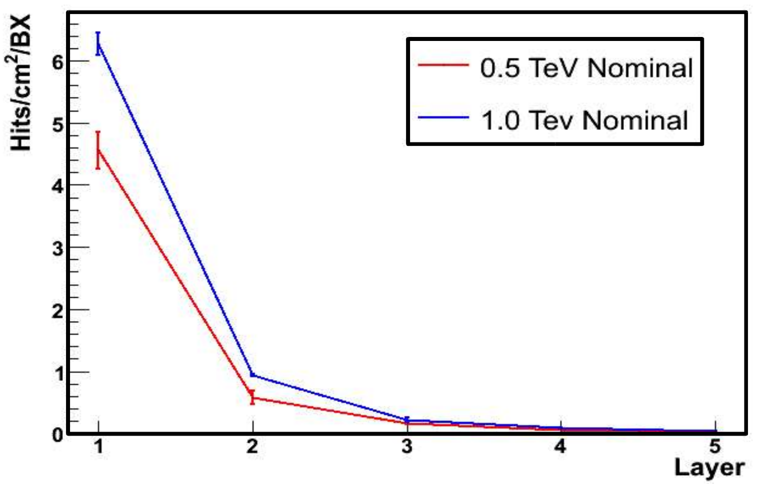
Pair Background Studies***

- 10 BX created with GuineaPig for ILC Nominal beam parameters at 0.5 TeV, 1.0 TeV
- Simulation in Mokka with LDC with CMOS VTX at B = 4T
- Reconstruction of pair background on VTX with Marlin
- Use cut: $|\cos\theta|<0.998$
- Simulation of high luminosity background, more detailed study underway

Beam Parameters	Pairs/BX [x 10^3]	Cut Pairs/BX [x 10^3]
0.5 TeV Nominal	77±1	17±0.2
1.0 TeV Nominal	143±4	25±0.4



electrons positrons photons VTXhits

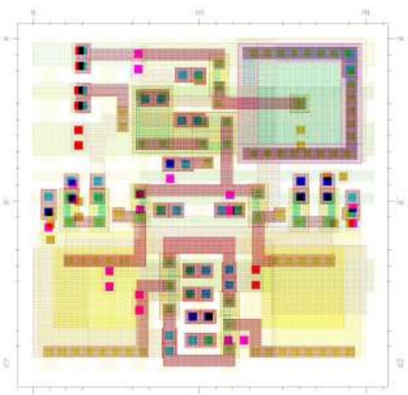


Ben Hooberman
DPF2006

Future R&D at LBNL

3 lines of R&D on monolithic pixel sensors

- Implement functionality on-chip for CMOS
  - In-pixel CDS $\rightarrow$ LDRD2 (fast read-out, 6 sectors)
  - On-chip ADC's $\rightarrow$ LDRD3 (5 bits, fast read-out, low power dissipation)
  - On-chip data sparsification
- Fully digital CMOS sensor with time-stamping capability using IBM 0.13 mm triple-well process
- First prototype of active pixels using Oki **S**ilicon **O**n **I**nsulator process



LDRD-2 just arrived

- AMS 0.35 μm CMOS OPTO process from CMP
- ~2×2 mm^2, 20μm pitch
- 3-T vs. self-bias, 3×3 μm^2 vs. 5×5 μm^2 diode size