SOI technology and study on its dose effect

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KEK Detector Technology Project : [SOIPIX Group]

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http://rd.kek.jp/project/soi
Vertex detectors play an essential role in particle physics
- precise decay position measurements of the heavy quarks and leptons

Silicon On Insulator (SOI) is one of the techniques usable for future high energy experiments, space experiments and medicine.
- no bump bonding
- high resistive substrate for radiation detection and low resistive silicon layer for transistor formation; two silicon layers are separated by SiO2 Buried Oxide (BOX)
- can be very thin
Characteristics of the SOI transistors

- radiation hard
  ◆ no parasitic PNPN structure, therefore no latch-ups.
  ◆ thin active transistor, i.e. insensitive to SEU
- high speed and lower power consumption
SOI pixel detector design
Overview of our SOI

• Fully-Depleted CMOS SOI fabricated by OKI Electric Industry Co. Ltd.
  - commercial technology with 150nm rule
  - thin Si layer (~20nm) + metal gate
• OKI adopts Unibond wafers from SOITEC, France
  - Top Si: Cz, ~18Ωcm, p-type, ~40nm thickness
  - Buried Oxide (BOX): 200nm thickness
  - handle wafer: Cz, high-resistive with > 1kΩ
    • no type assignment, however, identified by I-V measurements, shown later.
    • original thickness 650μm, thinned to 350μm and plated with Al (200nm).
SOI wafer production (UNIBOND™, SOITEC)

1. Initial silicon wafers A & B
2. Oxidation of wafer A to create insulating layer
3. Smart Cut ion implantation induces formation of an in-depth weakened layer
4. Cleaning & bonding wafer A to the handle substrate, wafer B
5. Smart Cut - cleavage at the mean ion penetration depth splits off wafer A
6. Wafer B undergoes annealing, CMP and touch polish => SOI wafer complete
7. Split-off wafer A is recycled, becoming the new wafer A or B

Diagram:
- Wafer A
- Wafer B
- H⁺ ions in wafer A
- Si bulk
- SOI wafer
- New A
- New B
Diode TEG

Metal contact & p+ implant
I-V characteristics of the handle wafer

The substrate is N-type with a resistivity of $\sim 700\,\Omega\text{cm}$ and a carrier concentration of $\sim 6 \times 10^{12}\,\text{cm}^{-3}$.

The graphs show the current-voltage characteristics for different wafer widths ($w = 0.68, 10, 30\,\mu\text{m}$) and substrate regions.

- **n+ - BACK**: Measured at different wafer widths.
- **P+ - BACK**: Measured at different wafer widths.

The diagrams illustrate the behavior of the diodes under various biases.
• 2.5 x 2.5 mm$^2$ Chips
  – Transistor
    • p-MOS and n-MOS transistors of different parameters
    • the characteristics are measured
    • radiation test has been performed -> this talk
  – Circuit
    • preamp, Q2T etc.
  – Strip
    • Silicon strip sensor for studying its basic performance
  – pixel
    • 32 x 32 matrix of 20 x 20 $\mu$m$^2$ pixels
    • correlated double sample circuit
      – reset -> integrate -> readout

Next speaker
Pixel TEG

6" φ MPW wafer

2.5 mm (chip)

20 μm (pixel)
proton irradiation test of the transistor TEG

- 70MeV proton beam irradiation to the transistor TEG
  - CYRIC @ Tohoku U.
- up to $8 \times 10^{14} \text{ p/cm}^2$
- three different types of transistors are mounted.
  - HVT, LVT, I/O
  - NMOS and PMOS

<table>
<thead>
<tr>
<th>Transistor</th>
<th>$V_{DD}$ [V]</th>
<th>$V_{TH}$ [V]</th>
<th>$V_{DD}$ [V]</th>
<th>$V_{TH}$ [V]</th>
<th>$I/O$</th>
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<tbody>
<tr>
<td>HVT</td>
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<td>1.0</td>
<td>1.8</td>
<td>0.30</td>
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<tr>
<td>LVT</td>
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<td>5.0</td>
<td>0.30</td>
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<tr>
<td>I/O</td>
<td>2.5</td>
<td>2.5</td>
<td>5.0</td>
<td>0.30</td>
<td></td>
</tr>
<tr>
<td>NMOS and PMOS</td>
<td>0.4</td>
<td>0.2</td>
<td>0.5</td>
<td>0.30</td>
<td></td>
</tr>
</tbody>
</table>

Matrix of the transistors

Fig. 2 Transistor Matrix Circuit
proton irradiation test to the transistor TEG chip

- Total dose effect
  - positively charge trap in buried oxide (BOX)
  - changes the threshold voltage of the transistor
  - increases the leakage current of NMOS transistors

Threshold shifts of the transistors

\[ \Delta V_T \sim -0.1 \text{V} \]
for NMOS(LVT), PMOS(LVT, HVT)

\[ \Delta V_T \sim -0.2 \text{V} \]
for NMOS(HVT)
Leakage current of the transistors

Leakage currents were found to be

\[ \sim 100 \mu A \] for (LVT, HVT) Gate length = 0.15 \mu m

\[ \sim 30 \mu A \] for (LVT, HVT) Gate length \( \geq \) 0.15 \mu m
-23V back gate bias compensates the threshold voltage shift
5. Next Submission Plan

Next submission is our own Multi Project Wafer run.
Design Dead line ~ Dec. 5
Chip Delivery ~ End of Next March

!! Space is still available !!
2.5 x 2.5 mm² space ~ $18k
Summary

- We have started R&D for the SOI detector with OKI Elec. Ind. Co.
- 2.5 x 2.5 mm² TEG chips have been fabricated
  - transistor, circuit, strip and pixel
- Transistor TEG chip was irradiated by the proton beam up to $8 \times 10^{14}$ p/cm²
  - threshold shifts of -0.1~-0.2V
  - leakage current of NMOS increases by 30~100μA depending on gate length.
  - the back gate bias reduces the threshold voltage shift.
- New submission on Dec., 2006
backup
Pixel TEG

CMOS Active Pixel Sensor Type
20 μm x 20 μm
32 x 32 pixels
Window for Light Illumination
(5.4 x 5.4 \text{um}^2)

p+ junction

Storage Capacitance
(100 fF)
$V_{\text{break}} \sim 100\, \text{V}$

Hot Spot observed with infrared camera

$I = 40\, \mu\text{A}, \, T = 1\, \text{min}$

→ Smooth the corner and move the ring inward at next submission.