SOI technology and study on its dose effect

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SOIPIX group

KEK Detector Technology Project : [SOIPIX Group]

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http://rd.kek.jp/project/soi

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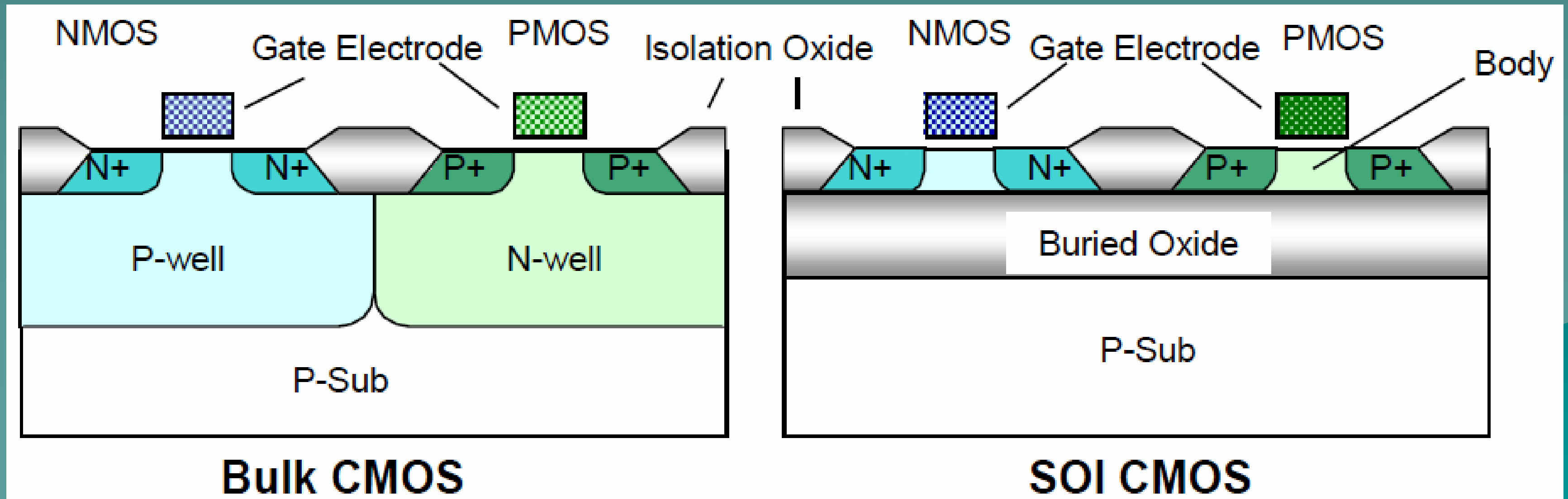
Motivation

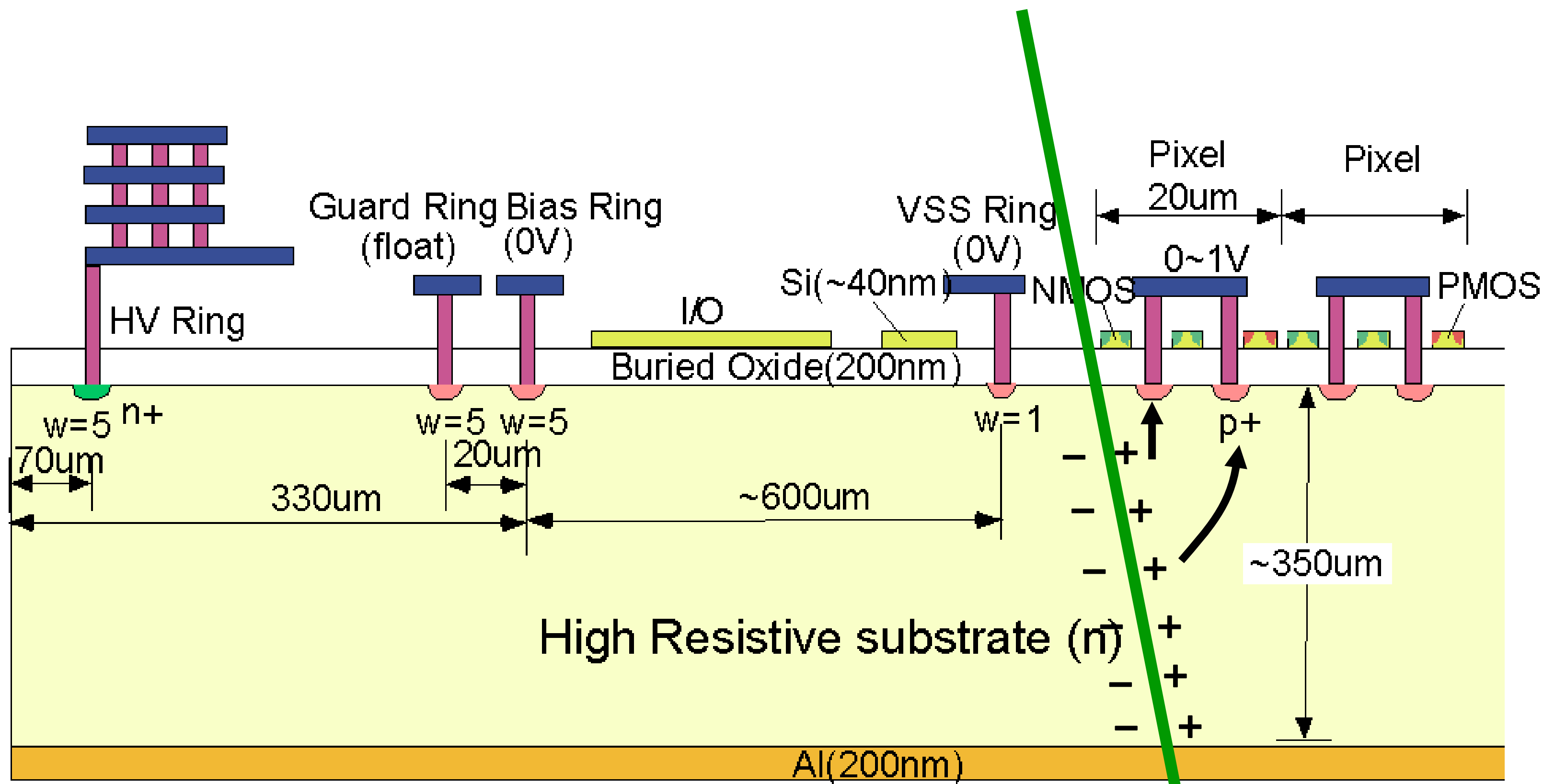
- Vertex detectors play an essential role in particle physics
  - precise decay position measurements of the heavy quarks and leptons
- Silicon On Insulator (SOI) is one of the techniques usable for future high energy experiments, space experiments and medicine.
  - no bump bonding
  - high resistive substrate for radiation detection and low resistive silicon layer for transistor formation; two silicon layers are separated by SiO_2 Buried Oxide (BOX)
  - can be very thin

Characteristics of the SOI transistors

- radiation hard
  - ◆no parasitic PNPN structure, therefore no latch-ups.
  - ◆thin active transistor, i.e. insensitive to SEU
- high speed and lower power consumption



SOI pixel detector design



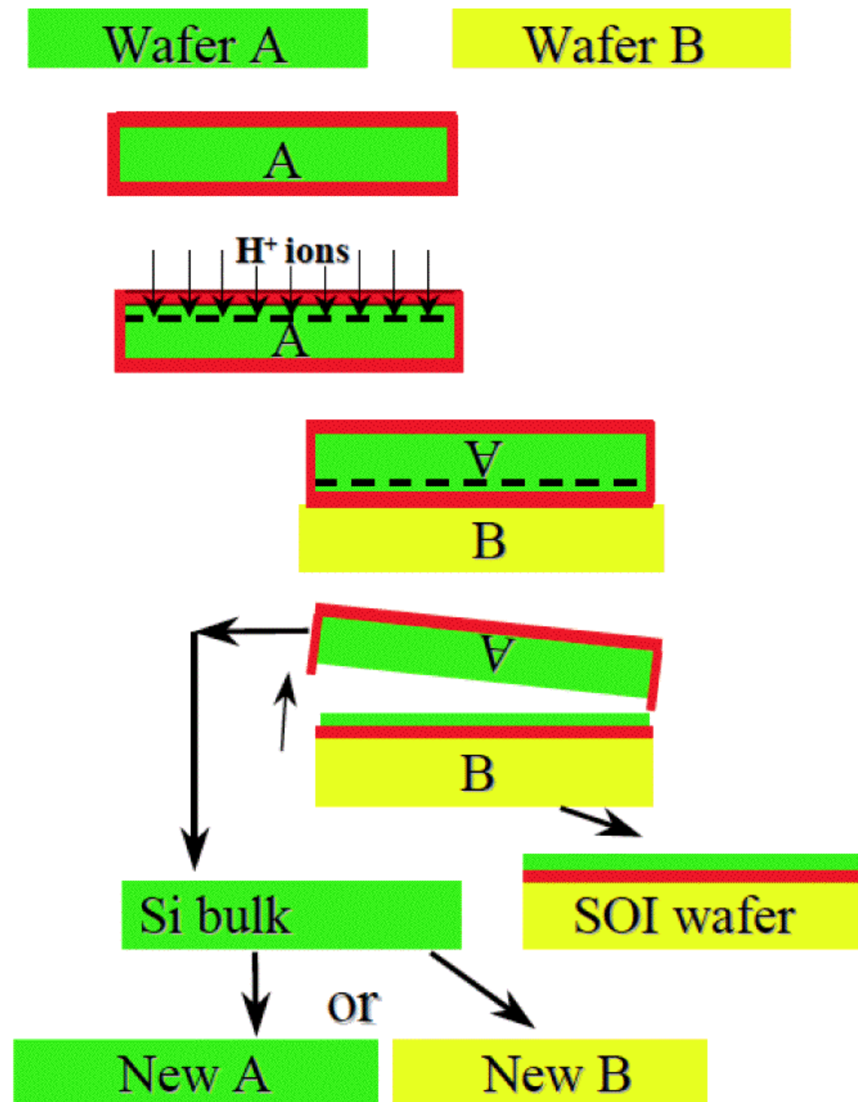
(This figure is not to scale)

Overview of our SOI

- Fully-Depleted CMOS SOI fabricated by OKI Electric Industry Co. Ltd.
  - commercial technology with 150nm rule
  - thin Si layer (~20nm) + metal gate
- OKI adopts Unibond wafers from SOITEC, France
  - Top Si: Cz, ~18Ωcm, p-type, ~40nm thickness
  - Buried Oxide (BOX): 200nm thickness
  - handle wafer: Cz, high-resistive with > 1kΩ
    - no type assignment, however, identified by I-V measurements, shown later.
    - original thickness 650μm, thinned to 350μm and plated with Al (200nm).

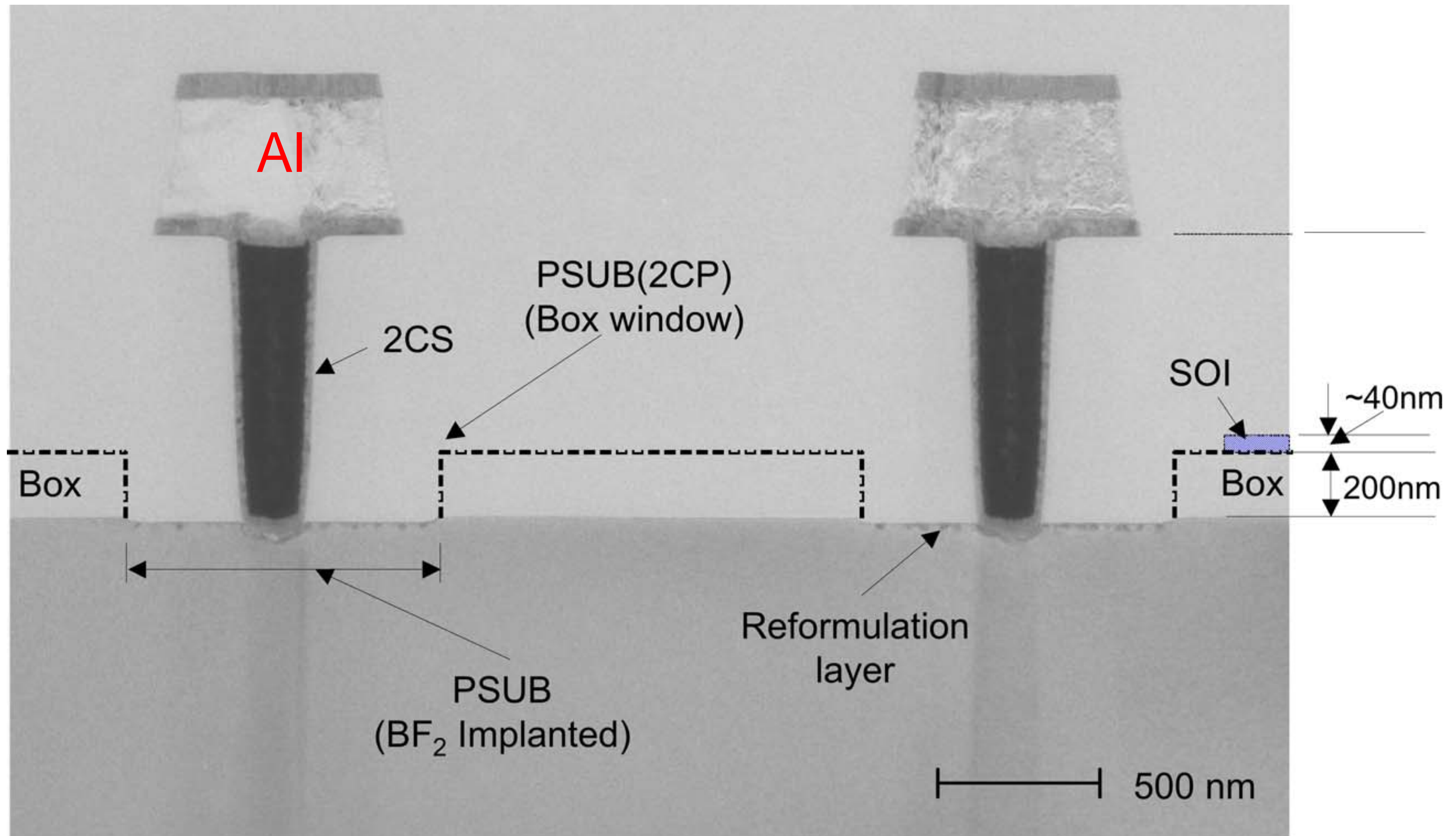
SOI wafer production (UNIBOND™, SOITEC)

1. Initial silicon wafers A & B
2. Oxidation of wafer A to create insulating layer
3. Smart Cut ion implantation induces formation of an in-depth weakened layer
4. Cleaning & bonding wafer A to the handle substrate, wafer B
5. Smart Cut - cleavage at the mean ion penetration depth splits off wafer A
6. Wafer B undergoes annealing, CMP and touch polish => SOI wafer complete
8. Split-off wafer A is recycled, becoming the new wafer A or B

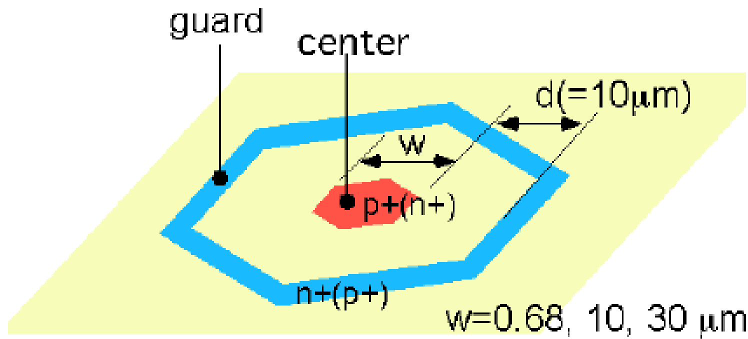


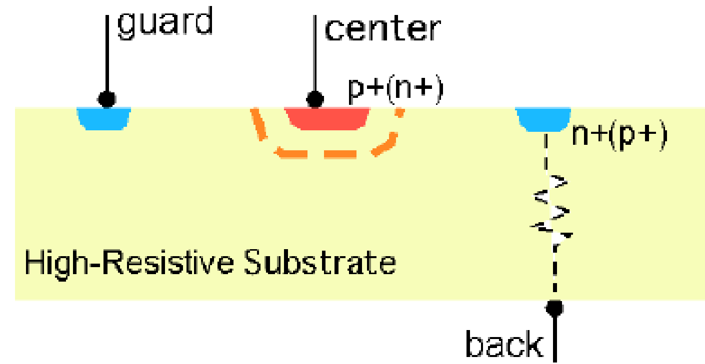
Diode TEG

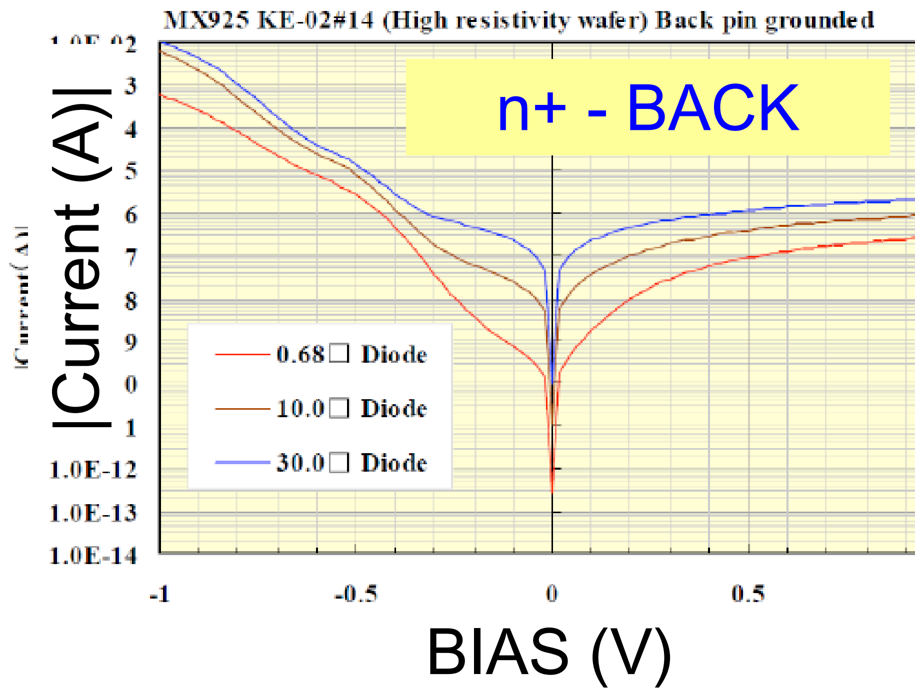
Metal contact & p+ implant

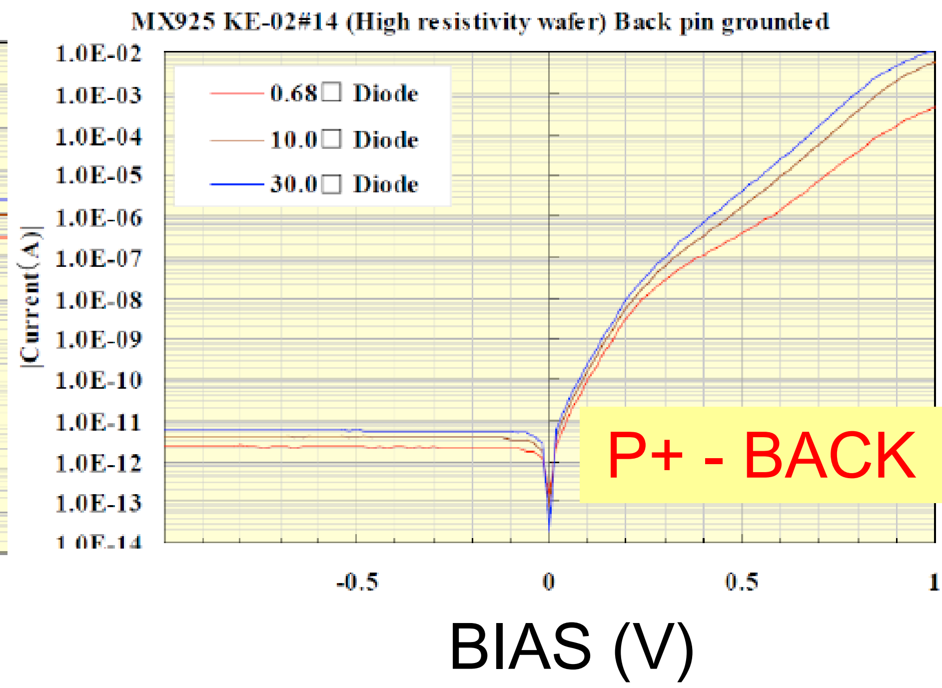


I-V characteristics of the handle wafer









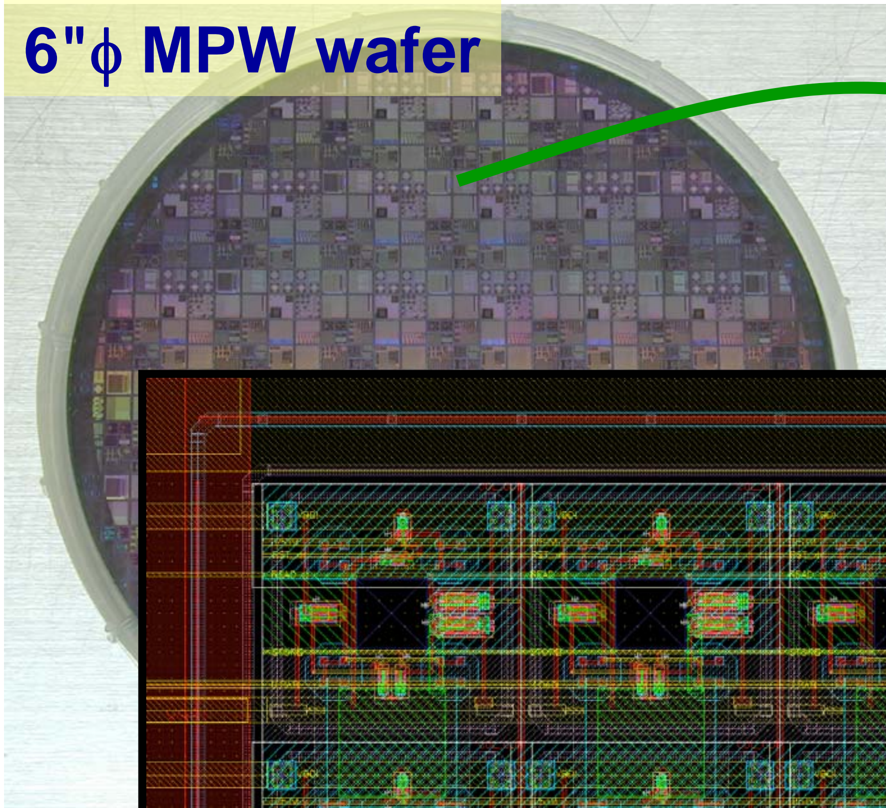
substrate is N-type ~700Ωcm ~6×10^{12} cm^{-3}

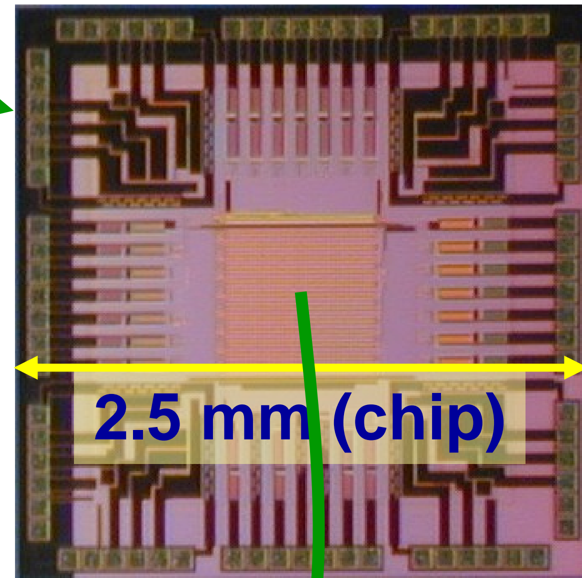
SOI TEG submitted in 2005

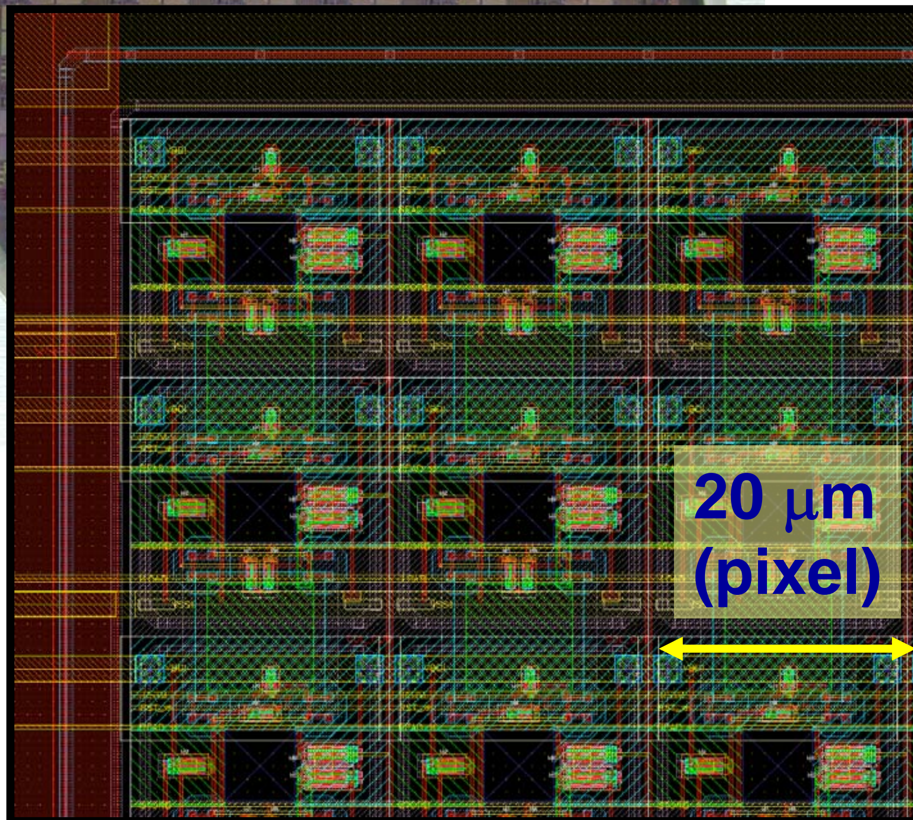
- 2.5 x 2.5 mm^2 Chips
  - Transistor
    - p-MOS and n-MOS transistors of different parameters
    - the characteristics are measured
    - radiation test has been performed -> this talk
  - Circuit
    - preamp, Q2T etc.
  - Strip
    - Silicon strip sensor for studying its basic performance
  - pixel
    - 32 x 32 matrix of 20 x 20 μm^2 pixels
    - correlated double sample circuit
      - reset -> integrate -> readout

Next speaker

Pixel TEG

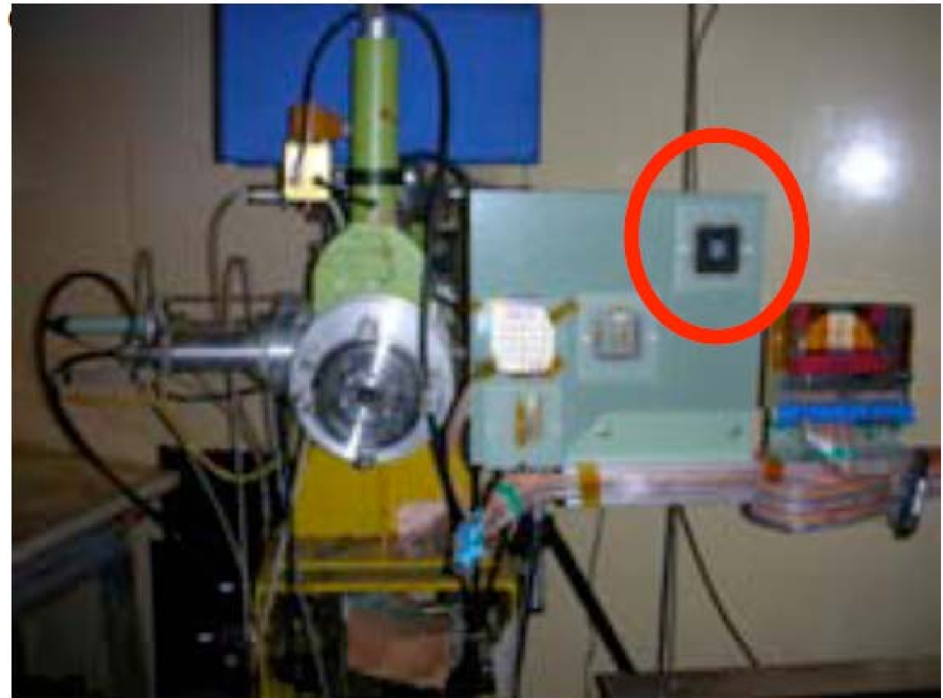






proton irradiation test of the transistor TEG

- 70MeV proton beam irradiation to the transistor TEG
  - CYRIC @ Tohoku U.
- up to 8 x 10^{14} p/cm^2
- three different types of transistors are mounted.
  - HVT, LVT, I/O
  - NMOS and PMOS



Transistor		Basic Logic HVT	Low V_{TH} LVT	I/O IO
V_{DD}	[V]	1.0	1.0	1.8
Gate Length	[µm]	0.14	0.14	0.30
Gate Oxide	[nm]	2.5	2.5	5.0
V_{TH}	[V]	0.4	0.2	0.5

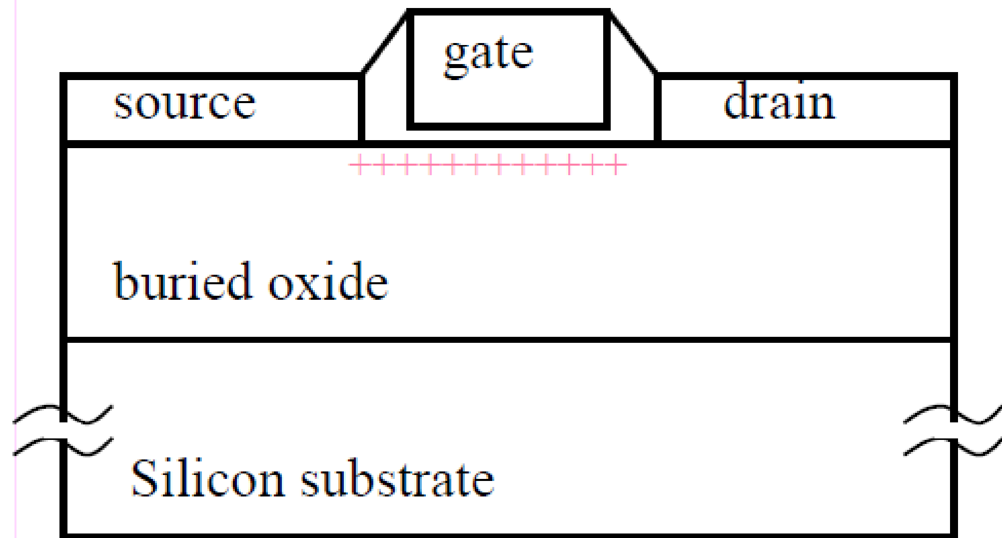
Ref. http://www.oki.com/en/otr/196/downloads/otr-196-R15.pdf

Matrix of the transistors

Fig.2 Transistor Matrix Circuit

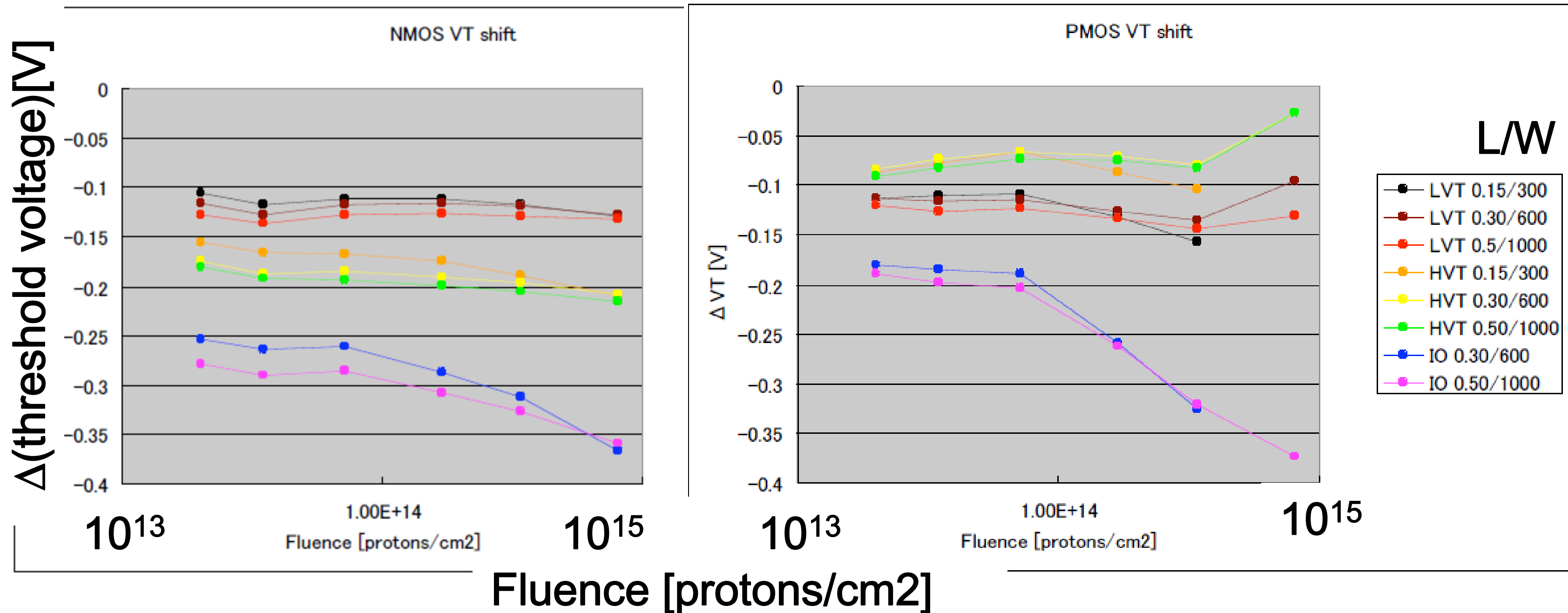
proton irradiation test to the transistor TEG chip

- Total dose effect
  - positively charge trap in buried oxide (BOX)
  - changes the threshold voltage of the transistor
  - increases the leakage current of NMOS transistors



Ref. IEEE Trans. on Nucl. Sci. Vol. 35, p.1529, 1988

Threshold shifts of the transistors



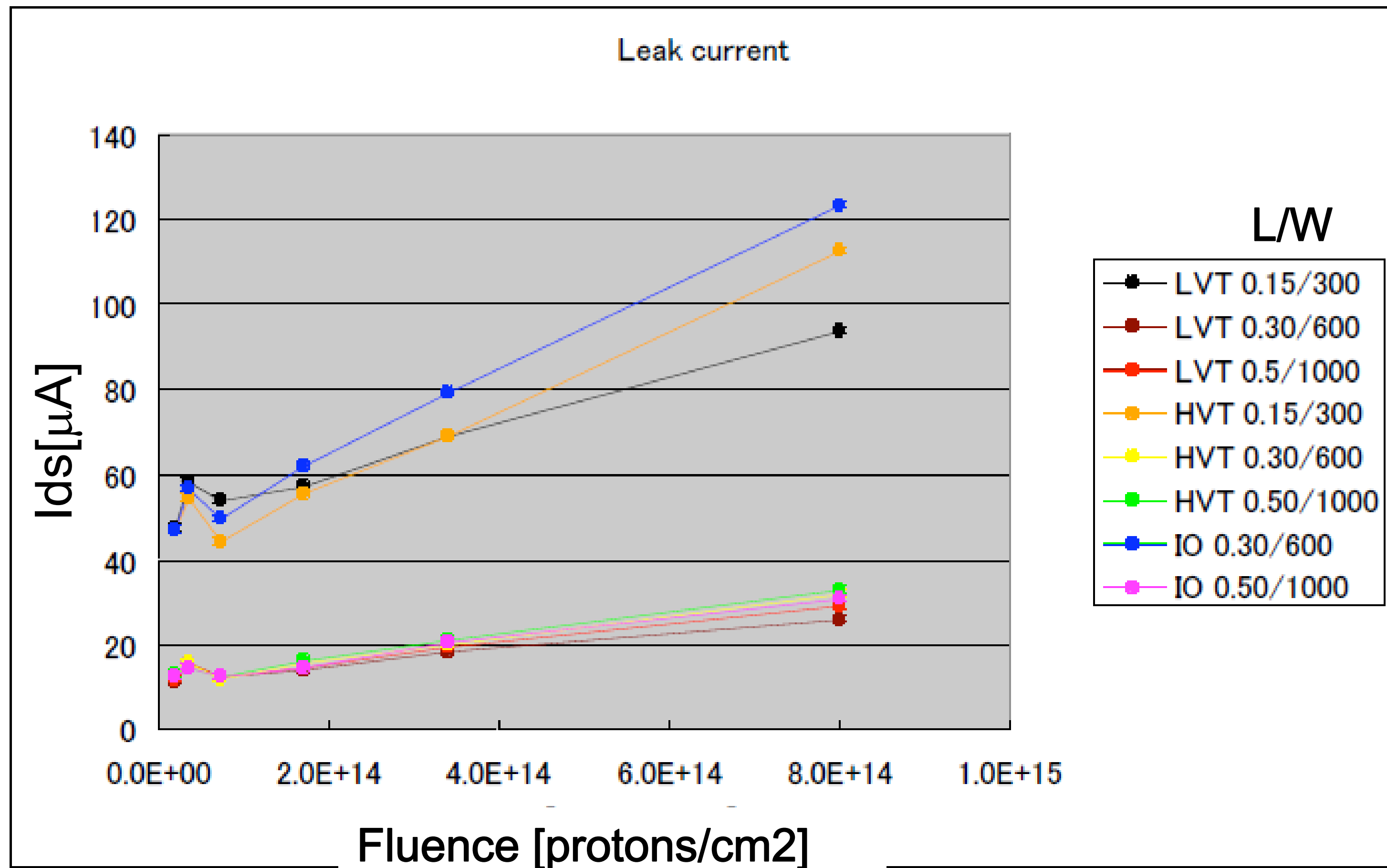
$\Delta V_T \sim -0.1V$

for NMOS(LVT), PMOS(LVT, HVT)

$\Delta V_T \sim -0.2V$

for NMOS(HVT)

Leakage current of the transistors



Leakage currents were found to be

~ 100μA for (LVT, HVT) Gate length = 0.15μm

~ 30μA for (LVT, HVT) Gate length > 0.15μm

Back gate bias compensation

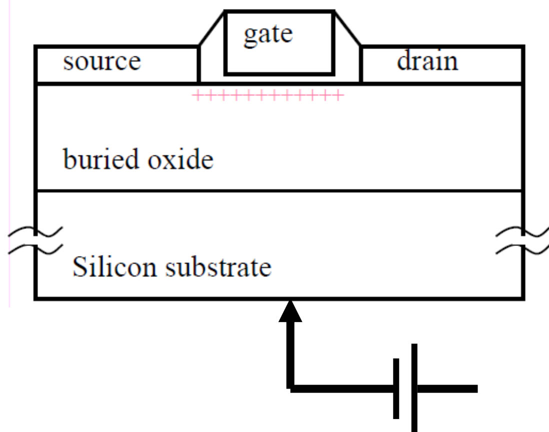
ΔV[V]

0.4
0.3
0.2
0.1
0
−0.1
−0.2
−0.3
−0.4

−30 −25 −20 −15 −10 −5 0

Back gate[V]

NMOS LVT
NMOS HVT
NMOS IO
PMOS LVT
PMOS HVT
PMOS IO



-23V back gate bias compensates the threshold voltage shift

5.Next Submission Plan

Next submission is our own Multi Project Wafer run.

Design Dead line ~ Dec. 5

Chip Delivery ~ End of Next March

!! Space is still available !!

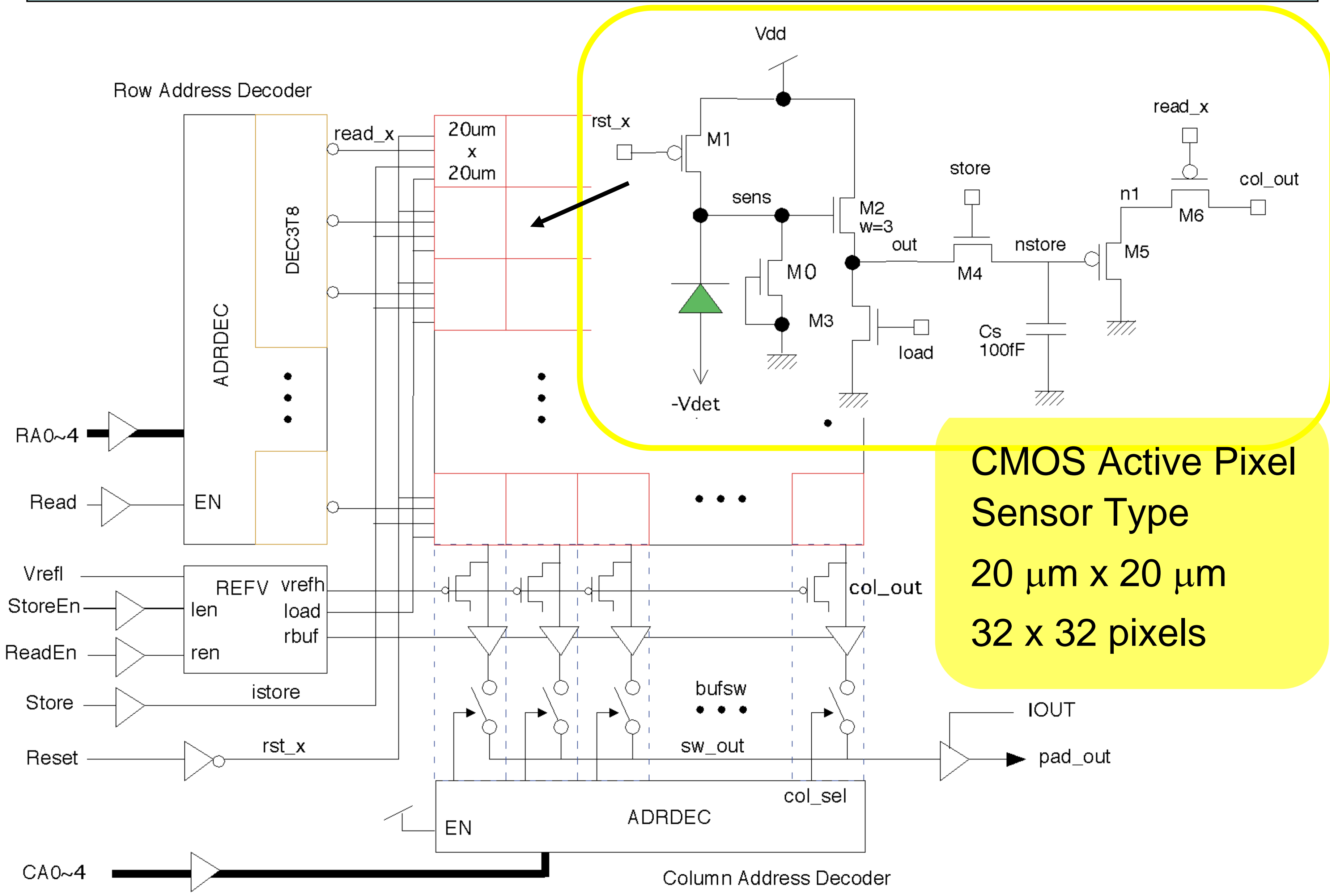
2.5 x 2.5 mm^2 space ~ $18k

Summary

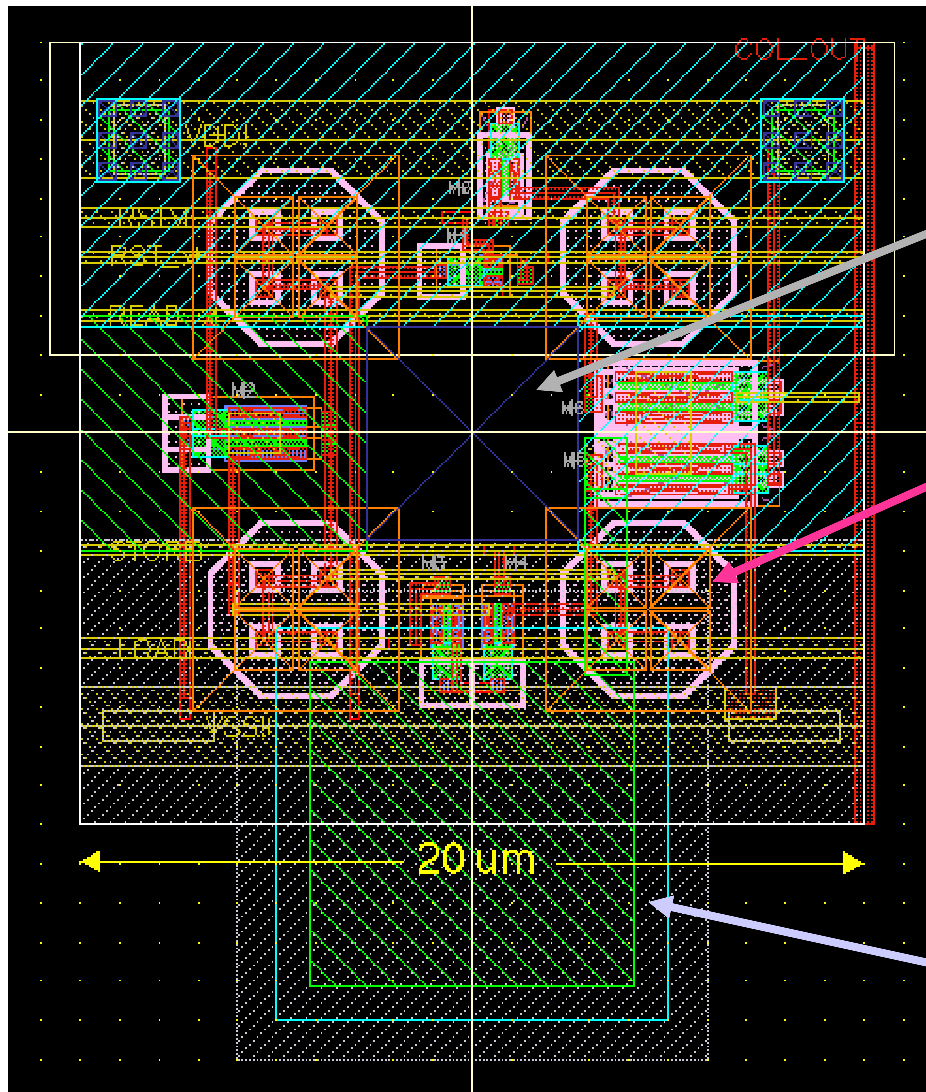
- We have started R&D for the SOI detector with OKI Elec. Ind. Co.
- 2.5 x 2.5 mm^2 TEG chips have been fabricated
  - transistor, circuit, strip and pixel
- transistor TEG chip was irradiated by the proton beam up to 8 x 10^{14} p/cm^2
  - threshold shifts of -0.1~-0.2V
  - leakage current of NMOS increases by 30~100μA depending on gate length.
  - the back gate bias reduces the threshold voltage shift.
- New submission on Dec., 2006

backup

Pixel TEG



Pixel layout



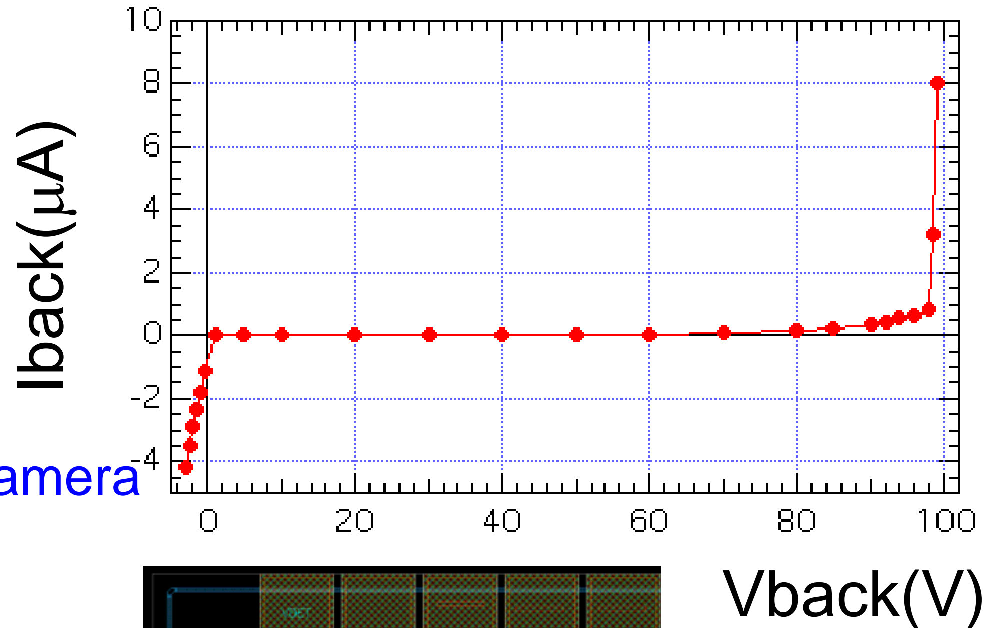
Window for Light Illumination ($5.4 \times 5.4\ um^2$)

p+ junction

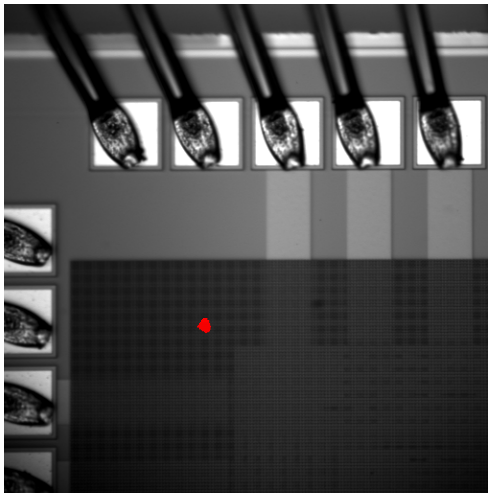
Storage Capacitance (100 fF)

Pixel IV character

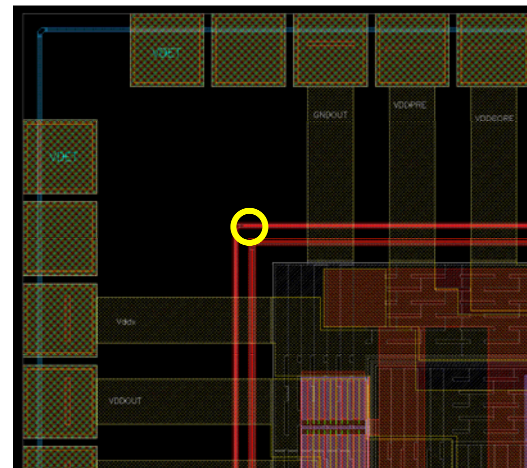
V_{break} ~ 100 V



Hot Spot observed with infrared camera

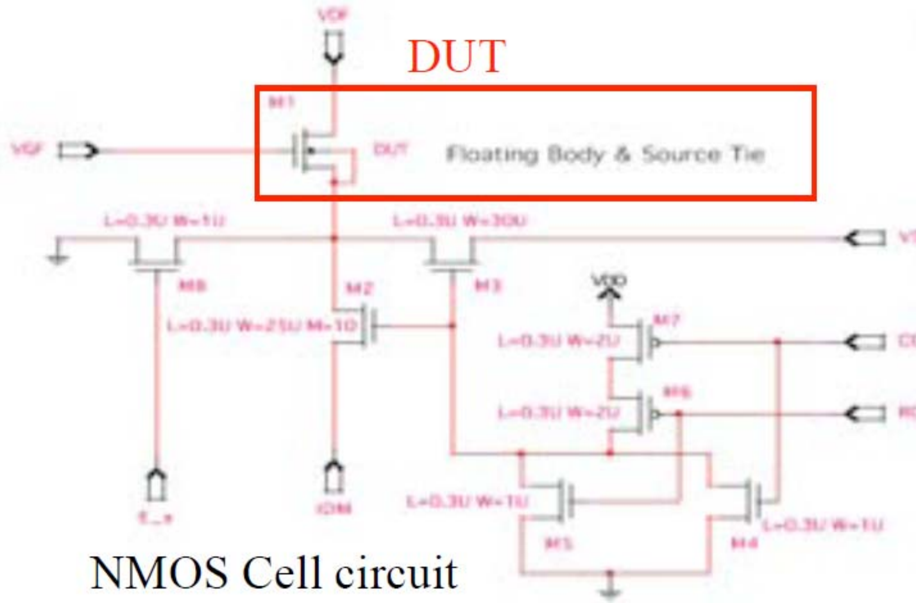


I = 40 μA, T = 1 min

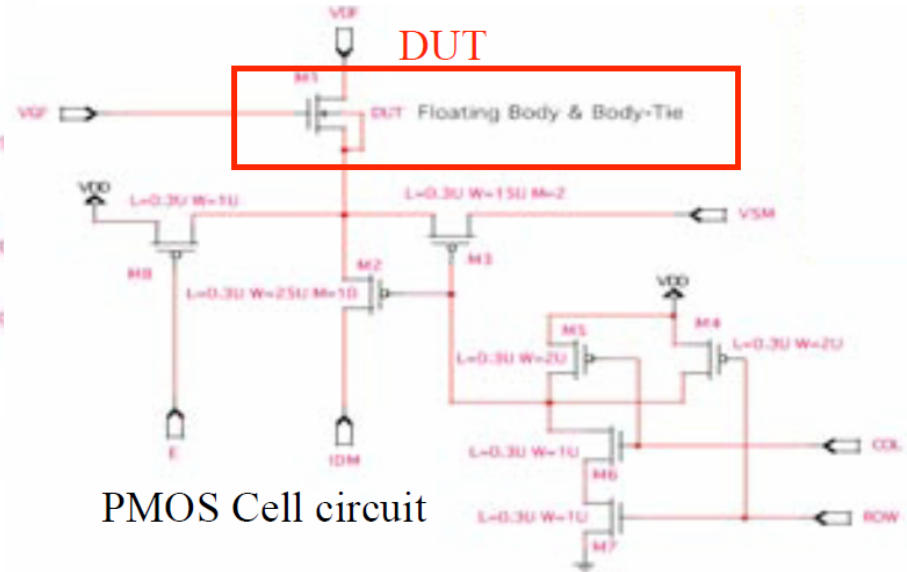


corner of the bias ring

→ Smooth the corner and move the ring inward at next submission.



NMOS Cell circuit



PMOS Cell circuit