Global Decision Logic

Y. Iwasaki (KEK)
2012 TRG/DAQ Workshop
@
Univ. Hawaii

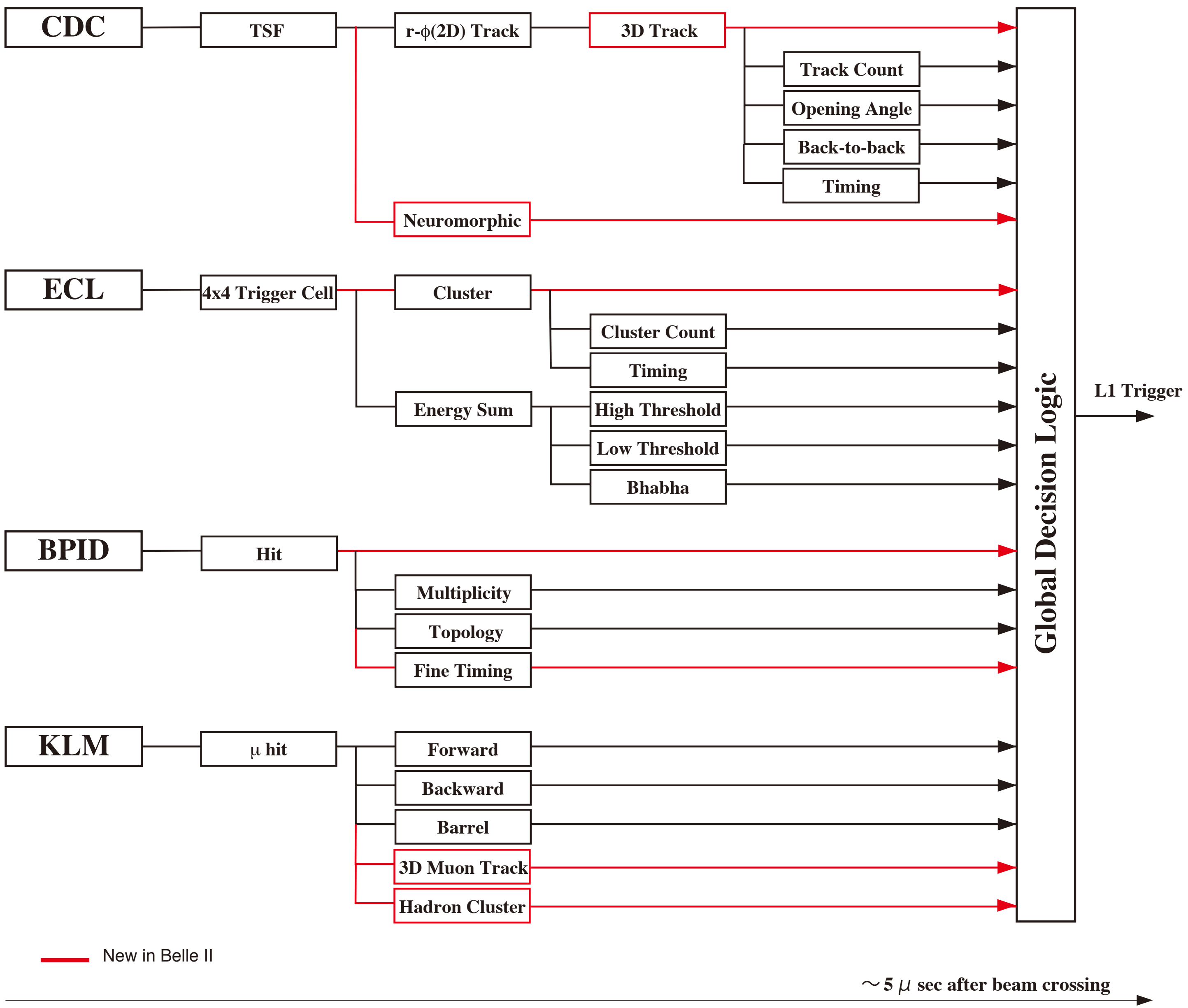
Sub-Triggers

Korea U.
National United U.
Fu Jen Catholic U.
Univ. Heidelberg
KEK

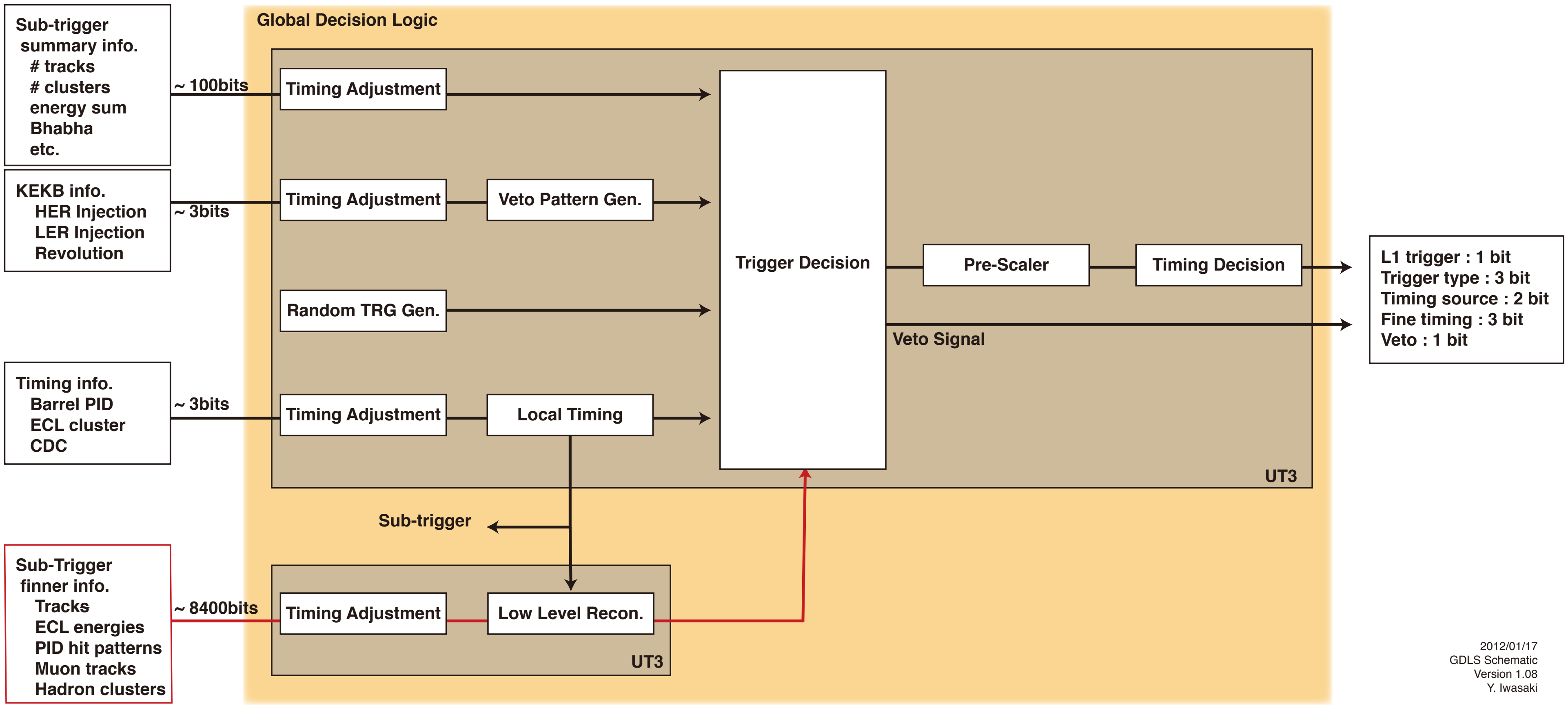
Hanyang U.
Seoul National U.

Hawaii U.

Virginia Tech
Hawaii U.



GDL



2012/01/17
GDLS Schematic
Version 1.08
Y. Iwasaki

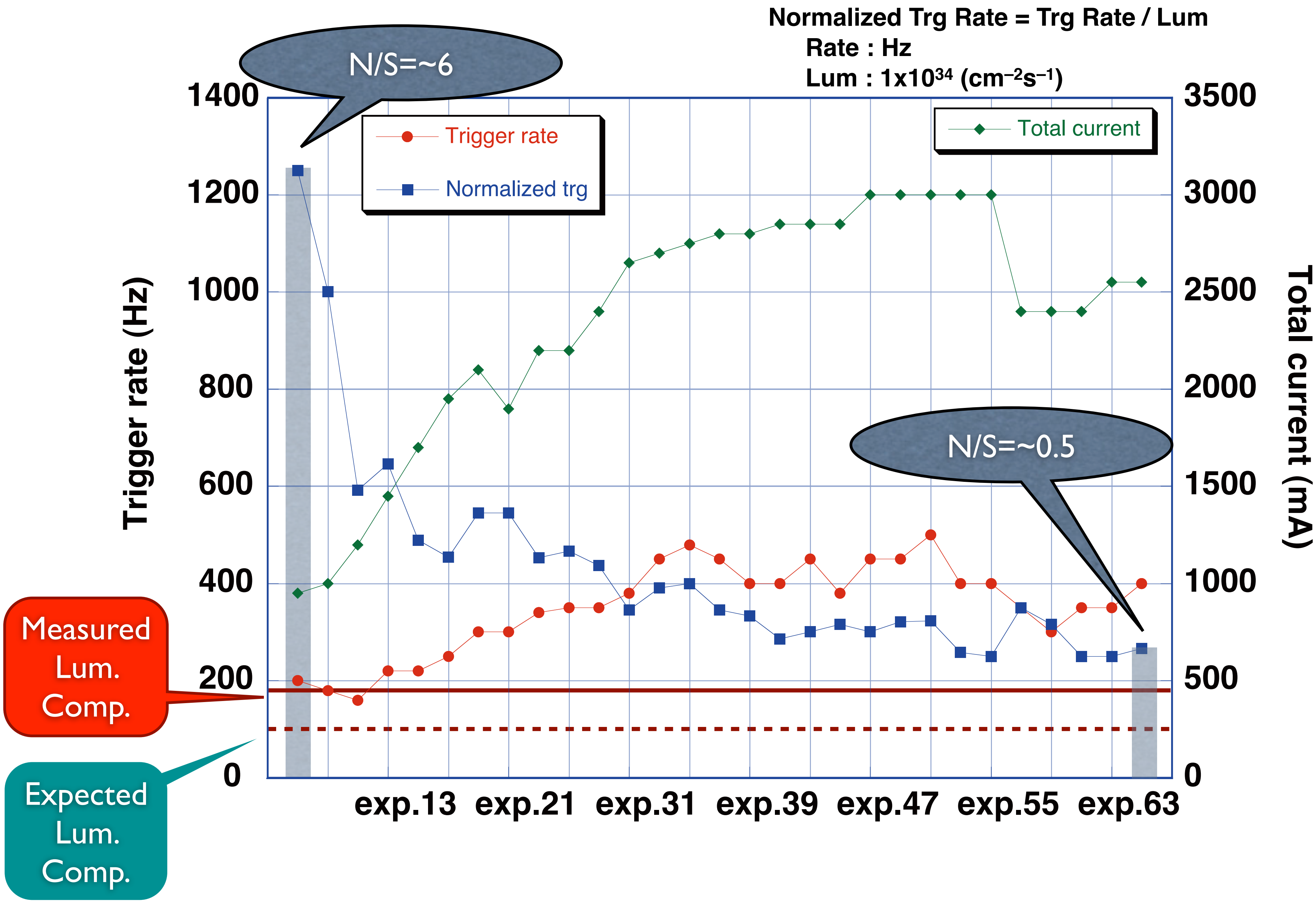
GDL Output

- Level 1 trigger : 1 bit
  - Sent after the fixed latency from T_0 : 4.5 us (8ns * 562 clks)
  - Minimum distance between two triggers : ～200 ns (8ns * 24 clks)
  - Logical maximum rate : ～5MHz
    - The maximum trigger rate allowed is 30 kHz
- Trigger type : 3 bit
  - Physics, random,
- Timing source : 2 bit
  - BPID, ECL, CDC, GDL
- Fine timing : 3 bit
  - 1ns LSB
- Veto : 1 bit
  - KEKB injection veto
- All output
  - Driven by the DAQ system clock (～126MHz)
  - All output are aligned to the level 1 trigger

Strategy for TRG Commissioning

- **Before Belle-2 commissioning**
  - **Start TRG operation @ 2014**
  - **Develop monitoring and control tools**
  - **ECL, KLM, and GDL will have drill with BEAST-II**
- **Establish the basic logics**
  - **CDC 2D, total energy, isolated clusters, Bhabha, timing, injection veto, random trigger**
  - **Trigger performance should be checked in offline**
  - **New triggers will be turn on with large pre-scaling from the begining**
    - **CDC 3D, CDC neuromophic, KLM muon, etc**
- **If the trigger rate is too high**
  - **Use large pre-scaling before establishing basic logics**
  - **Then tune up trigger logics to reduce the backgrounds**

TRG History in Belle



TRG Rate Estimation

Based on Belle History

Lum ($cm^{-2}s^{-1}$)	Lum. Comp.	N/S=~0.5		N/S=~6	
		BG	Total	BG	Total
1×10^{34}	190 Hz	100 Hz	290 Hz	1100 Hz	1300 Hz
1×10^{35}	1.9 kHz	1.0 kHz	2.9 kHz	11 kHz	13 kHz
8×10^{35}	15 kHz	8 kHz	23 kHz	88 kHz	100 kHz

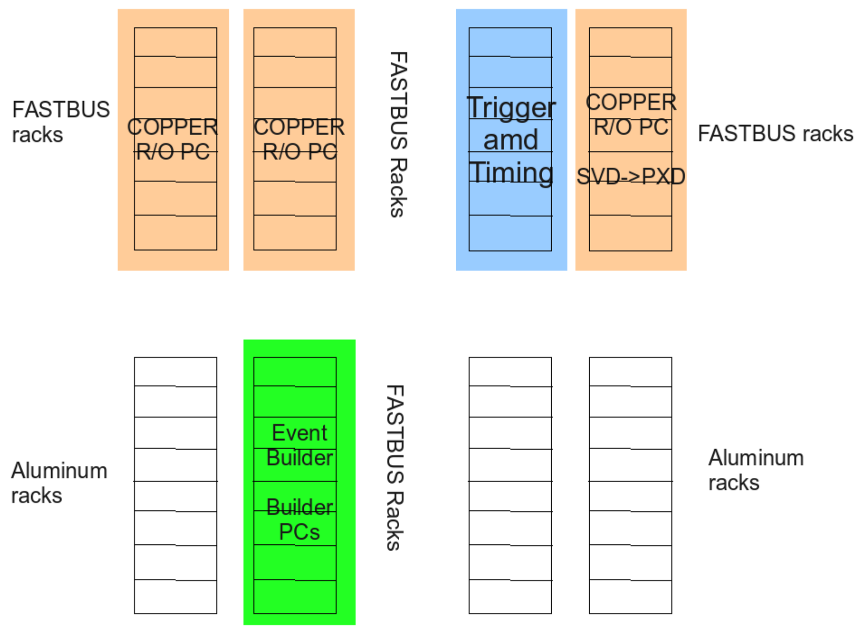
- **No reliable estimation**
  - **for the beam induced background**
  - **We will simulate it with TSIM when software is available**
- **If history repeats,**
  - **Early stage : lower currents with bad vacuum → N/S = ~ 6 → 13 kHz**
  - **Final stage : high currents with good vacuum → N/S = ~ 0.5 → 23 kHz**
- **Tighten the TRG conditions if BG is serious**
  - **New tools : CDC 3D tracking, low level reconstruction for BG reduction**
  - **Suppress two-photon events : these are the signal in Belle**

Universal Trigger board 3 (gamma)

- **Final proto-type**
  - **For CDC, KLM, and GDL**
  - **FPGA : Virtex-6 HXT**
    - **FF1923 package : 3 FPGA choices**
- **IO**
  - **Main board**
    - **Clock : 1 in, 1 out**
    - **NIM : 2 in, 2 out**
    - **24 GTH (11 Gbps x 24)**
    - **LVDS : 64(32x2) in/out**
  - **GTX daughter board (optional)**
    - **40 GTX (6.25 Gbps x 40)**
  - **General IO board (optional)**
    - **Clock : 2 out**
    - **NIM : 8 in, 8 out**
    - **RJ-45 for Belle2Link : 4**
  - **All IO tested successfully**
    - **GTH/GTX BERT (PRBS31) ... no error for more than 3 days at target link speed**
- **28 boards purchased**
    - **GDL : 4 (2 spares)**
    - **CDC : 18 (2 spares)**
    - **KLM : 2 (1 spares)**
    - **For test bench : 4**

Floor Plan

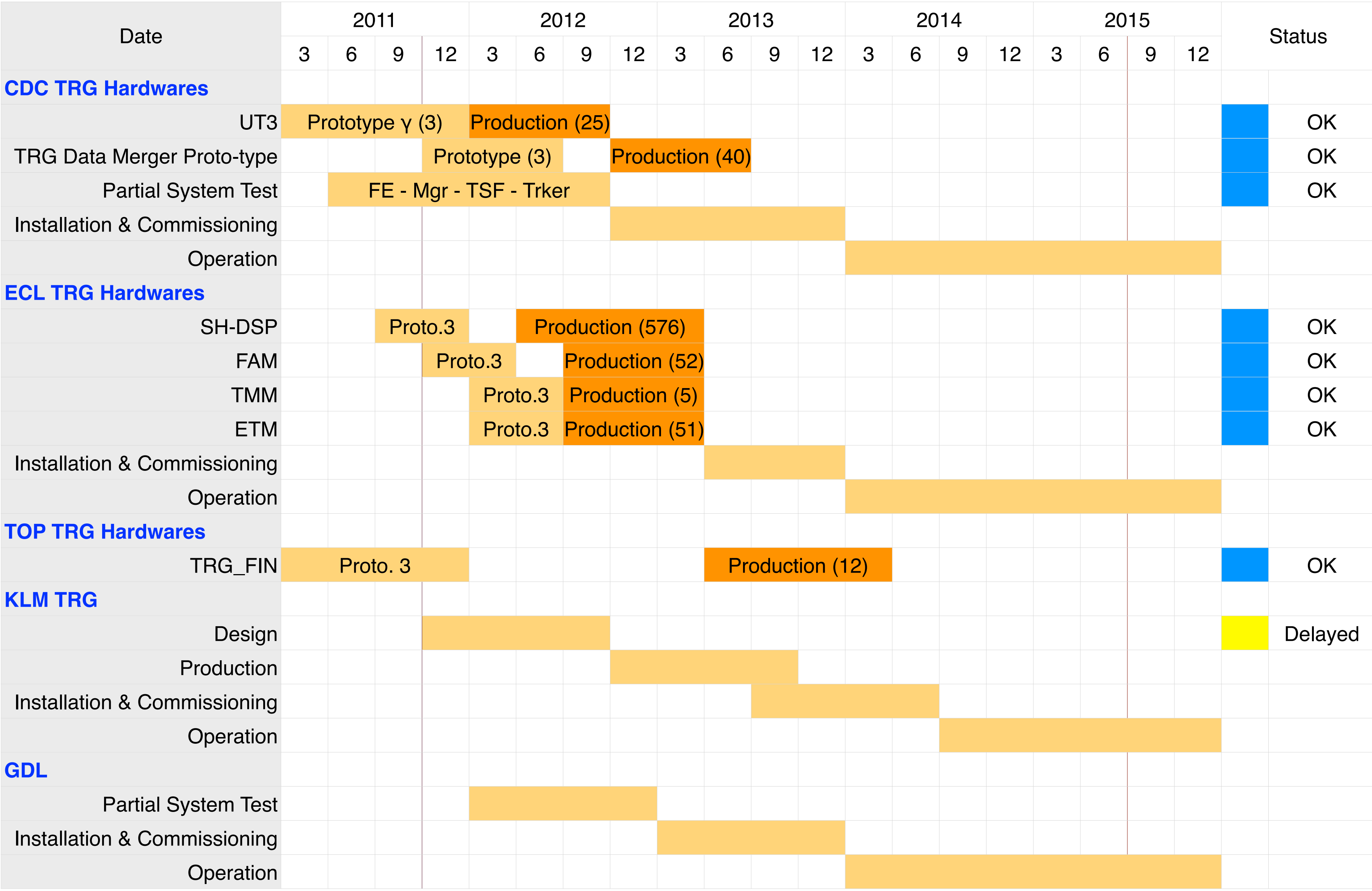
1F: 0th version layout



CDC : 6U VME crate x 4
ECL
TOP, KLM
GDL : 6U VME crate, NIM crate, Terminal, LA

- **#VME CPU for trigger < 20**

TRG Status and Schedule



TRG : Requirements and Strategy

- Requirements (☑ = ok, ☒ = under study or unknown)
  - ☑ High efficiency almost 100% for Upsilon 4S events
    - No dead-time -> pipeline
    - Redundant and independent TRG logics -> 3 main TRG
  - ☒ Max. average rate 30 kHz @ $8x10^{35}$ $cm^{-2}s^{-1}$
    - Limit from DAQ
    - Good background reduction
      - Flexible TRG logics to manage BG rates
      - Low level event reconstruction to identify BG
  - ☑ Latency ~ 5 usec
    - Limit from SVD front-end
  - ☑ Timing precision less than 10 nsec
    - Request from SVD front-end
  - ☒ Event separation 200 nsec
    - Request from DAQ
- Belle triggering scheme is employed again
  - Sub-Triggers + Global Decision Logic
  - Basic idea is same, but each components will be improved

    Data flow : parallel -> high-speed serial

    Data rate : 16 Mbps -> 190 Mbps (CDC wire case)

    Logic : hard-coded -> FPGA

    #cables and modules : O(1000) -> O(100)

Physics Targets

Process	C.S. (nb)	R @ L=10^{34} (Hz)	R @ L=8×10^{35} (Hz)
Upsilon(4S)	1.2	12	960
Continuum	2.8	28	2200
$\mu\mu$	0.8	8	640
$\tau\tau$	0.8	8	640
Bhabha *	44	4.4	350
γ-γ *	2.4	0.24	19
Two photon **	13	130	10000
Total	67	~190	~15000

* Rate of Bhabha and γ-γ are pre-scaled by factor 100

** Rates are estimated by the luminosity component in Belle L1 trigger rate

Physics Processes and TRG Logics

Process	σ (nb)	Rate (Hz) @ L=8x10^{35}
Upsilon(4S)	1.2	960
Continuum	2.8	2200
μμ	0.8	640
ττ	0.8	640
Bhabha *	44	350
γ-γ *	2.4	19
Two photon **	13	10000
Total	67	~15000

* Rate of Bhabha and γ-γ are pre-scaled by factor 100

** Rates are estimated by the luminosity component in Belle L1 trigger rate

- **Physics triggers**
  - **Upsilon 4S + continuum**
    - **Three-track**
    - **Total energy**
    - **Isolated cluster**
  - **Tau pair**
    - **Two-track**
- **Calibration triggers**
  - **Bhabha**
    - **Pre-scaled by Bhabha trigger (ECL)**
  - **γ-γ**
    - **Pre-scaled by γ-γ trigger (ECL)**
  - **Mu pair**
    - **Two-track**
  - **Random trigger**
- **Veto**
  - **Beam injection**
  - **Two photon events if necessary**
    - **Low level reconstruction is necessary**

TRG Read-Out

- Data to be read
  - Sub-trigger summary info. at each GDL stage
    - @ ITD, @ FTDL, @ PSNM, @ FINAL
  - Sub-trigger finer info. (for low-level reconstruction)
    - CDC, ECL, KLM, iTOP
- Contents of data
  - Bit(ex. CDC back-to-back) or word(ex. CDC 3D Track z position)
  - Edge info. (edge type and time stamp)
    - Time stamp := clock count @ 127MHz (= GDL system clock)
    - 16 bits for one edge
      - 15 bits for time counter, 1 bit for edge type
    - Time window : ～33 usec
- Data size
  - ～ 5 kB / event
- Request to DAQ group
  - One COPPER crate (16 boards, 64 Belle2 links)
    - 10 boards will be connected @ T0
    - 6 boards are spares

Sub-Trigger Summary Info.

Sub-Trigger	Type	Bit Width	Clock (MHz)
CDC	# Low Pt Tracks	3	127
	# Middle Pt Tracks	3	
	# High Pt Tracks	3	
	Charge Sum	3	
	Back-to-Back	1	
	Opening Angle	1	
ECL	E Low	1	
	E High	1	
	E Lum	1	
	# Isolated Clusters	4	
	Bhabha	11	
	Cosmic	1	
	Timing	5 *	
TOP	Timing	5 *	
	# Hits	3	
KLM	# Muon Hits	3	
	# Hadron Hits	1	
	Cosmic	1	
Total		40	

* 1 bit : hit or not, 4 bit : time counts (LSB 1ns)

TRG Read-Out Data Size

Sub-Trigger	Category	Type	Info	Bit Size	#Av. Hit	Size (Byte)		
CDC	2D Tracks	word	Pt, φ, charge	48	10	60	992	5194
	3D Tracks	word	Pt, (Pz?), φ, z, (r?),	80	10	100		
	Track Segment	word	ID, timing	32	200	800		
	Summary	bit		16	16	32		
ECL	Trigger Cell	word	Energy, timing	32	200	800	832	
	Summary	bit		16	16	32		
Barrel PID	Hit Pattern	word	ID, timing	32	20	80	112	
	Summary	bit		16	16	32		
KLM	Track	word		48	10	60	552	
	Hadron Cluster	word		48	10	60		
	Hits	word	ID, timing	32	100	400		
	Summary	bit		16	16	32		
GDL	Event	word	ID	48	1	6	2706	
	ITD, FTDL, PSNM	bit		16	150	300		
	Recon	word		48	400	2400		

2011/11/17
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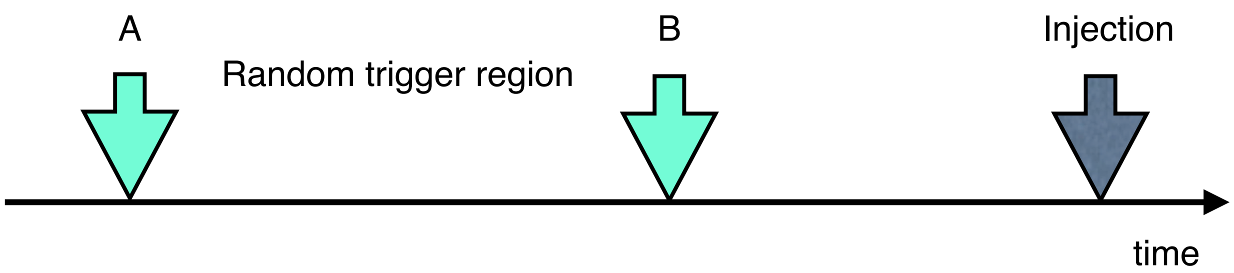
TRG for BEAST II

- **Run starts in 2014/12**
  - **No official request from BEAST II group**
  - **No special preparation**

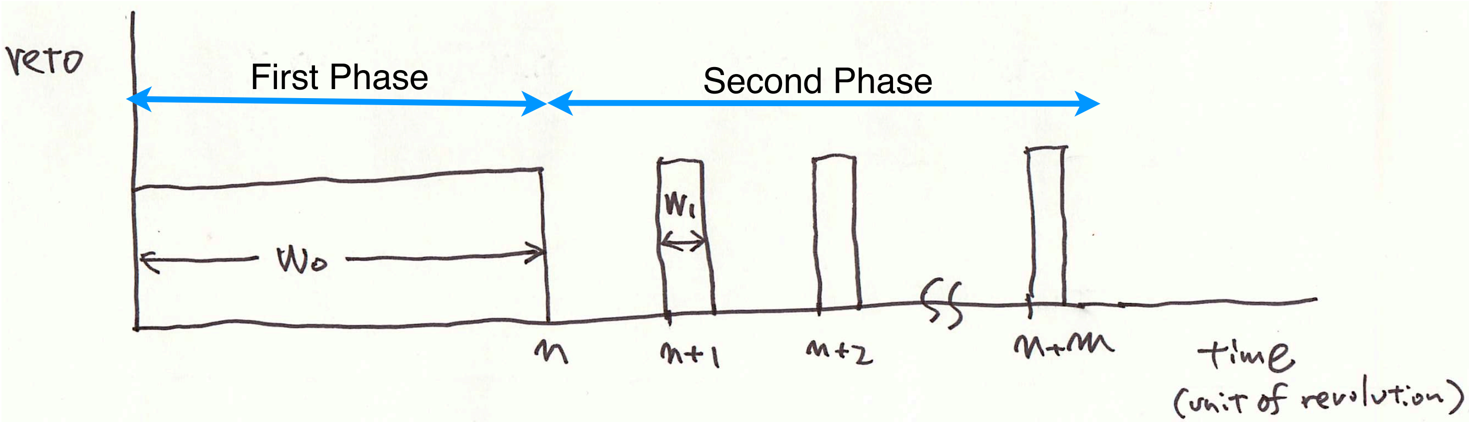
- **ECL-TRG, KLM-TRG, and GDL will be ready**
  - **Plan to do our own trigger system test**
  - **If necessary, we can provide**
    - **Random trigger**
    - **Injection veto**
    - **Bhabha trigger**
  - **In such a case, I/F to BEAST II should be discussed**
    - **Belle2Link ? (<- DAQ)**
    - **NIM level ?**
    - **Something else ?**

Comment on Random Trigger

- We will prepare three types
  - Periodical random trigger (sync'ed to the KEKB revolution signal)
  - Pseudo-random trigger
    - Random seed generation method with the independent local clock
  - Delayed Bhabha trigger
    - Delay : ～ 50 usec
    - Issued at the same KEKB bunch after 5 turns
    - Proportional to the KEKB luminosity
- If you want random trigger just before injection
  - We have to take into account of the abort gap
  - Latency between random trigger and injection can be random in fixed period
    - To above looking at the same bunch (depending on KEKB injection mechanism)
    - Timing of A and B relative to injection should be fixed according to sub-detector's requests



Injection Veto



- **Two phases**
  - **First phase : veto n turns completely**
    W0 = n * 10 usec
    n = 10〜100
  - **Second phase : veto periodically**
    W1 = 〜1 usec

    m 〜 300
  - **Three parameters (n, m, W1) : SKEKB dependence**
- **Veto pattern is generated in GDL**
- **The first phase only in Belle case (n=350)**
- **Veto signal is sent to SEQ to calculate dead-time**