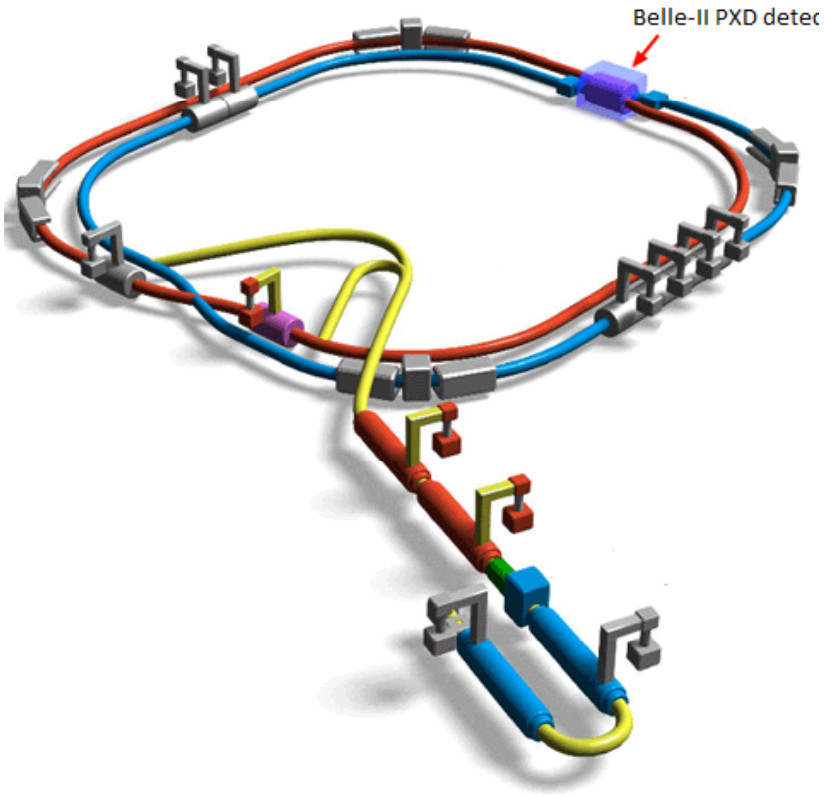
Belle II PXD Power Supply Firmware Development Status



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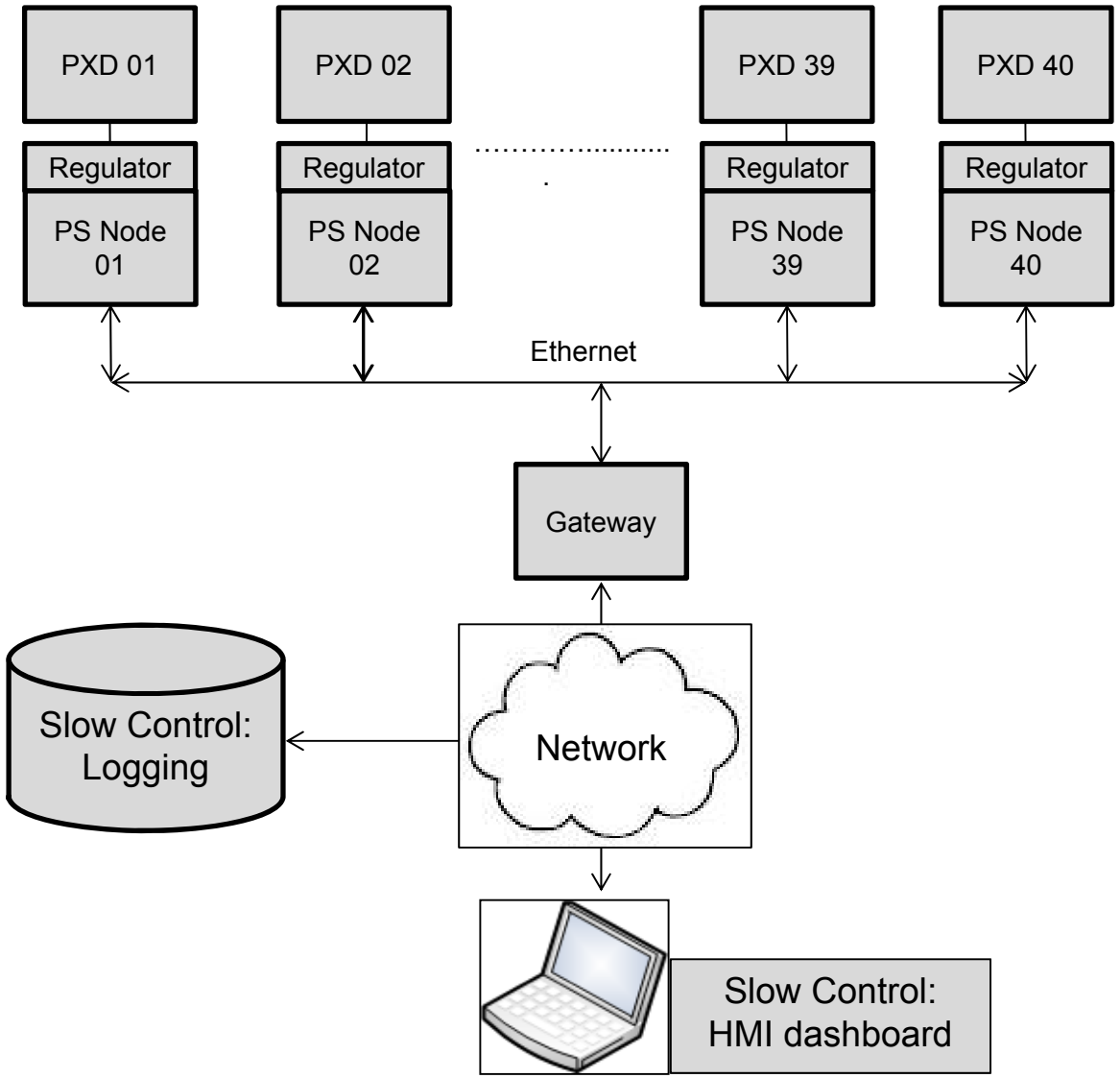
PXD Power Supply Control System: Architecture (1/2)



PXD Power Supply Control System: Architecture (2/2)

- Slow control
  - Interface to operator: power-up, power-down, calibration
  - Logging and Monitoring
  - Platform: Linux/PC
  - Software: QT application

- Gateway
  - Connect PS nodes and Slow control (HMI, Logging)
  - Platform: Linux/PC
  - Gateway software
    - Chromosome Middleware
    - Slow Control interface (Network Shared Memory, OPC-UA, …)

- Power supply nodes
  - Steer power-up and power-down sequences of highly sensitive voltage and current channels
  - Calibration and configuration
  - Monitoring
  - Platform
    - ARM Cortex-M3 MCUs (STM32F107VC)
    - Analogue interface to regulators: ADCs and DACs
  - Software
    - FreeRTOS + lwIP IP stack
    - Chromosome Middleware

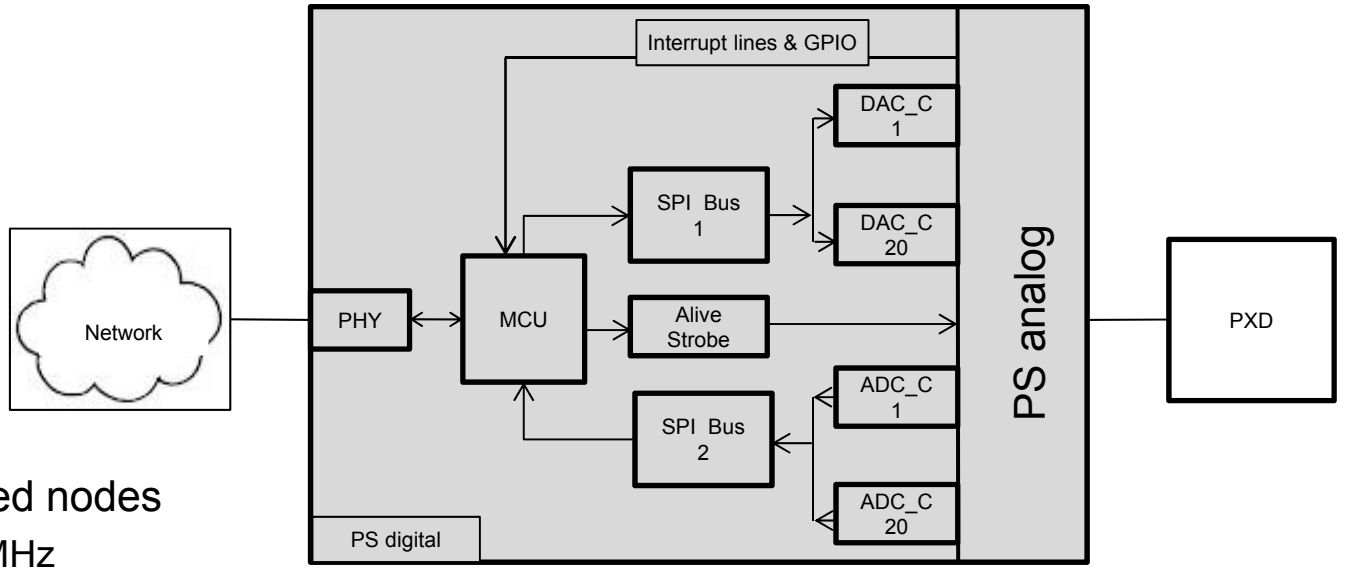
Reliability analysis results

- Analyses performed
  - Failure Mode and Effect Analysis (FMEA)
    - Bottom up analysis
    - Performed based on our understanding of the requirements documents
  - Fault-Tree Analysis (FTA)
    - Top-down analysis
    - Performed in project meeting with LMU to achieve best coverage
- Starting point of analysis: Relevant HW components considered
  - Digital part (ADC, DAC, processor, …) and analog part (current amplifiers, resistors, …)
  - Goal: Get feeling for the need of reliability measures implemented in SW
- Results:
  - All catastrophic events must ultimately be handled in HW (by analog regulator part)
    → Decision against node design with redundant MCUs: Reduce cost and complexity

Component	Failure mode	Recognition/Tolerance	Recommended actions
DAC	Hold	MCU	Shut down, send notification
	Arbitrary	MCU	Shut down, send notification
DC/DC Card	Arbitrary	(1) MCU (2) Hardware Safety System	(1) Graceful shutdown (MCU) (2) Hard shutdown

Excerpt of FMEA worksheet

PXD Power Supply Nodes: Hardware Architecture

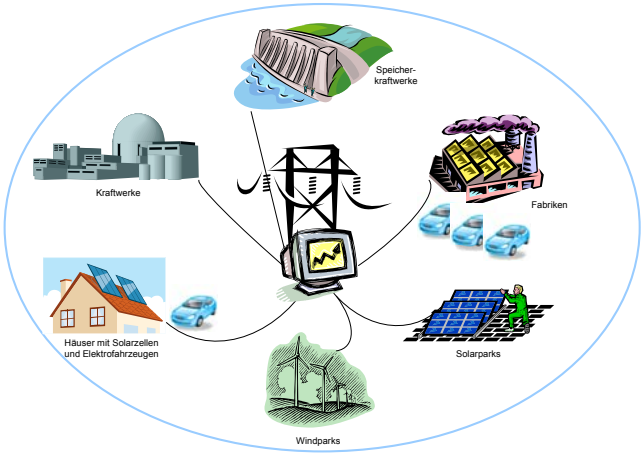


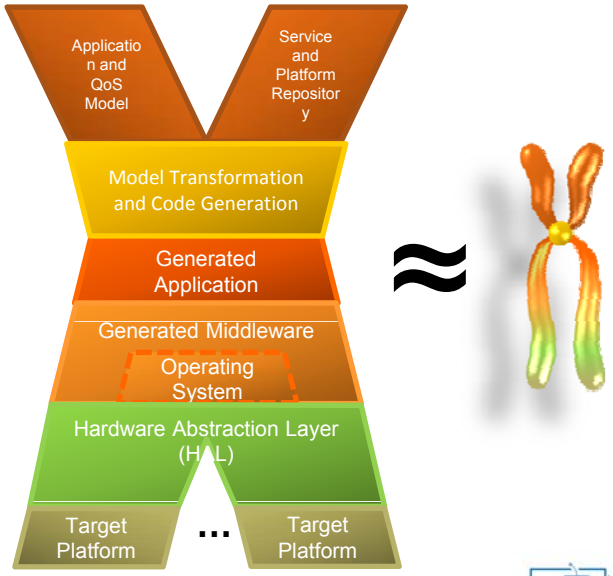
- STM32F107VC-based nodes
  - Cortex-M3 @ 72 MHz
  - Memory: 256 kb flash ROM, 64 kb SRAM, external EEPROM (calibration)
  - Connectivity: 100 MBit Ethernet, 2 SPI busses available

- Interface to regulators
  - DAC: AD5392: Set voltages and current limits
  - ADC: AD7322: Read back voltages and currents
  - Interrupts & GPIOs: Status information
  - Alive strobe
    - Result of reliability analysis
    - Analog part issues shutdown if digital part fails

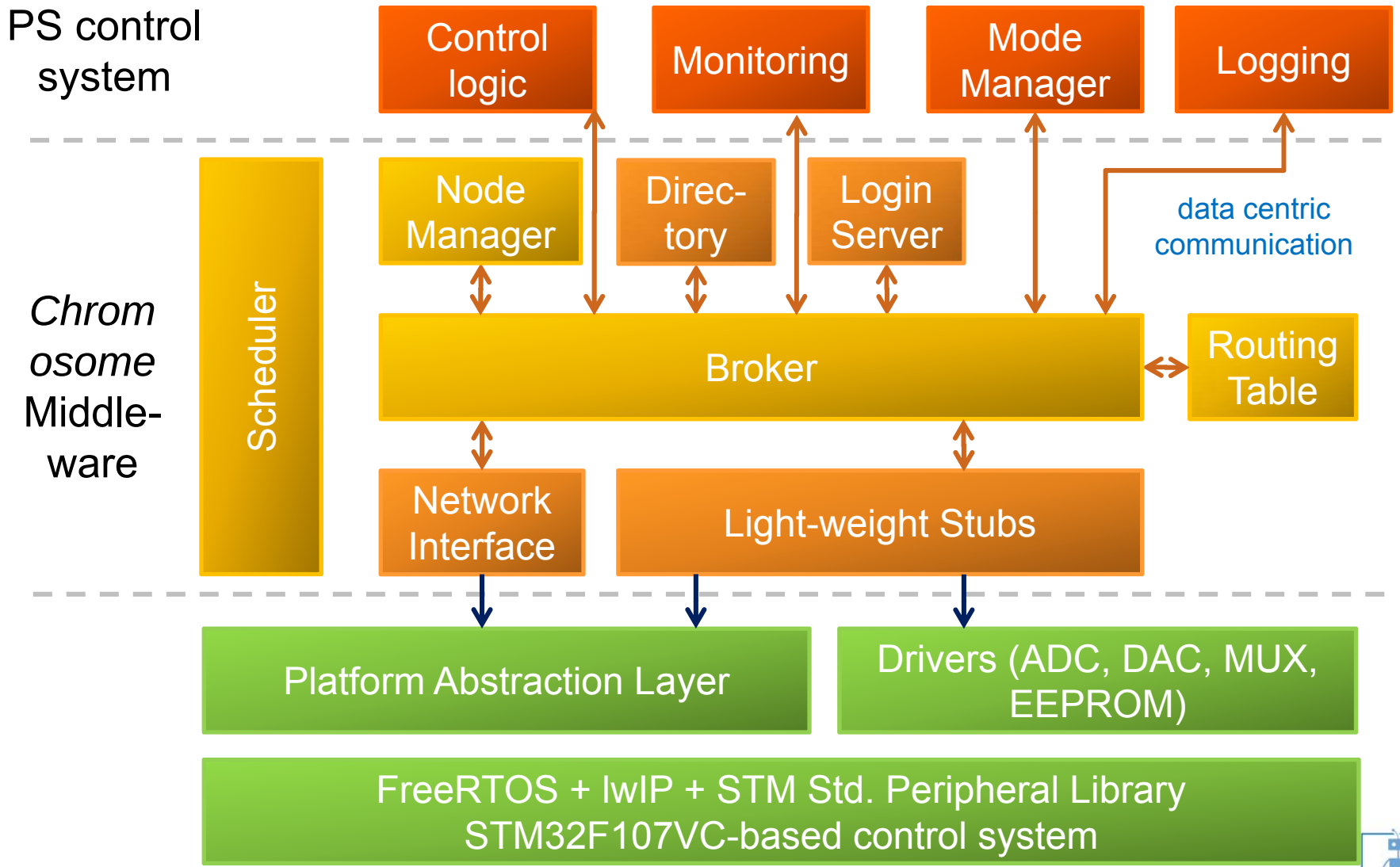
CHROMOSOME

- CHROMOSOME: open-source middleware for Cyber-Physical Systems developed by **fortiss**
- Challenges in Cyber-Physical Systems:
  - Systems-of-Systems
  - Global optimization / control instead of local control
  - Increasing sensor data
  - Future communication partners are not always known up front
  - Combination of systems with different requirements:
    - » safety-critical and non-critical subsystems (mixed criticality systems)
    - » Real-time and non-realtime
    - » Resource constrained devices and cloud computing
- Cyber-Physical Systems are cross-domain, hence a cross-domain solution is required.
  - Embedded middleware and SOA middleware will converge / get interconnected
  - Monolithic middleware architectures will disappear
  - A (meta-) data centric approach is used to combine basic building blocks

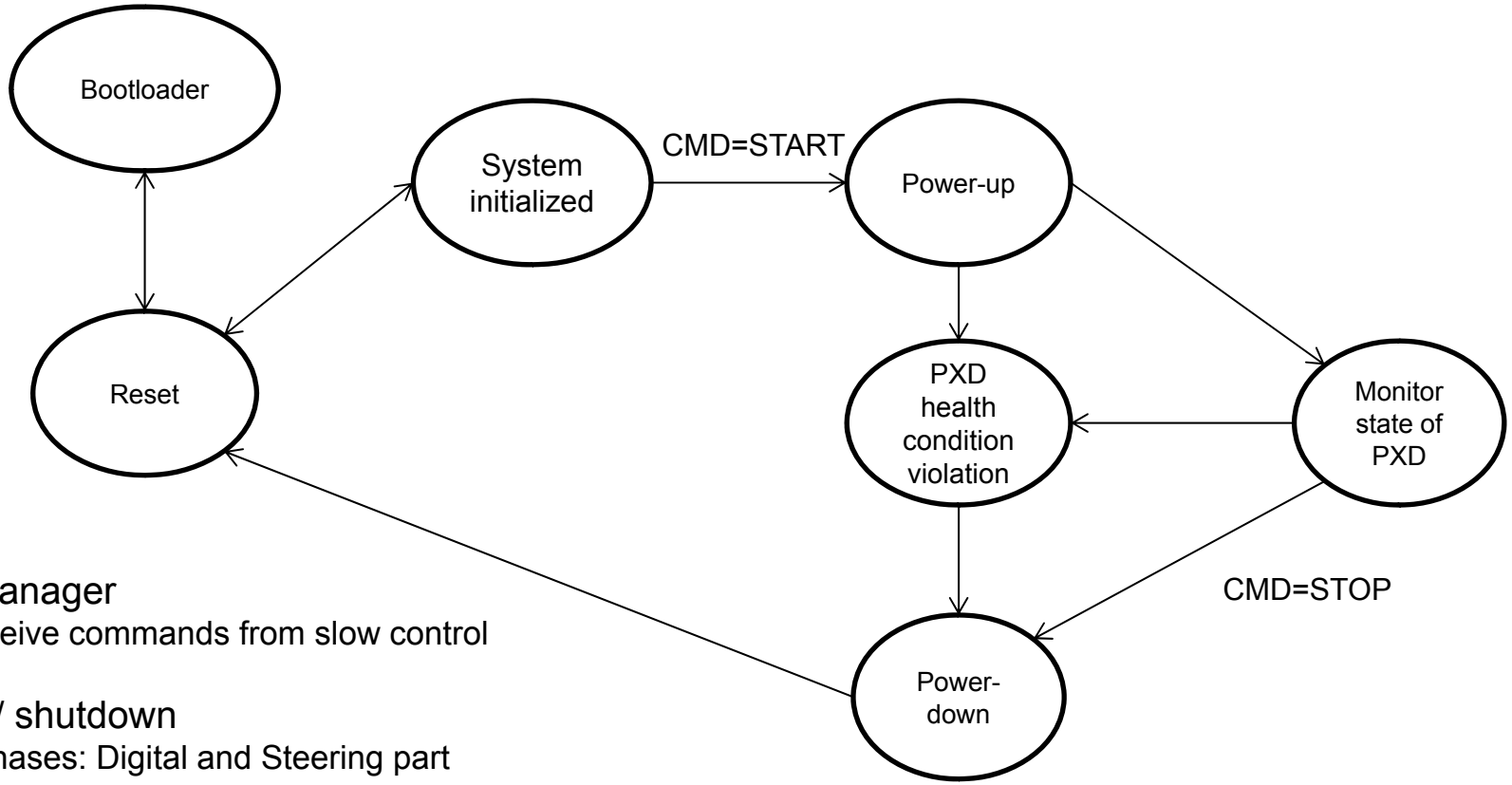




PXD Power Supply Nodes: Software Architecture



Firmware: Control logic



- Mode manager
  - Receive commands from slow control
- Startup / shutdown
  - 2 Phases: Digital and Steering part
  - Synchronized with overall system via slow control (e.g., cooling interlock)
- Health monitoring
  - Firmware
    - Monitor PXD state via ADCs
    - Issue graceful shutdown
  - Analog hardware
    - Monitor digital part and PXD state
    - Issue emergency shutdown

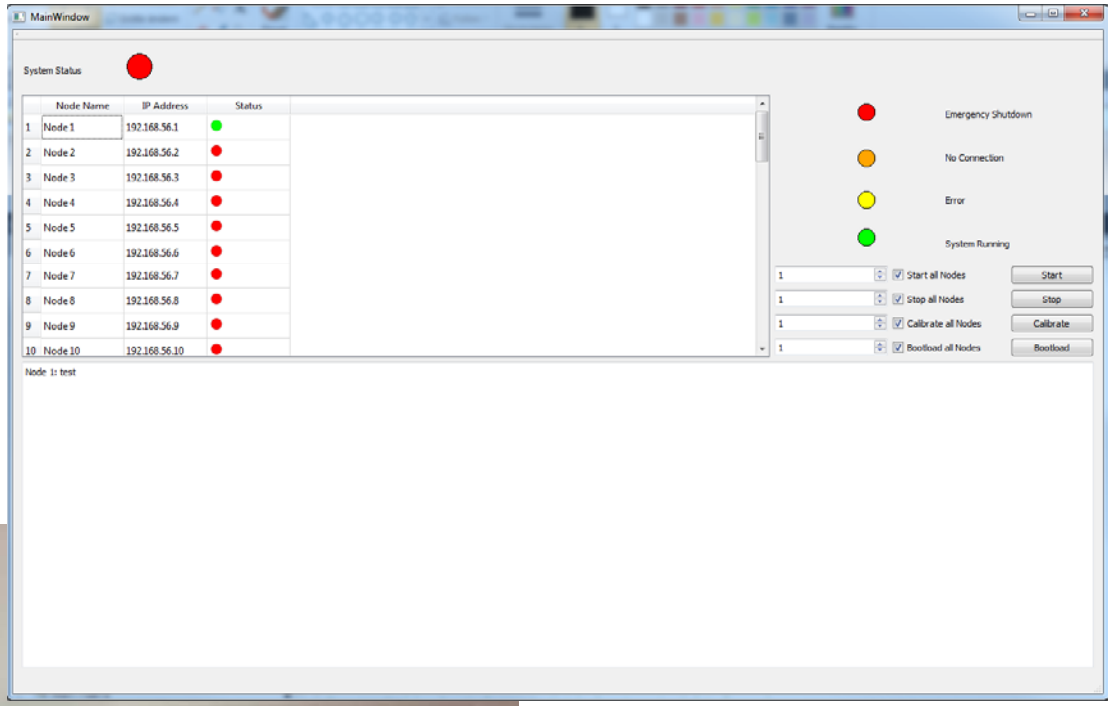
Project Progress

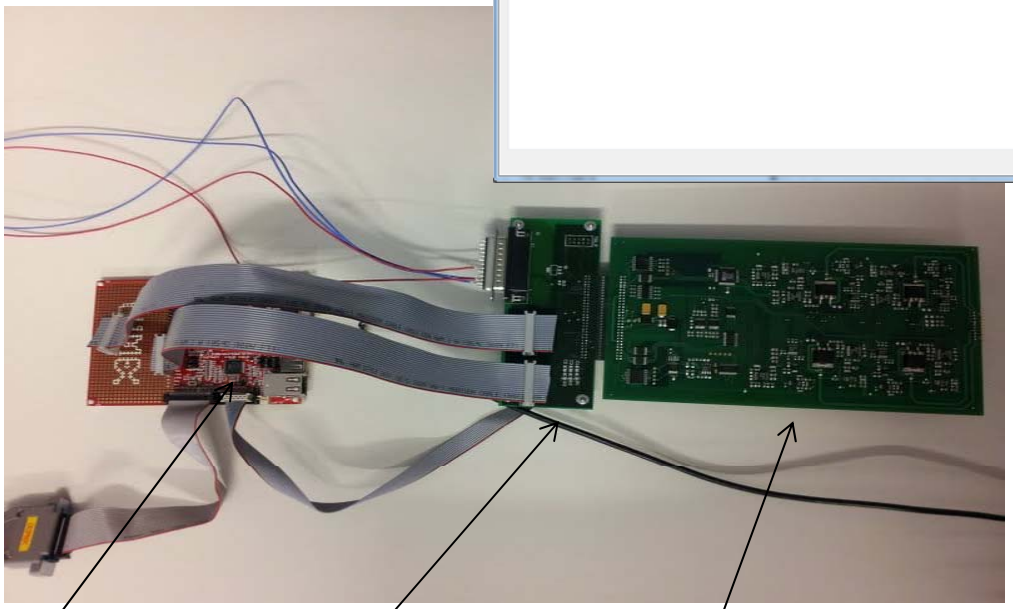
- Completed
  - Requirements and Reliability analysis
  - Consulting in Hardware Design
  - Firmware
    - Select and prepare open source tool-chain for ARM MCU
    - Integration of third party libraries (ARM CMSIS, STM Standard peripheral library, FreeRTOS, lwIP
    - Infrastructure: DHCP, Bootloader
    - Port of Chromosome Middleware to MCU
    - Design Specification
- In progress
  - Firmware Implementation:
    - Drivers for external ICs: final testing
    - Monitoring and control logic
  - GUI: First version almost ready

Start Date:
12.04.2011

Deadline:
31.3.2012

Laboratory Setup





MCU Breakout board Regulator module

Thank you for your attention!