Belle2Link and Model System Tutorial

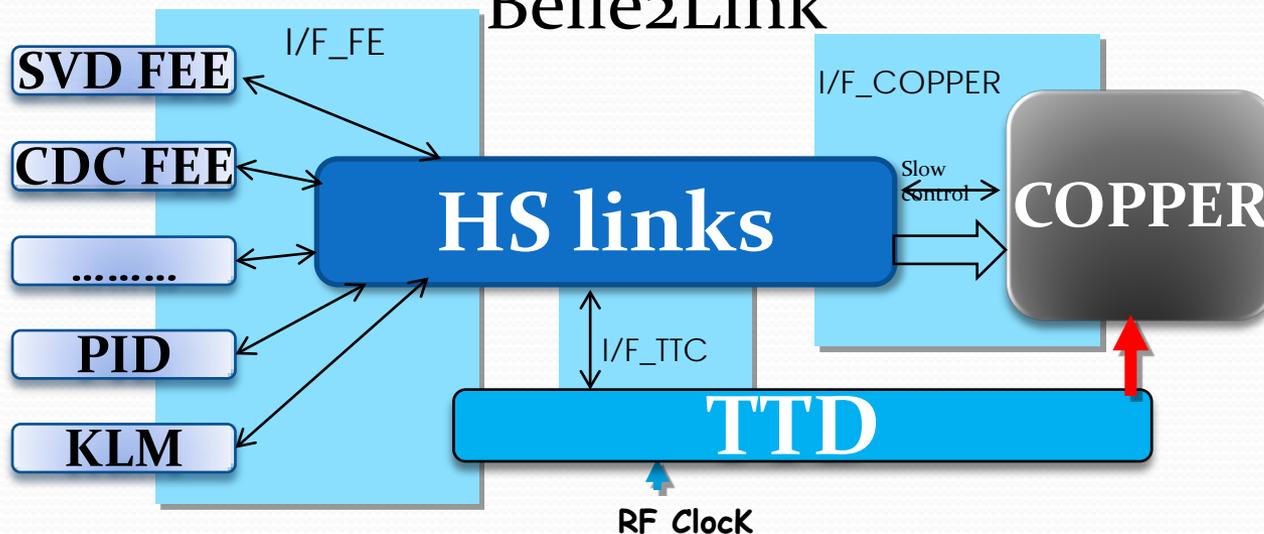Liu Zhen-An,   Triglab/IHEP, Beijing

Jan. 17 2012, Hawaii

Outline

- Status of Belle2link
  - Test made at KEK Nov/Dec. 2011
  - Problems met and solved
  - Results of the tests and concluson
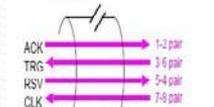- Tutorial of Belle2link MS System

Status of Belle2link

- Background
  - Belle2Link proved working well in KEK joint test with 16ch CDC Jul 2010
  - Slow control function added early year 2011
  - Joint test and merge with TTD at IHEP in Aug. 2011
  - Modification to 48ch CDC FEE
  - further test with CDC and ECL at KEK in Nov/Dec
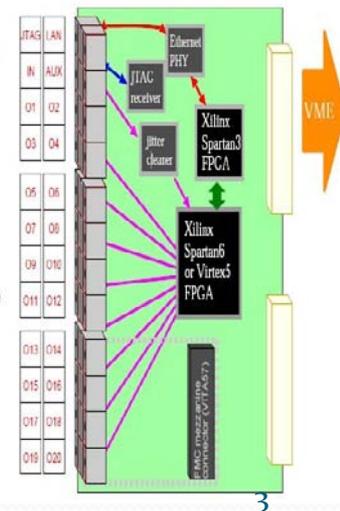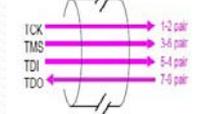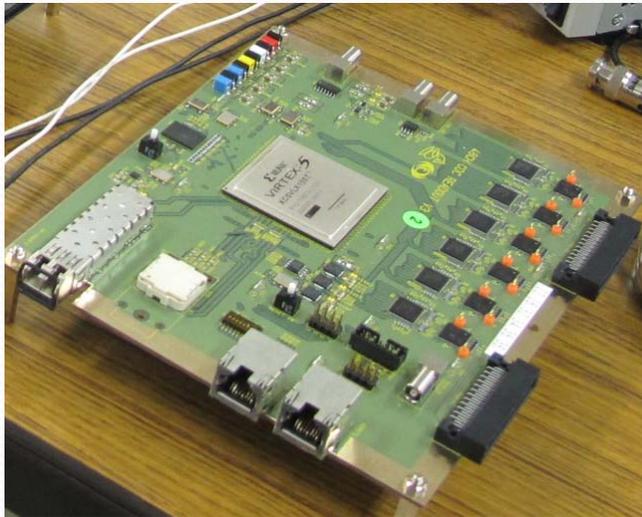

Belle2Link

Task of KEK test

- By Dehui,Jinzhou,Nakao,Zhen-An with help from Uno, Taniguchi ,Higuchi,itoh,…

  - Reading firmware for 48ch version CDC FEE OK?
  - Slow control functions OK with 48ch CDC FEE ?
  - Real trigger through TTD OK?
  - Reading 2-4 48ch CDC FEE board with FSLB/COPPER
  - Joint test with CDC detector prototype
  - Test with ECL FEE board
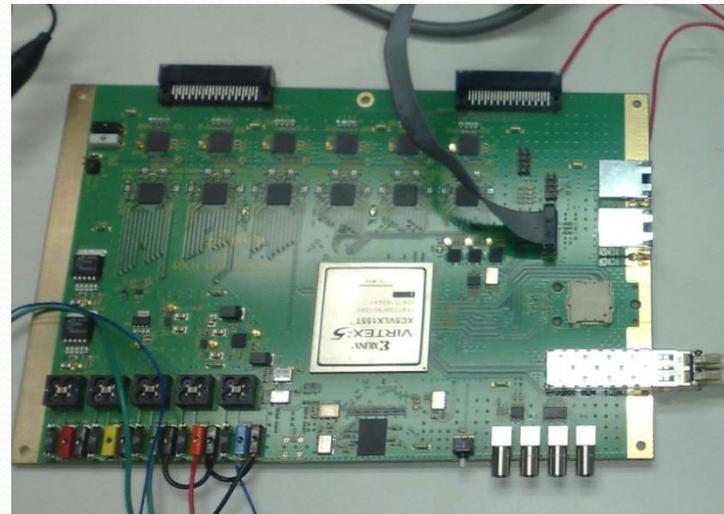
Work in Nov/Dec. at KEK-1

- Recovered Model System(MS) of Beijing at KEK
  - 16channel CDC board
  - Upgrade the Finesse Driver
  - Install the Software of B2L
  - Connect the Belle2Link with TTD module
- MS for 16channel CDC board works well with distributed clock and trigger by TTD
    - System initialization OK
    - Slow Control OK
    - Data acquisition OK

Work in Nov/Dec. at KEK-2

- Test for 48channel CDC boards was not smoothly
  - Firmware implementation based on the original 48 channel CDC board.
  - 48ch CDC FEE
    - 1 ver.1
    - 2 ver.3
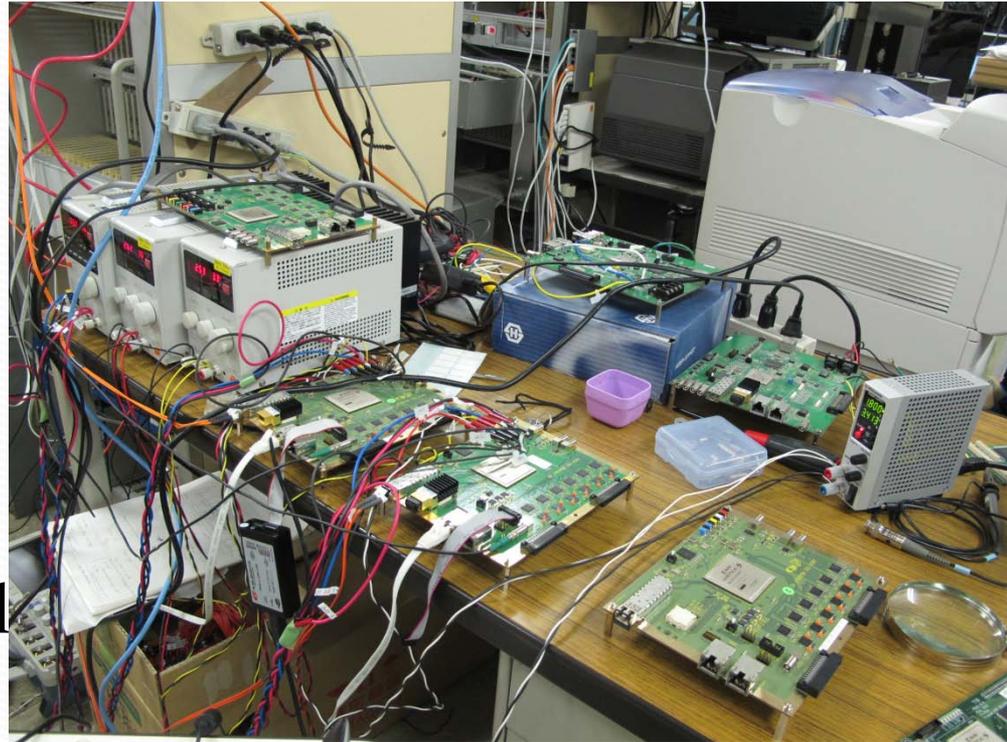 - Limited documentation
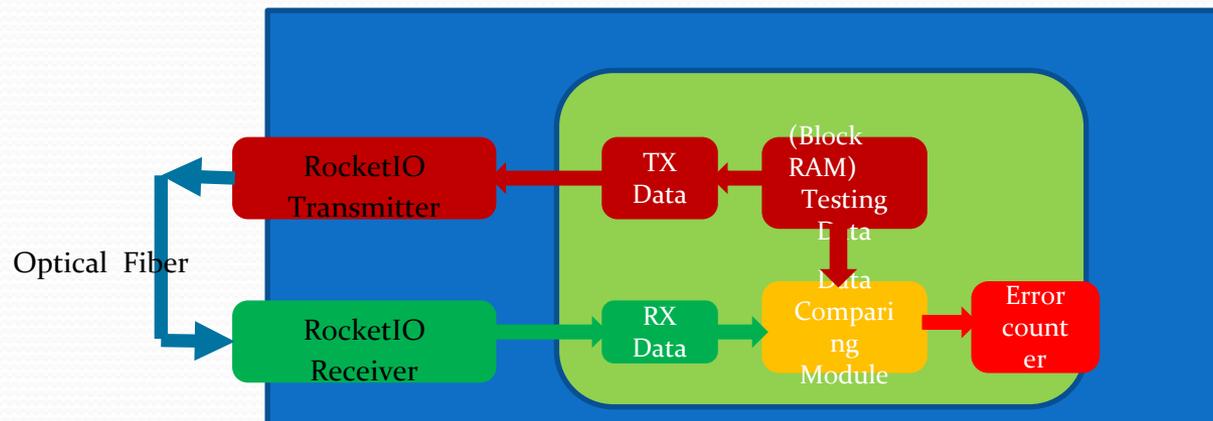

48ch CDC ver. 3

original 48ch CDC(Ver. 1)

Work in Nov/Dec. at KEK-3

- With help of Nakao-san' coordination, key changed are known
  - Redefinition of the pin constraint
  - Setting of the mode and event length by slow control
- Belle2Link get data but still unstable

Bit error test for 48ch CDC boards-1

- Board to be tested:
    - CDC_CH48_V3 NO.1 board,
    - CDC_CH48_V3 NO.2 Board,
    - CDC_CH48_V1 NO.3 board
- Bit error test to verify the problem.
    - Data pattern are produced in ISE RocketIO IP Core,
    - Transmitted out via RocketIO on to optical fiber, and then received via RocketIO.
    - Check received data against transmitted. A mismatch counts an error.

RocketIO Transmitter ← TX Data ← (Block RAM) Testing Data

Optical Fiber

RocketIO Receiver → RX Data → Data Comparing Module → Error counter

Bit error test for 48ch CDC boards-2

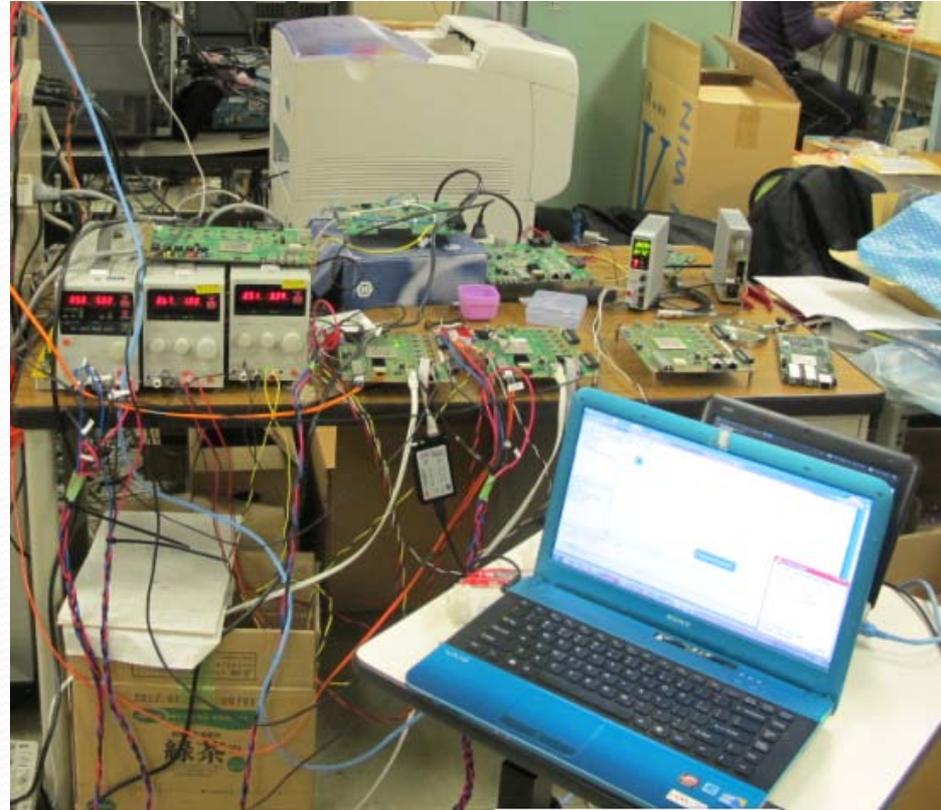- Result: Bad error rate from the board #2, returned to KEK electronics

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CDC_CH48_V3 NO.1 board			
CLK	Line rate(Gbps)	Time(minute)	Error Count
REFCLK_125M	2.5	10	0
REFCLK_125M	3.125	12	0

CDC_CH48_V3 NO.2 board			
CLK	Line rate(Gbps)	Time(minute)	Error Count
REFCLK_125M	2.5	10	0
REFCLK_125M	3.125	11	16

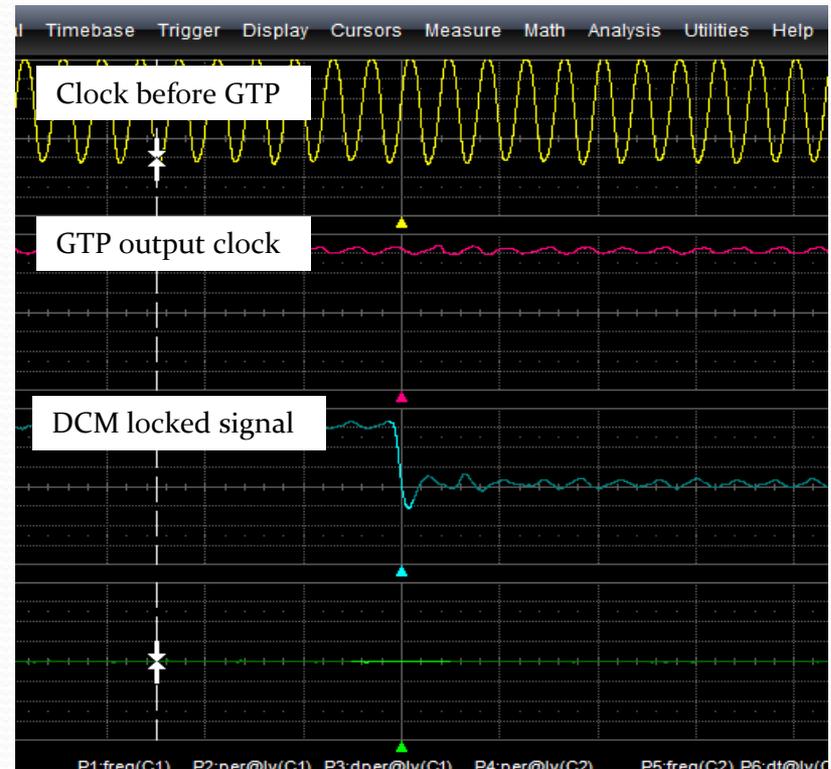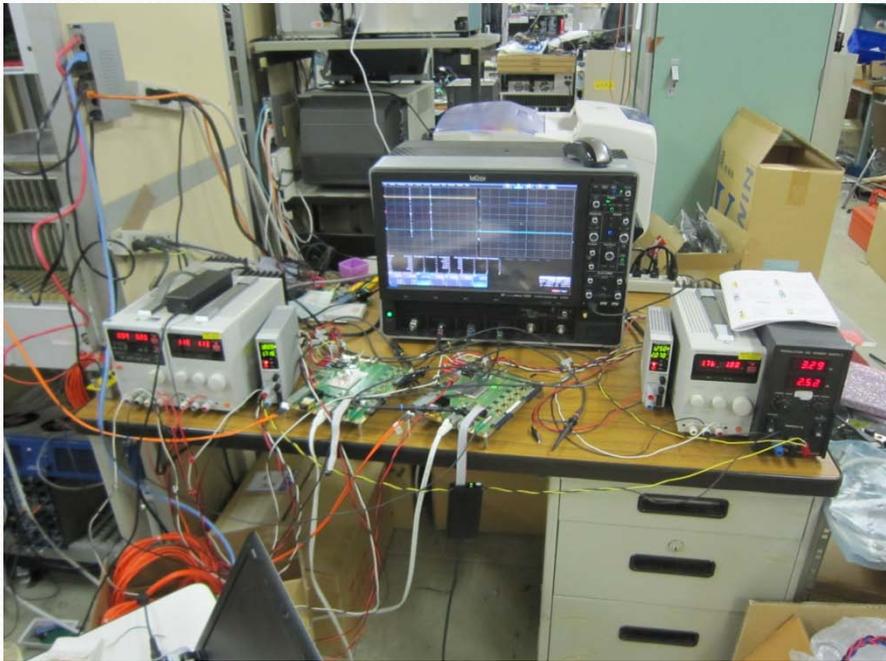| CDC_CH48_V3 NO.3 board			
CLK	Line rate(Gbps)	Time(minute)	Error Count
REFCLK_125M	2.5	10	0
REFCLK_125M	3.125	10	0

Stability test for CDC #1 and #3(1)

- The board #1 and #3 can work for a short time before one of them is down.

- Test to verify the problem
  - Providing independent power supplies for two boards
    - board #3(ver.1) is better than board #1(ver.3)
    - Board #3 can work steadily for more than 12 hours
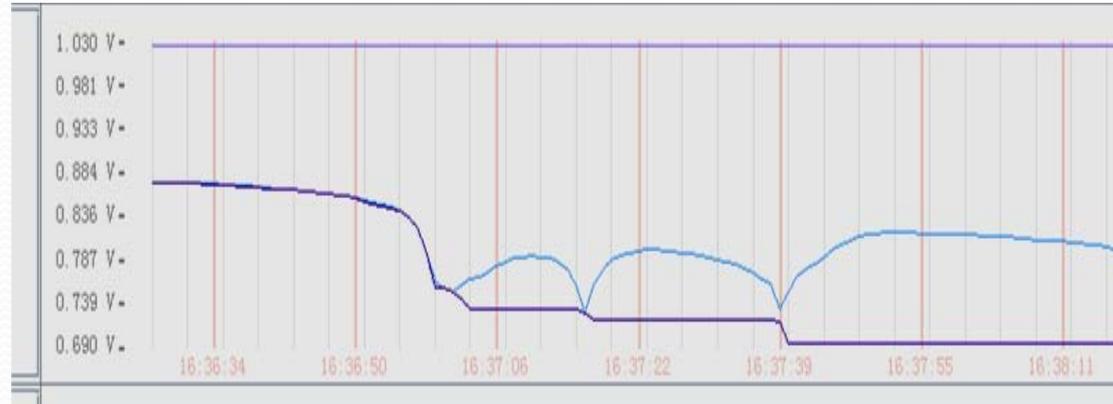   - Board #1 can work for no more than 20 minutes.

Stability test for CDC #1 and #3(2)

- test with Osciloscope
  - Detect the signal of the GTP output clock and DCM lock signal
  - The GTP output clock was down when the link is down.

Clock before GTP

GTP output clock

DCM locked signal

Stability test for CDC #1 and #3(3)

- Core voltage and temperature of the board #1 by system monitor.
  - For dummy version:
    - Temp. ~45 deg
    - Core voltage : 0.9v
    - Work steadily
  - For full function version:
    - power supply of 1.0V
      - Temp.: ~50 deg, Volt. at pin: 0.867v,Core volt: ~0.788v
      - Can't work steadily : Link is down after 1 minutes
    - Increase the power supply of 1.0 to 1.2
      - Temp.： ~56 deg,Volt. at pin： 1.074v,Core volt.： ~0.9 v
      - Can't work steadily. The voltage dropped suddenly to 0.75V. The link is down.
    - Increase the PS to 1.25v(1.0v: Matsusada ;1.8v KENWOOOD)
      - Temp.: ~59 deg,Volt. at pin: 1.115v,Core volt. : ~0.95v current of 1.0v is 2.072A
      - Can work steadily for long time.

Summary of 48ch CDC FEE boards test

- CDC FEE #2(ver.3) unstable, returned to electronics
- The CDC #1(ver.3) is sensitive for the 1.0v PS
  - High quality PS for 1.0v
  - Be careful with the difference between PS reading and the Pin voltage
  - The core volt. must be near 1.0
  - The high quality PS helps, but need further checking
- The CDC #3(ver.1) is better. Further test is expected.

- Reason: Second hand FPGA might be the reason.
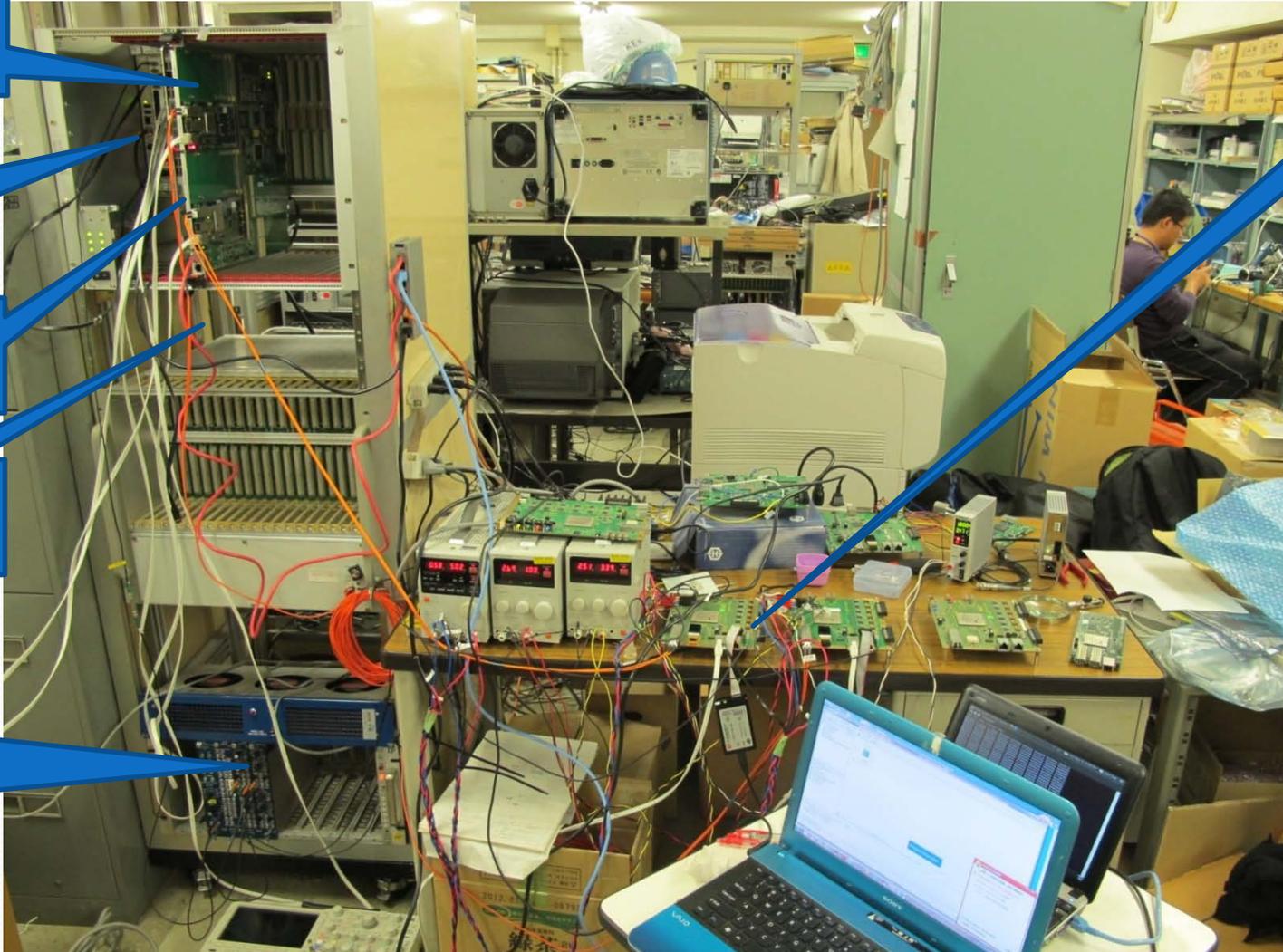
Further test on CDC detector

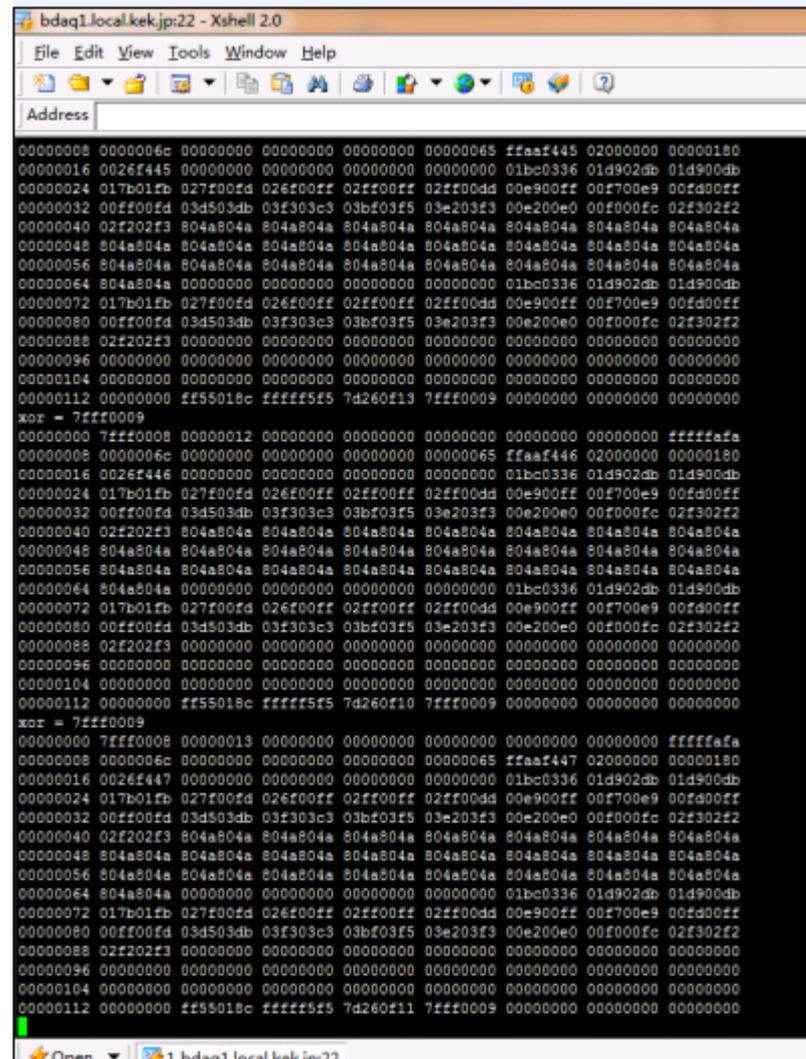COPPER

TTD

HSLBs

Fibers

Test signals and trigger

CDC FEE

Results of the joint test(1)

- 1-4 FEEs/HSLBs reading OK

- Disk data saving OK

- CDC window, delay, threshold, pedestal setting OK

win6delay73.xlsx

	A	B	C	D	E	F	G	H
1	Board B:	Trigger#=00000000 ***/						
2	100	100	100	100	100	100	100	140
3	140	140	140	140	140	140	140	149
4	100	100	100	100	100	140	100	100
5	100	100	100	100	100	100	100	100
6	100	100	100	100	100	100	100	100
7	100	100	100	100	100	100	100	140
8	100	100	100	100	100	140	100	140
9	Board D:	Trigger#=00000000 ***/						
10	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0
13	0	0	0	0	0	0	0	0
14	0	0	0	0	0	0	0	0
15	0	0	0	0	0	0	0	0
16	0	0	0	0	0	0	0	0
17	Board B:	Trigger#=00000001 ***/						
18	100	100	100	100	100	140	100	140
19	140	140	140	140	140	145	147	155
20	100	100	100	100	100	140	100	100
21	100	100	100	100	100	100	100	100
22	100	100	100	100	100	100	100	100
23	100	100	100	100	100	140	100	140
24	100	100	100	100	100	140	100	100
25	Board D:	Trigger#=00000001 ***/						

Results of the joint test(2)

- Problems found
  - Test signals were too small
  - Delay, window Term mis-understood
    - Transformation of delay, window is needed
- Proven by Nakao-san's work later

Test with ECL

- Late of the KEK stay, test with ECL tried
- Firmware/software provided
- Some success as reported by Zhulanov.
- Furtere communication for problems met.

- Other information please see Nakao-san's talk.

Z.A. LIU, BelleII TDAQ Workshop at Hawaii

Conclusion

- The joint test at KEK was helpful and neccessary, not only to Belle2link, but also to FEE
  - Lot of test results are useful to electronics
- Belle2link is fully functional with slow control for CDC system test
  - Minor refinement for misunderstood part.
- Test with ECL started with some success, further mutal understanding will help
- Second Distribution with some ngc file, but will be fully source later as it was in first distribution, after some discussion at IHEP.
- Comments and suggestions are welcome, epecially from Nakao-san.

Toturial of Belle2link and MS System

- Remarks
  - 2 Versions of the source code(firmware,software) of Belle2link are in hand of Nakao-san for distribution
  - Documentation are also included in the distributions
  - Most of the information of this tutorial is included in the documentation

Part 1: Hardware

- For MS, following hardware are needed
  - FEE board(CDC board as model)
  - Optic fibers
  - High Speed Link Board (HSLB, Plugged to COPPER)
  - COPPER board
  - A 9U VME
  - Server PC (file system server)
  - Control PC or terminal

CDC board linked to HSLB in 9U VME

COPPER board with HSLBs

HSLB

16channels CDC and 48 channels CDC

Part 2: Firmware

- Two sets of firmware are needed
  - FEE FPGA
    - Belle2link core part
      - RIO_receiver: slow control module
      - RIO_trans: data link module
      - Para_decode(for CDC): Parameter I/F(reference design)
    - TTD part
      - Belle2clk
      - Belle2trg
    - CDC FEE part
      - ADC TDC PROC EBUF RAW
  - HSLB
    - SLOWCONTROL: slow control module
    - Frame_check : data link module

Part 3: Software

- Integrated tool for belle2link functions
  - B2LD0
    - link   - check the link and make HSLB prepared for data acquisition
    - trigger   - release the trigger signal on FEE board
    - Linkrst - reset the Belle2Link
    - Trghold – hold the trigger signal of FEE board
    - Parameters （window, delay…）
      - Configure the parameters of FEE board
    - Checkfee –check the version, type of FEE board, serial#.
    - Checkerr -check the error of the Belle2Link
    - trigger source[real, sim] -choose the trigger source
    - Data acquisition -future
- Data collection
  - Readhslb ： read the data of FEE from the COPPER;
- **Driver : for HSLB board**
  - ..\belle2link\driver\Cprfin_generic.o

Part 4: Distribution file structure

- Belle2Link
  - Document
    - Belle2link-note-draft-ver0.2.doc (document for Bell2link)
  - Driver
    - cprfin_fngeneric(HSLB driver)
  - Firmware
    - 16ch CDC(Belle2link firmware for 16 channel CDC)
      - CDC ch16 ver. 1_0
      - Hslb
        - CPLD
        - HSLB firmware ver. 1_0
    - 48ch CDC (Belle2link firmware for 48 channel CDC)
      - CDCV3_REV01 - VER1
        - Belle2link
          - CDC (CDC readout directory)
          - ISE12 (project directory)
          - Src (source file directory)
          - TT (Timing and trigger directory)
    - Hslb
      - CPLD
      - HSLB firmware ver. 1_1

- Belle2Link
  - Software
    - B2LD0.c
    - Readhslb.c
    - Record.c
    - Fileconf.c
    - ect.

Part 5: System Preparation

- **Configure the HSLB**
  - CPLD   iMPACT(JTEG)
  - FPGA   iMPACT(JTEG), XIlinx platform flash or online downloading
  - FPGA   online downloading : bootmgt
- **Configure CDC readout board**
  - CDC iMPACT(RJ45) ,FLASH
- **Driver installation**

  - Copy the general Finesse Diver to   /lib/modules/2.4.30-20050518a/misc/cprfin_fngeneric.o
  - Copy the Shell File HSLB to the
  -   /etc/init.d
  - use command "chkconfig" to install the module file
  - Reboot the system
- **Program installation**
  - Copy directory of "software" to Linux file system.

Part 6: Booting up a Belle2link running

- Trigger signal to FEE are blocked until the slow control reliese it by slow control. Following steps should be followed:

  - Step 1: *./B2LD0 –[abcd] link* :check the link, if the link works well, the upper green LED will light up.

  - Step 2 *./B2LD0 –[abcd] checkfee* :get and check the type of FEE board and the version of the hardware and software

  - Step 3 *./B2LD0 –[abcd] raw* :choose the date mode of the CDC readout board.

  - Setp 3 *./B2LD0 –[abcd] –p window HEX delay HEX* : Configure the parameter of the FEE readout board.

  - Setp 4. *$readhslb*: Create a new terminal, run the program " readhslb"

  - Step 5 *./B2LD0 –[abcd] trigger*:Release the trigger signal of the FEE board.

  - Then enjoy the game!

Part 7: Trouble Shooting

- **Error indication/messages and system recovery**
  - If there is something wrong with the Belle2Link, the yellow Error LED on HSLB Pannel will light up. You should follow the steps below to restart the system.
  - Step 1: *./reset-fifo-and-finesse*: reset the Finesse board and the fifo of the COPPER
  - Step 2 *./ B2LD0 –[abcd] trghold:* block the trigger signal to FEE board
  - Setp 3 *./ B2LD0 –[abcd] linkrst*: reset the belle2link
  - Step 4 boot up the Belle2Link again as in Part 6.

PLAY and ENJOY!