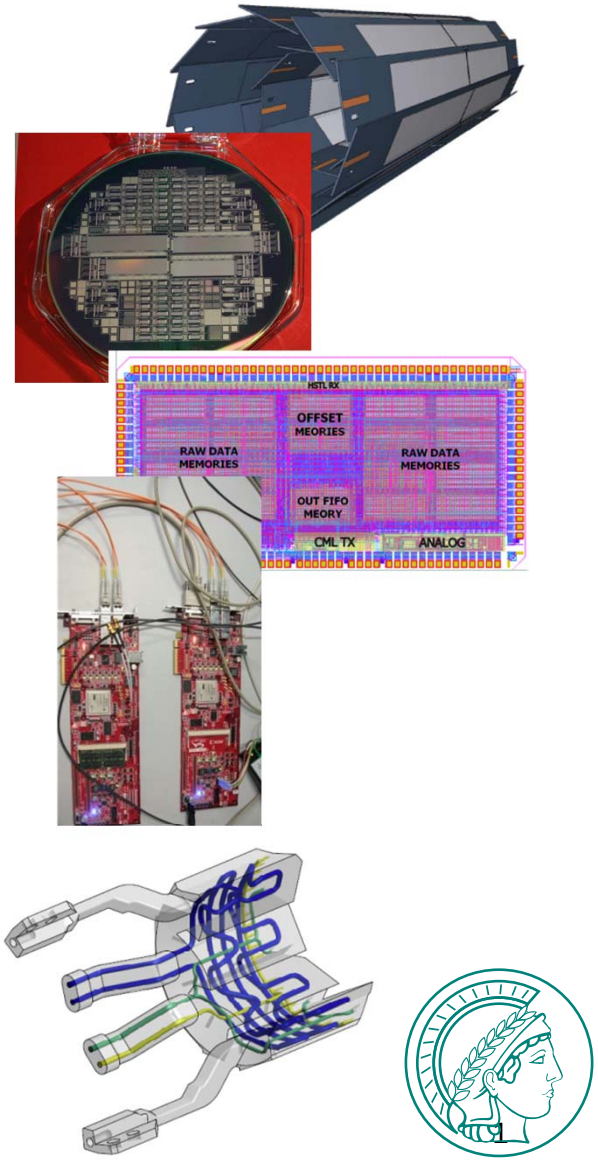
Hawaii TRG/DAQ Meeting
PXD-Fontend Status

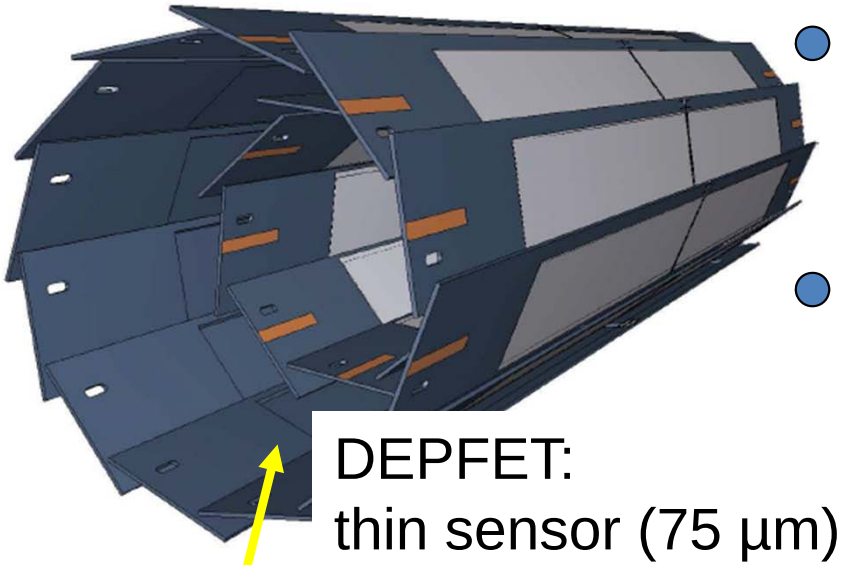
- Reminder of PXD @ Belle II
- Overview of PXD-DAQ Chain
- Interface between PXD and Belle II: Data Handling Hybrid („DHH“)
- Slow Control Considerations
- Schedule



Silicon Tracking System @ Belle II

SuperKEKB: Nano beam option, 1 cm radius of beam pipe

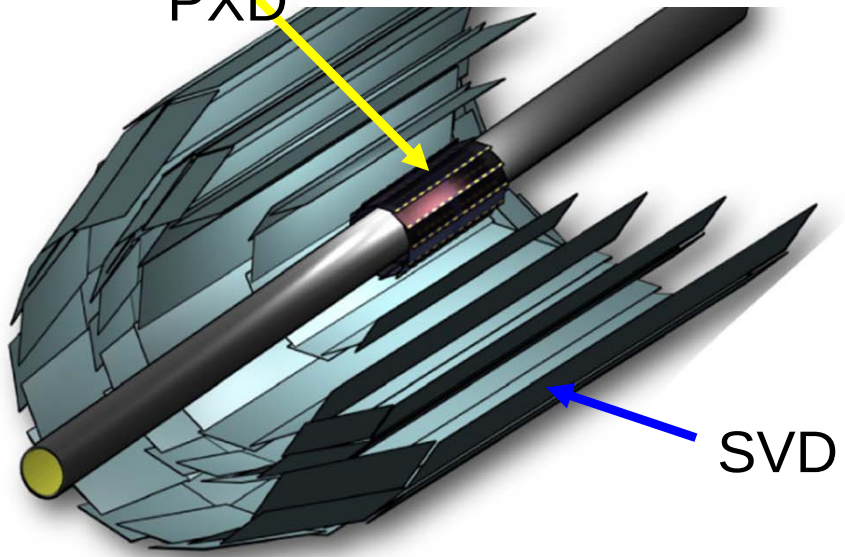
„PXD“



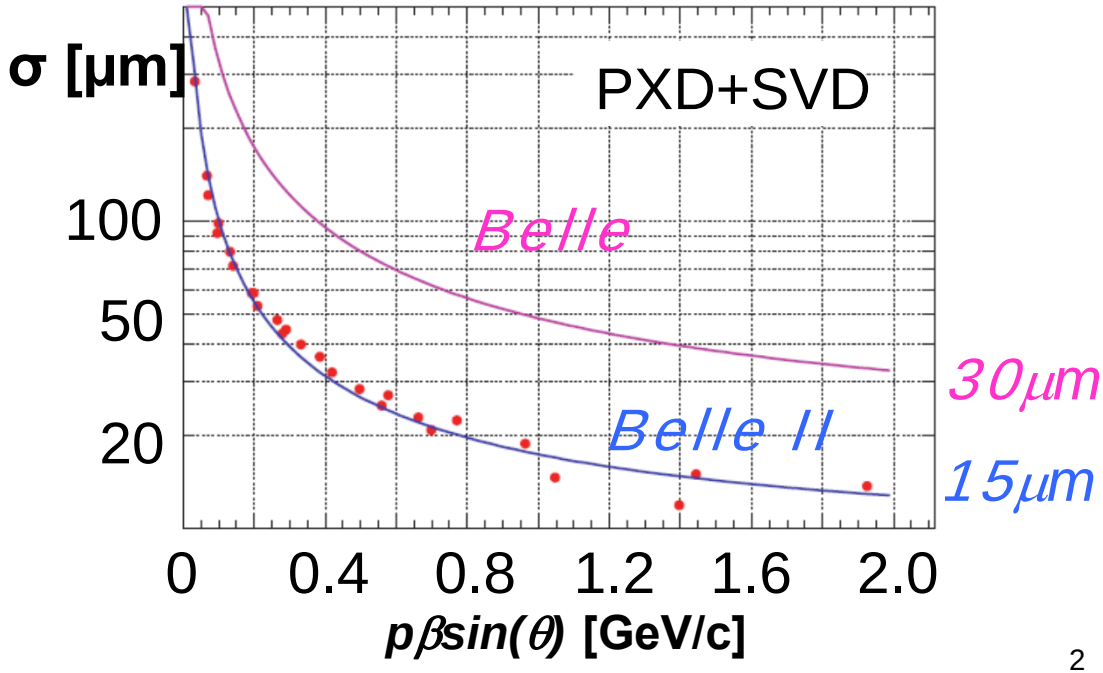
- 2 layer Si pixel detector (DEPFET technology)
  (R = 1.4, 2.2 cm) monolithic sensor
  thickness 75 µm (!), pixel size ~50 x 50 µm²
- 4 layer Si strip detector (DSSD) ← „SVD“
  (R = 3.8, 8.0, 11.5, 14.0 cm)

DEPFET:
thin sensor (75 µm)
unique worldwide

PXD



Significant improvement in z-vertex resolution



Principle of Operation of DEPFET-PXD

Row wise read-out

("rolling shutter mode")

- select row with external gate

  read current,

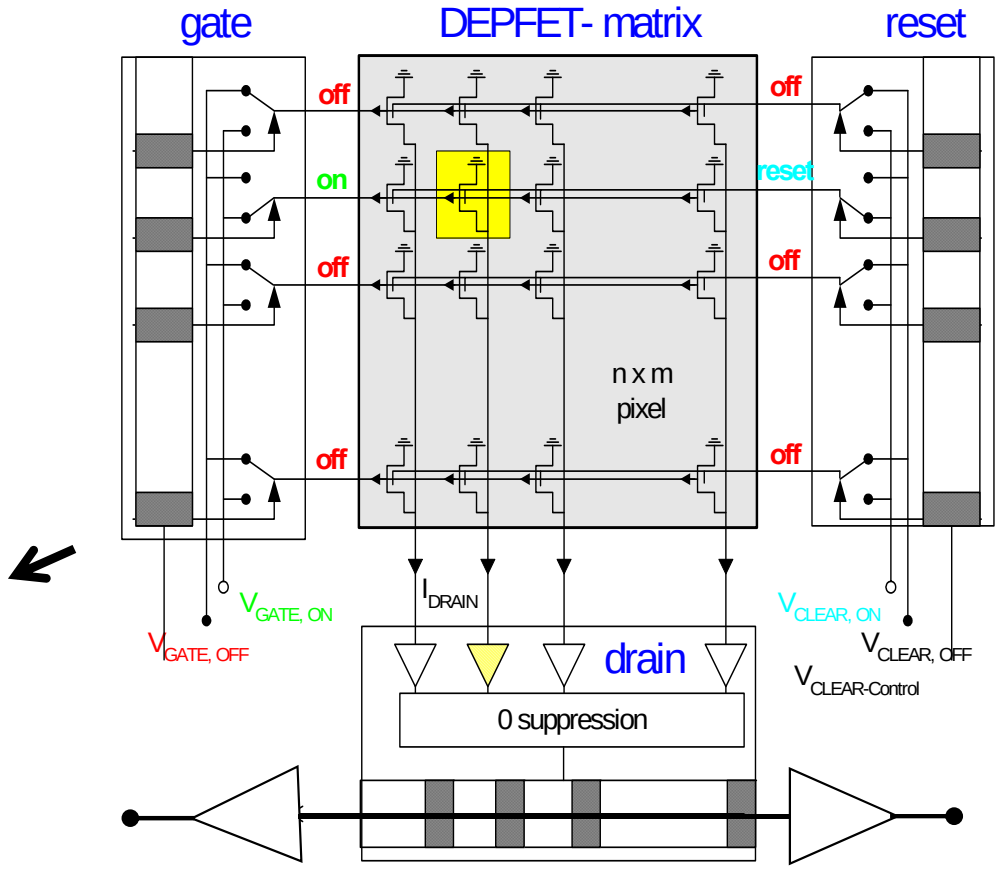
  clear internal gate,

  read current again

  → the difference is the signal

- readout time of entire PXD in 20 µs

- three different auxiliary ASICs needed



→ Switcher

→ DCD (drain current digitizer)

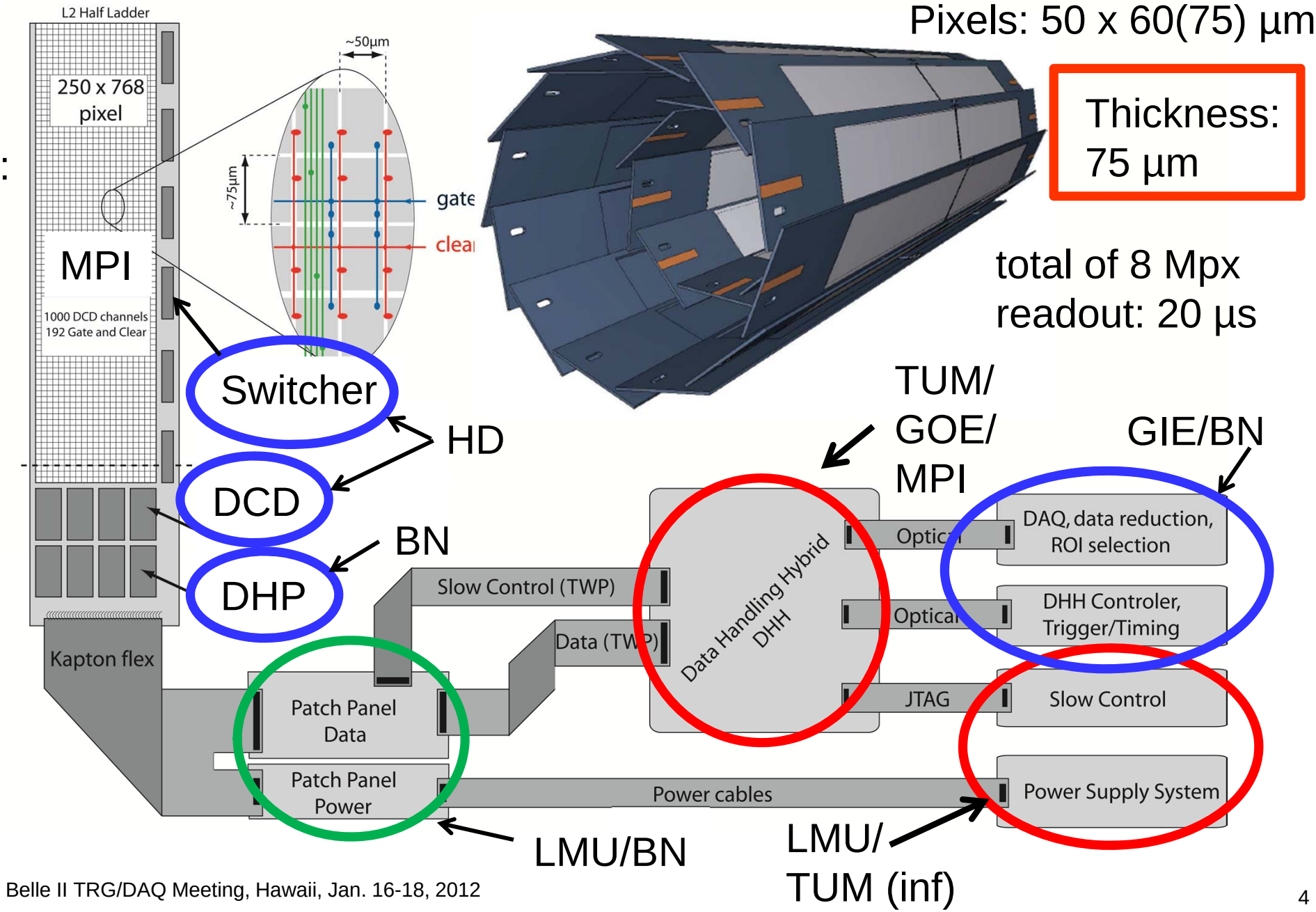
→ DHP (data handling processor)

PXD DAQ-Chain - Layout

half ladder: 768 rows

250 cols

15 x 70 (85) mm



Pixels: 50 x 60(75) µm

Thickness: 75 µm

total of 8 Mpx readout: 20 µs

Interface to Belle II TRG: DHH

Data **H**andling **H**ybrid

Incoming data 4x1.5Gb/s (4 DHP's per PXD half ladder)
Data buffering
Data Reformatting and Remapping

Housing clustering ASIC ("DCE") on piggyback card
(DDR2 SODIMM)

Further processing of cluster information in FPGA
Merging four DHP data streams into two streams 2x6Gb/s
Dead time generation to prevent data loss

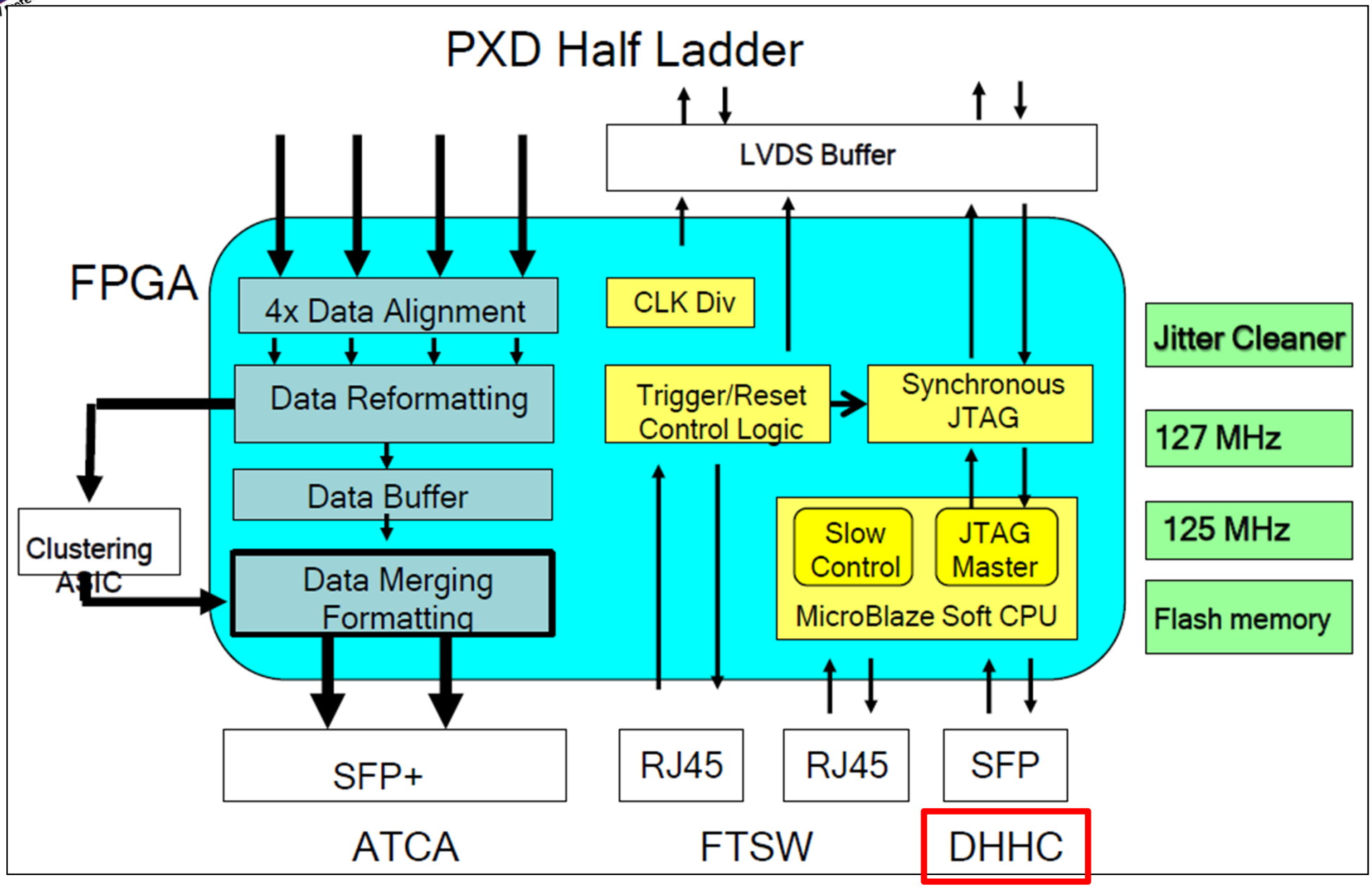
Translate signal from copper to optical -> ATCA

Interface to Belle II TRG: DHH

- Timing and Trigger Distribution
  - Synchronous clock and trigger distribution to all PXD mods. (triggered readout) using Nakao-san's TTD's
  - Clock synthesis in FPGA
    - 3/20 of 508.89 MHz RF clock = 76.33 MHz

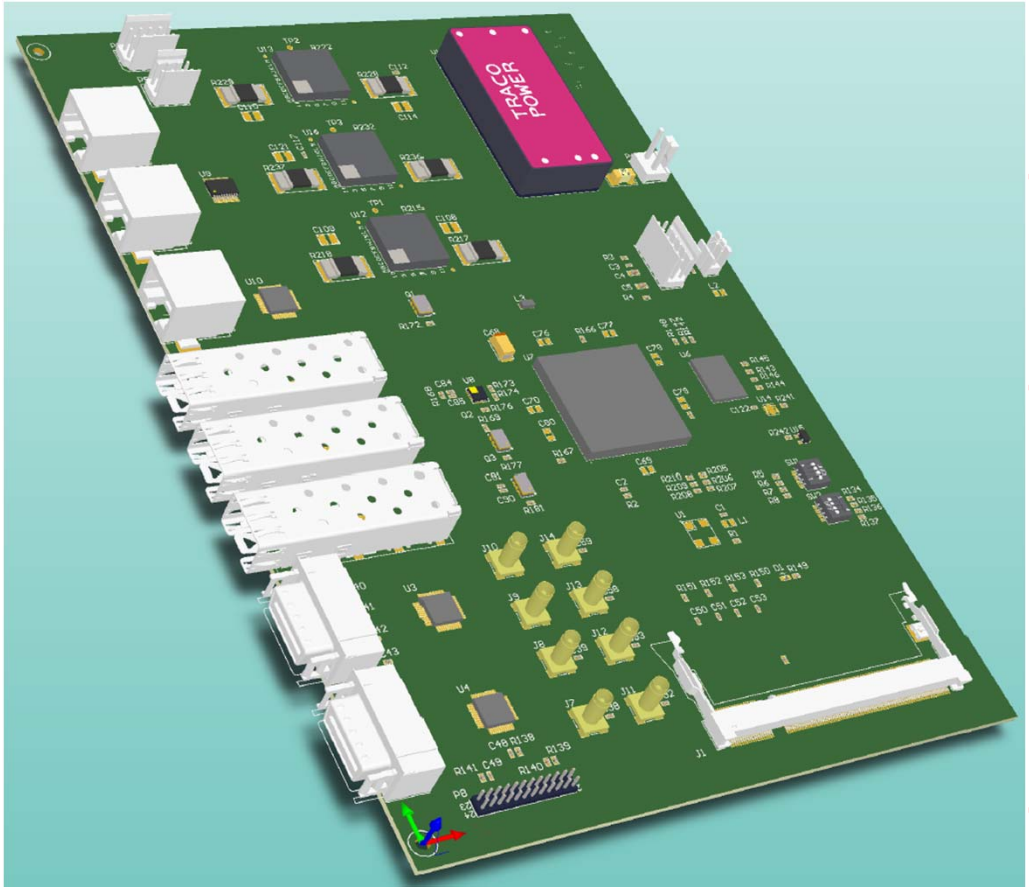
- JTAG interface for slow control (JTAG master to Belle II)
  - FPGA and flash memory programming
  - Microblaze CPU + Ethernet
  - DHP, DCD loading configuration parameters
  - Switching readout modes : suppressed ⇔ full frame

DHH Architecture



Status of DHH

tested OK:



DHH prototype
(2 modules delivered in mid november)

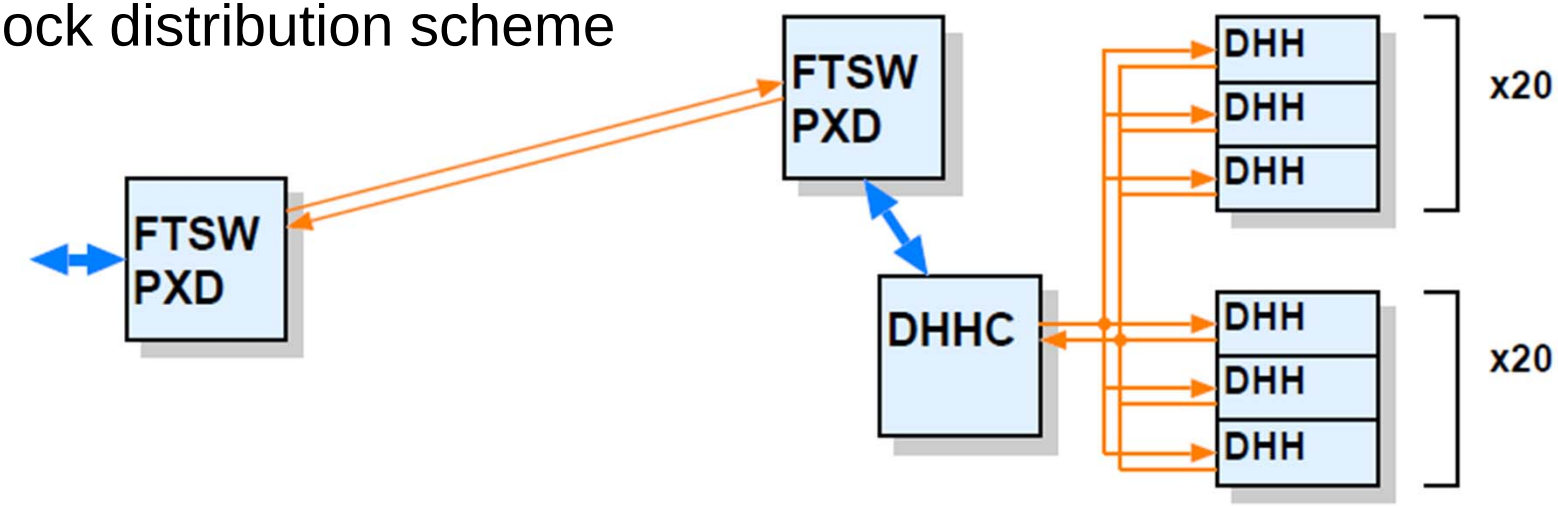
- ethernet (receive e.g. slow control commands)
- SFP optical links (small form pluggable transceiver)
- JTAG on the FPGA of the DHH, will have softcore-CPU running "MicroBlaze“ (can make a JTAG connection to all the ASIC's -> set thresholds and pedestals of DHP.
- DHH will be the JTAG-"master" for PXD.
- interface to FTSW Nakao-san's trigger distribution board.

Status of DHH: Next Steps

- One DHH board will be shipped to Bonn on Monday 16.01. (today!) for testing serial links over long (~15m) “Infiniband” cables from data PP to DHH, driven by LVDS on DHP frontend side, sending data with "pre-emphasis" (was shown to work by Bonn group)

- Problem with interface to DCE ASIC (cluster finder) was identified, needs high speed serial links.
  probably wrong pins at FPGA in current DHH design,
  will be changed in next iteration.

- Test clock distribution scheme



Slow Control Requirements

- Slow control runs on conventional PC
  - Power & Cooling control
    - PXD PS (for DHP, DCD, switcher and sensors)
    - CO2 two-phase cooling system (one unit, one spare)
    - DHH
  - Downloading FPGA firmware to DHH and ATCA
  - PXD temps. (via PXD PS or DHH ?) and CO2 system temps.
  - DHH temperature, voltages, currents
  - Calculating pedestals, noise and thresholds
    - gets full frame events from DAQ
  - downloading pedestals when needed via Ethernet-DHH link
  - Status information to run control system

Revised Schedule of PXD

(Some) milestones in the PXD construction

finish evaluation of PXD6 (test production):	Oct. 2011
start prototype (PXD9) production	Feb. 2012
power / cooling / DAQ ready (test)	Jan. 2013
Finish prototype production	Feb. 2013
Start final DEPFET production	July 2013
„Telescope Test“ at DESY („full“ DAQ + slow cont.)	Fall 2013
all ASICs produced	Feb. 2014
BEAST II near beampipe ready	Oct. 2014
finish final DEPFET production Batch 1	Feb. 2015
finish final DEPFET production Batch 2	May 2015
power / cooling / DAQ ready (installed)	July 2015

Status of CO2 Cooling

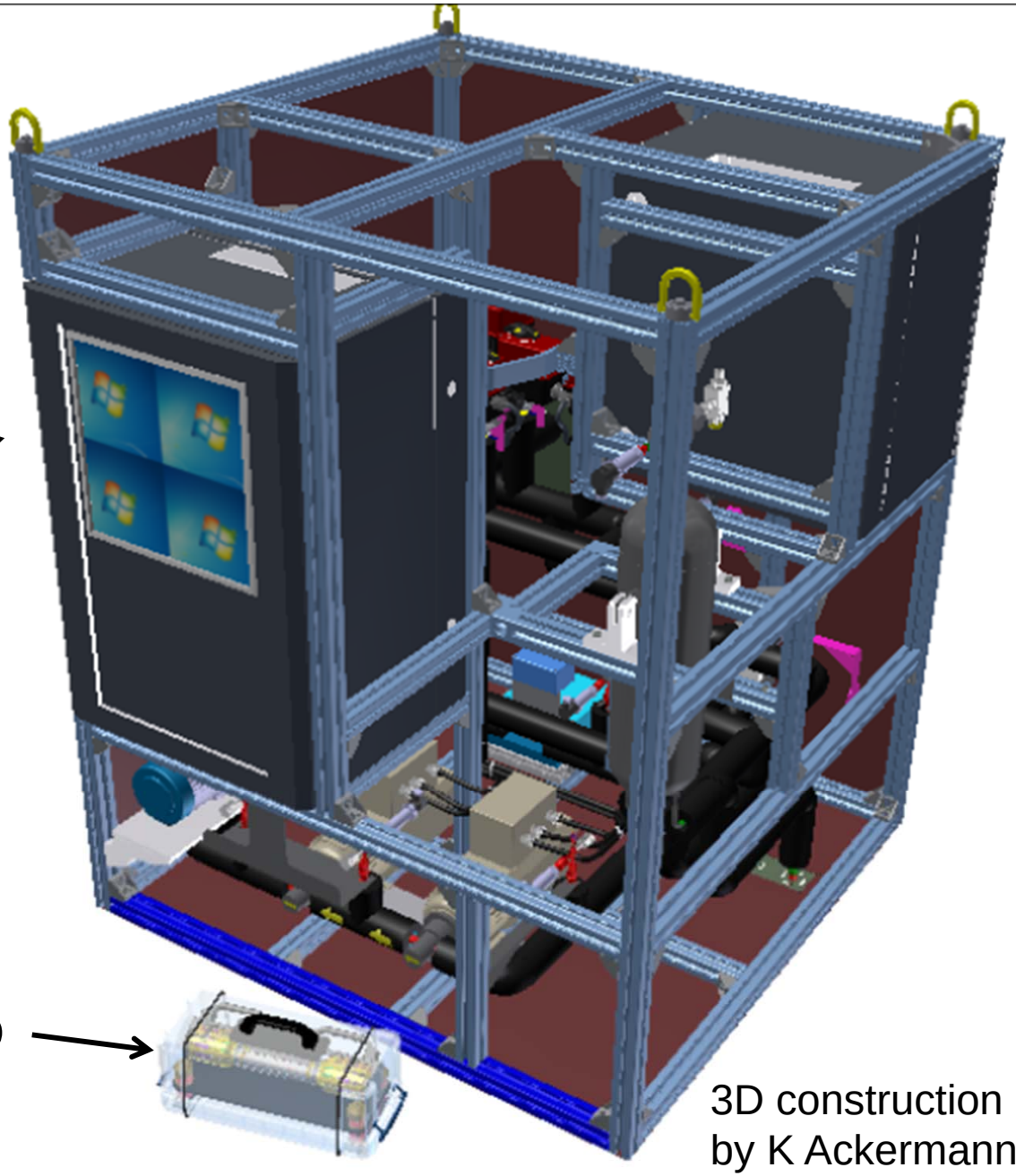
- Build a closed CO2 System for PXD and SVD at MPI with the help of Nikhef/CERN, Vienna, Karlsruhe, now also of DESY
- IBBelle (for ATLAS IBL and Belle II): 2kW unit
- start with
  MARCO (Multipurpose Apparatus for Research on CO2): 1kW unit
  - frame done at CERN by MPI technician
    - all parts from Swagelok have arrived
    - design of MARCO is finalized (K. Ackermann)
    - frame to be equipped by all parts except pipes
  - transport to Munich done on Dec. 20, 2011

CO2 Cooling (cont.)

MARCO 1 kW unit

User control panel (PVSS)

model of PXD



3D construction by K Ackermann

CO2 Cooling (cont.)

- Piping job done at MPI (new orbital welding eqipment) + pressure / leakage tests, finished by February 2012
- Electronic control system (PLC + PVSS) being ordered through CERN
- Electrical installation supported by technician from MPI, start in March 2012
- Commissioning starts in April/May 2012 at CERN
- MARCO ready for transport to MPI by end of June 2012 (available for long-term tests until IBBelle is built)
- Plan: build two IBBelle units to be installed at KEK in 2013