

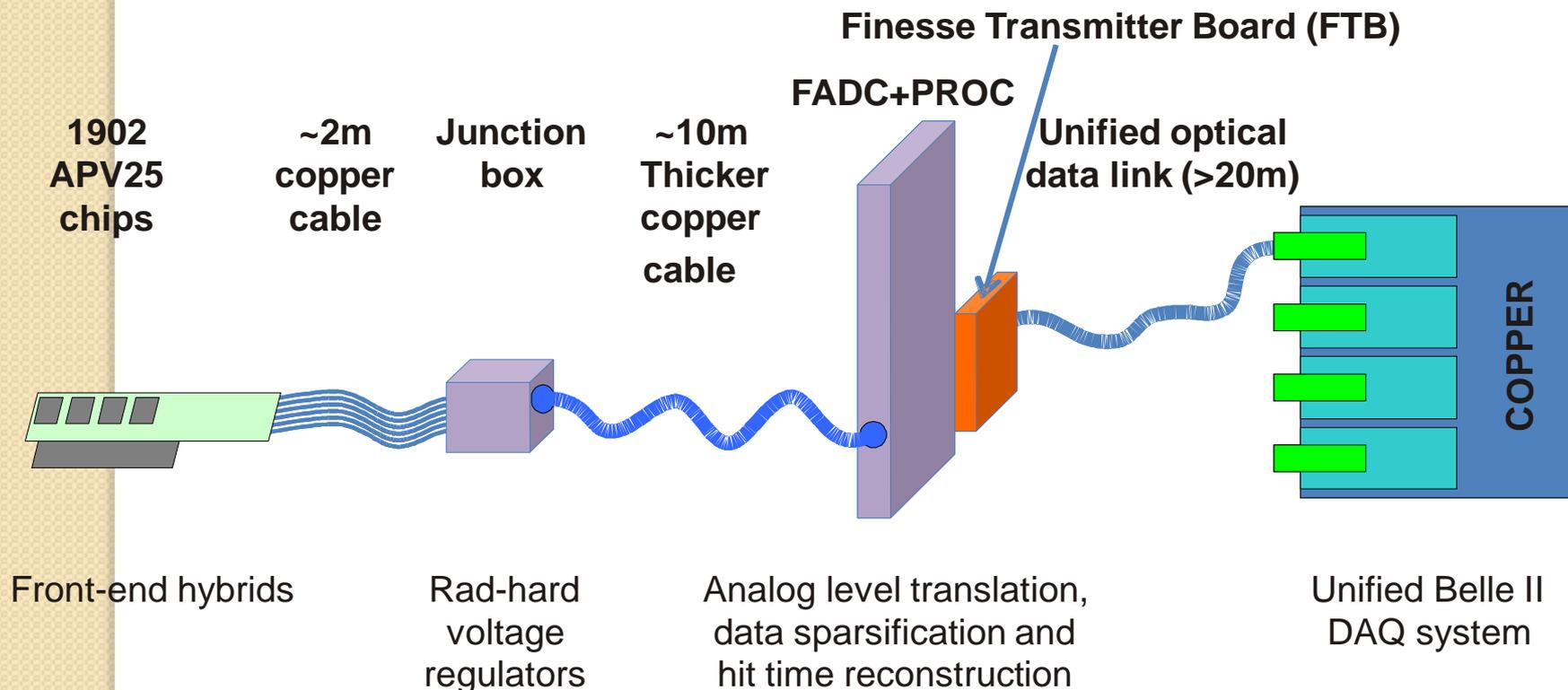


# Status of the SVD DAQ

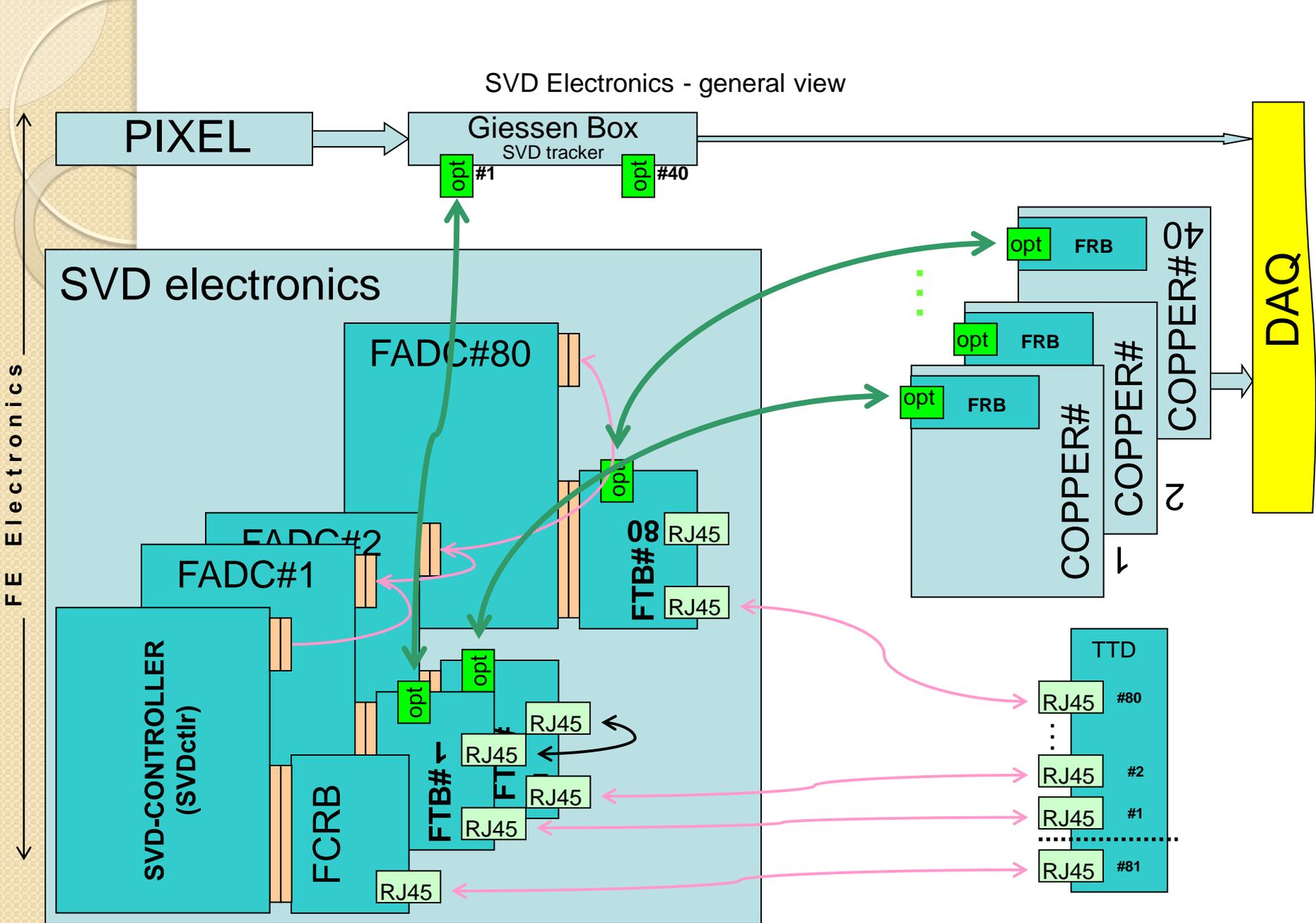
Koji Hara (KEK)

# SVD DAQ System Overview

- Analog APV25 readout is through copper cable to FADCs
- Sparsification and hit time finding is done in FADC modules
- Data is passed on through FTB to COPPER readout system
- Concept verified in beam tests.



# SVD Electronics - general view



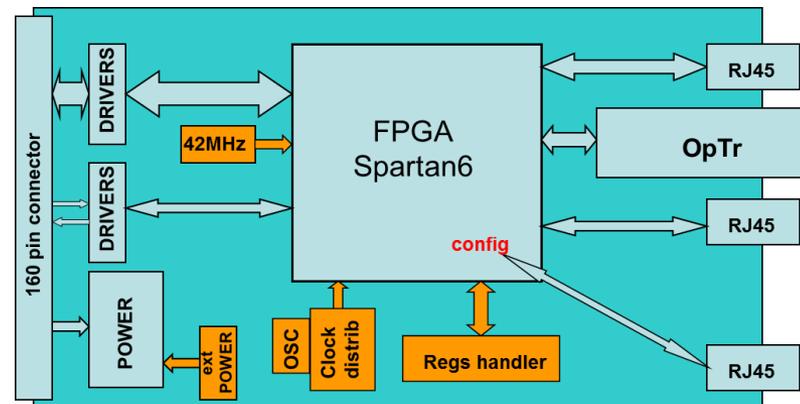
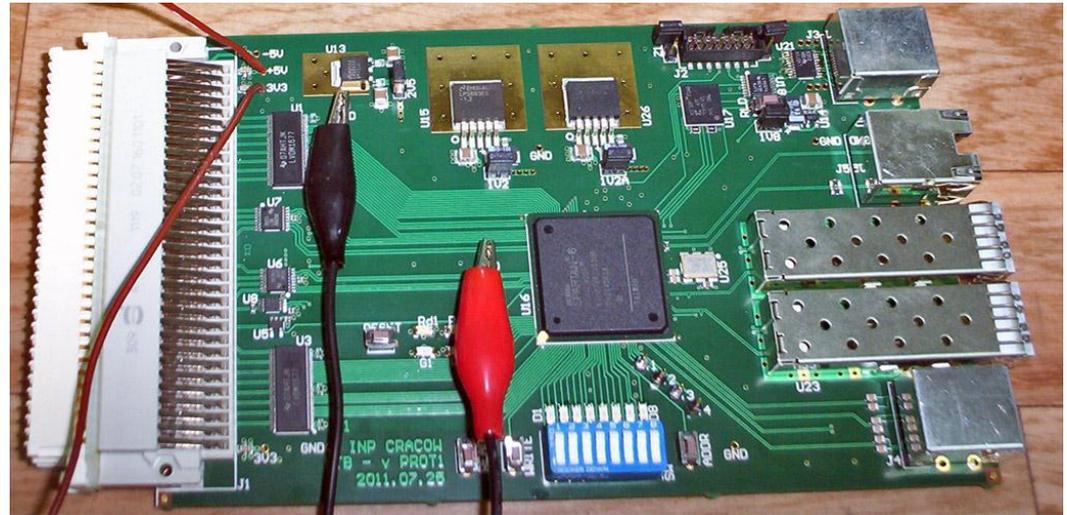
FE Electronics

# Current Status

- **FTB, FADC** designing and prototyping are on-going.
  - The prototypes will be ready in 2012.
    - Goal of 2012 work is to establish the complete readout chain using the FTB and FADC.
- K. Hara and A. Ishikawa (Tohoku) are starting the integration work at KEK. SNU is also willing to join.
  - DAQ test as a whole SVD is planed in mid. 2014.
    - The complete DAQ system must be ready before that at KEK.

# Finesse Transmitter Board (FTB)

- Sends FADC data through optical link to
  - COPPER
  - Pixel system
- Two first prototype boards are being sent to KEK from Krakow for firmware development.

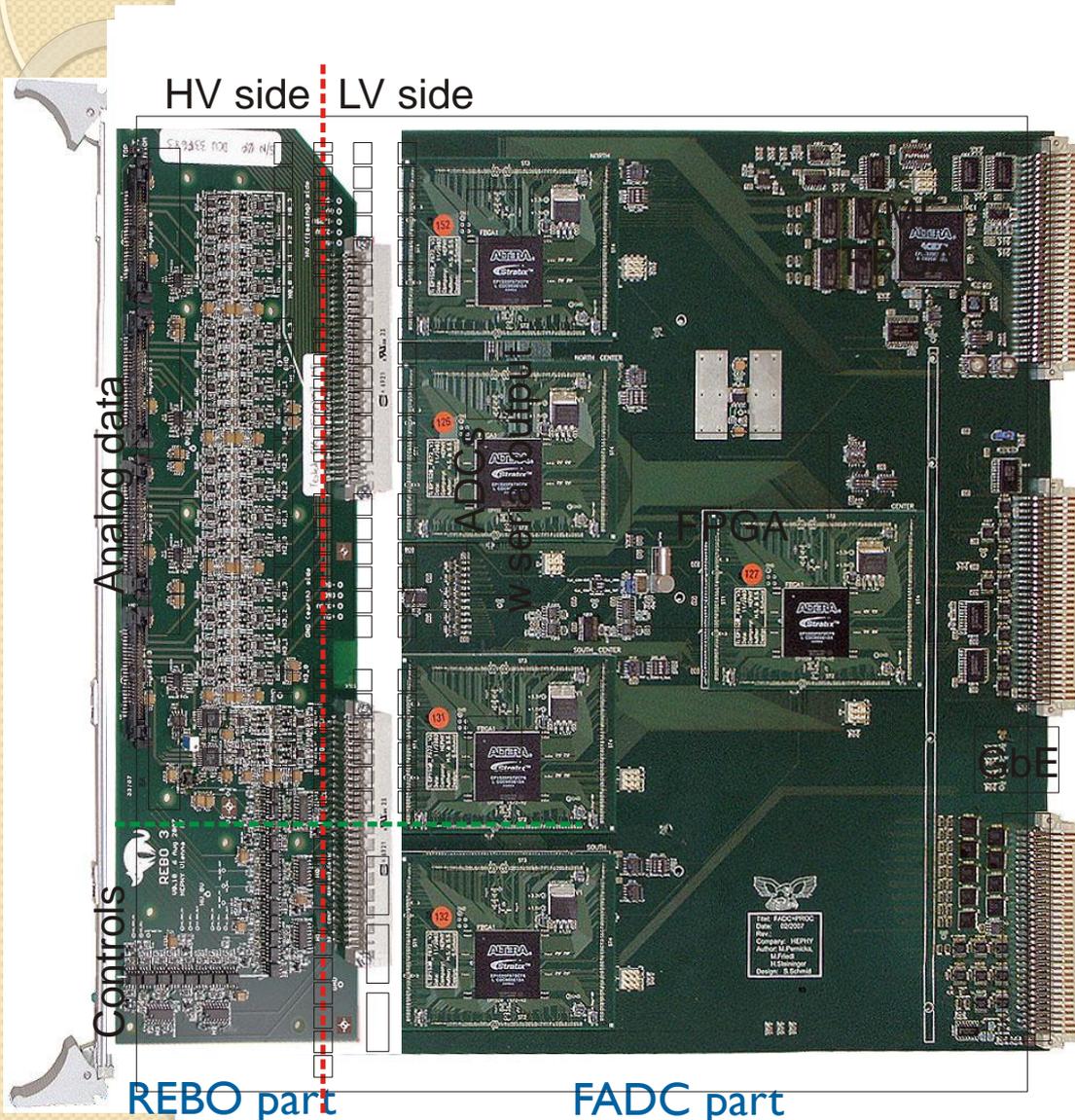


FTB  
functionality  
+ tests  
possibility

FTB components  
+ test components

# FADC

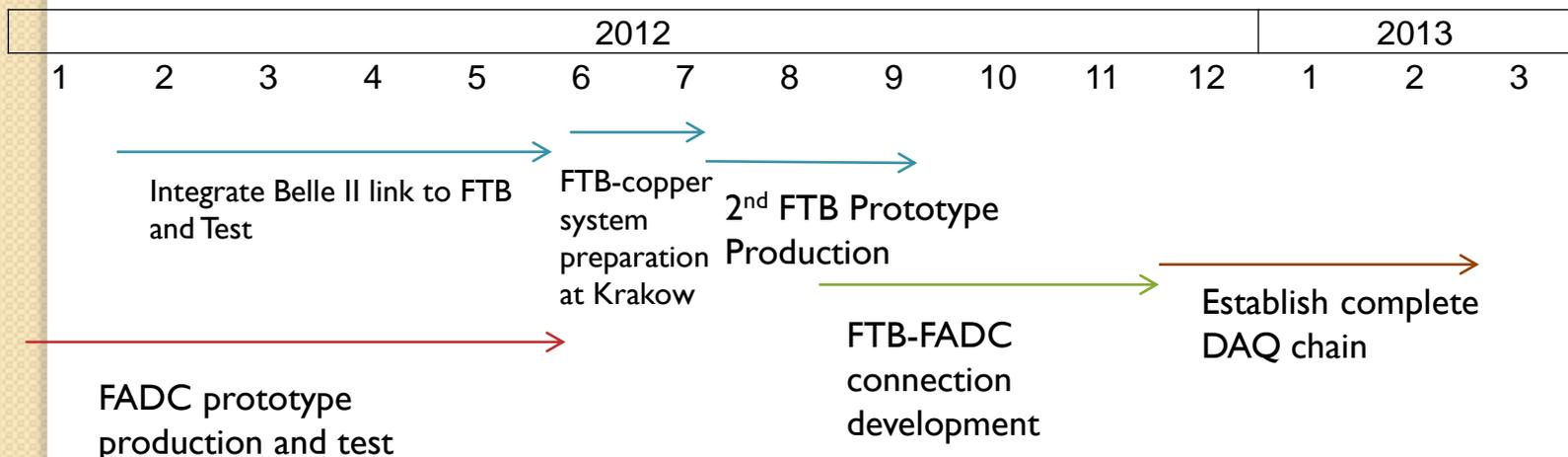
HV side | LV side



- Level translation on the VME board
- Serial output ADCs
- Single powerful FPGA (Altera Stratix 4 GX)
- GbE interface
- Compensation of 30m signal cable by digital Finite Impulse Response (FIR) filter in FPGA firmware
- Hit time reconstruction to reduce occupancy
- 2011-2012 Schedule  
December-January: design  
February: layout & firmware development  
March: prototype production & basic firmware development  
April: assembly & testing

# 2012-13 SVD DAQ Work Plan

- Establish FTB-Copper connection
  - Need to integrate Belle II link to FTB at KEK  
Translation from virtex to spartan is necessary. → SVD
    - Hara, Ishikawa (Tohoku), Joo (SNU) and Wacek (Krakow) will work on that.
- Establish FTB-FADC Connection
  - FTB-FADC development at Krakow
- Establish APV25-FADC-FTB-Copper chain by 2013 BPAC



# Summary

- SVD DAQ concept verified in beam tests.  
→ Developing Belle II full DAQ chain
  - Hara and Ishikawa starting integrating work at KEK.
- FTB and FADC prototypes are being produced.  
→ Firmware development will be done to establish the connection.
  - Need to translation Belle II link to spartan6
- Establish full DAQ chain by 2013 BPAC



# Prototype - tests setup

