TOP Electronics Status & Beam Test Experience

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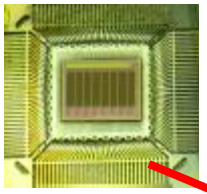
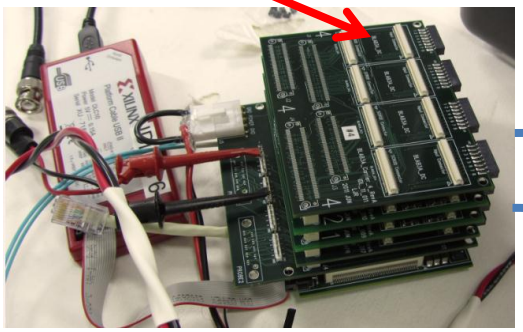
University of Hawaii
Belle II TRG/DAQ Workshop

Electronics Elements

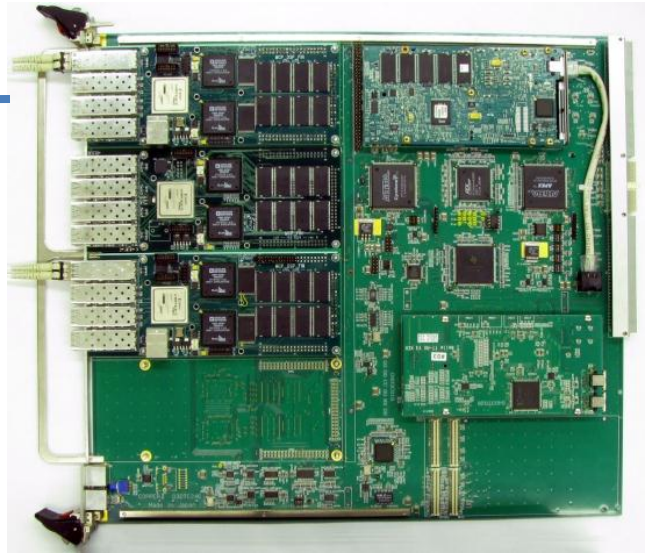


Waveform sampling ASIC (IRS2/3)



SCROD-based board stack (Spartan-6)

Aurora-based fiberoptic data



DSP_FIN (Virtex-4)

Aurora-based fiberoptic trigger

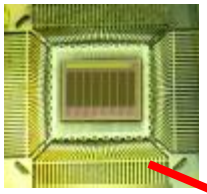
Timing/trigger distribution (CAT-7)

FTSW

TRG_FIN (Virtex-4)

Remote programming link (CAT-7)

Beam Test Electronics Elements



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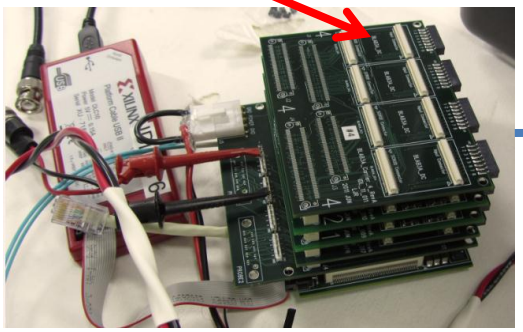
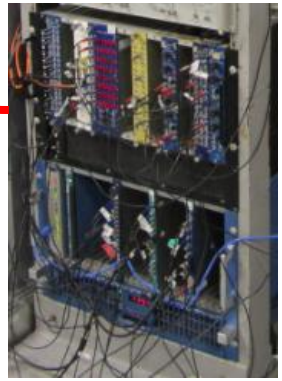


SCROD-based board stack (Spartan-6)

Timing/trigger distribution (CAT-6)

DSP_cPCI (Spartan-6)

FTSW



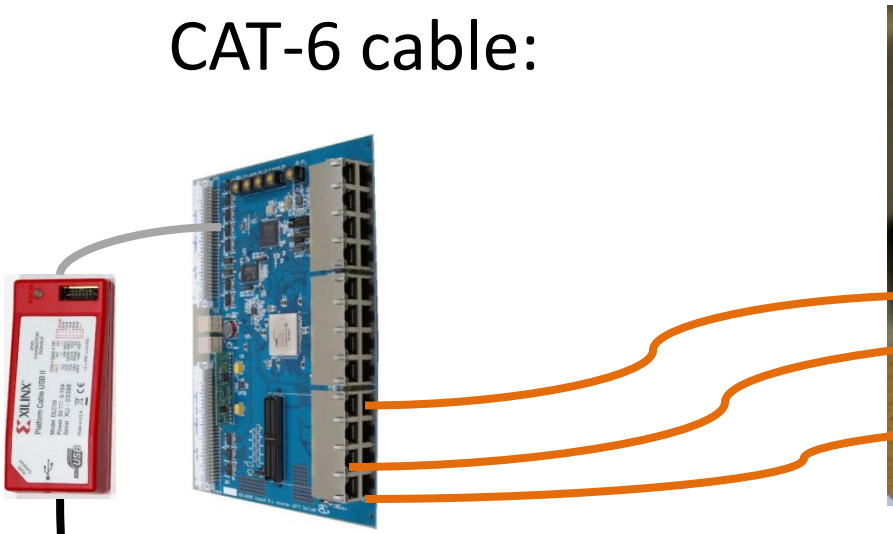
NIM trigger logic

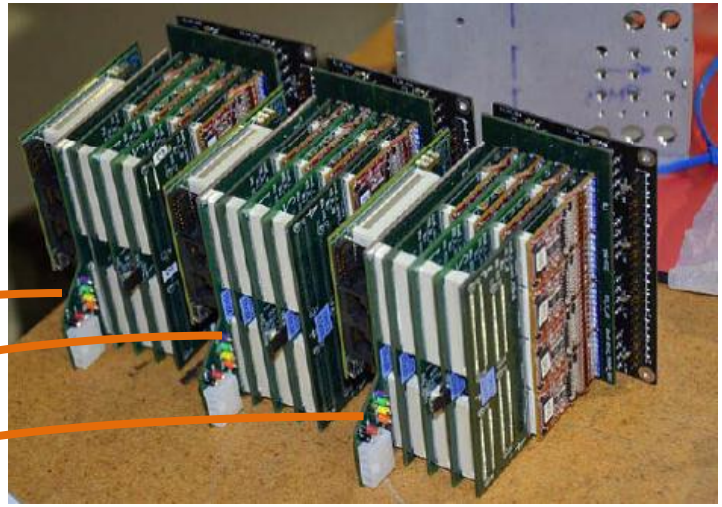
CAMAC TDC (trigger phase alignment)

Remote programming link (CAT-6)

Remote Programming

- JTAG programmer connects to FTSW, FTSW distributes to one or more front-end modules via CAT-6 cable:





- **Generally quite successful. A few issues:**
  - Programming sometimes worked at 6 MHz…
  - …but often had to be run at 1.5 or 0.75 MHz.
  - Sometimes failed completely. Reseating cables seemed to help, but there was never an obvious cause.

Timing/Trigger Distribution

- Clock strategy:
  - Derive 21 MHz clock from FTSW-distributed 127 MHz.
  - 21.2 MHz clock must be phase aligned across all modules.
- Serial data stream from FTSW is used to divide and synchronize clocks across all modules*. Some caveats:
  - Timing constraints are very tight.
  - Could only get this firmware to act stably by manually specifying the location of the PLL:

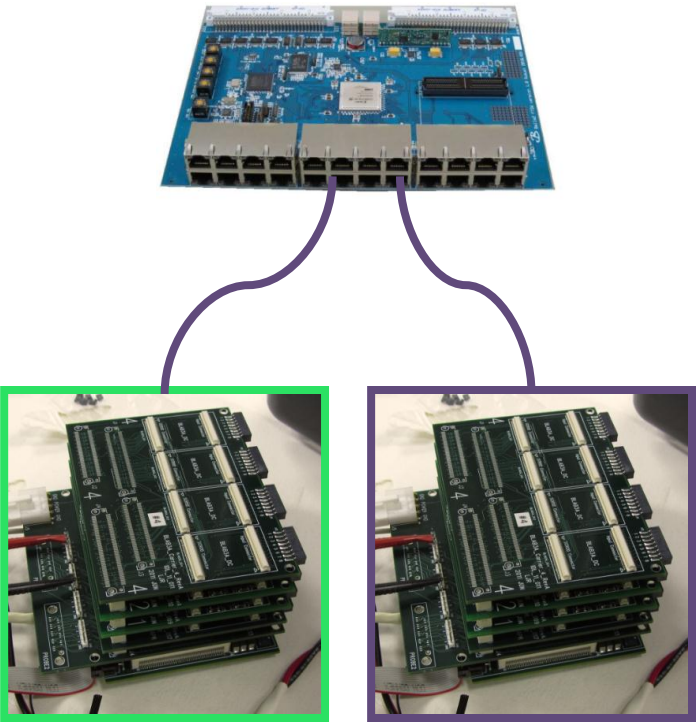
```
#The location of the FTSW receiver PLL seems to only work in specific locations.
#The one below is verified working... others may also work but have not been
#systematically tried.
INST map_clocking_and_ftsw_interface/map_FTSW_interface/map_belle2clk/map_pll/map_pll  LOC = PLL_ADV_X0Y0;
```

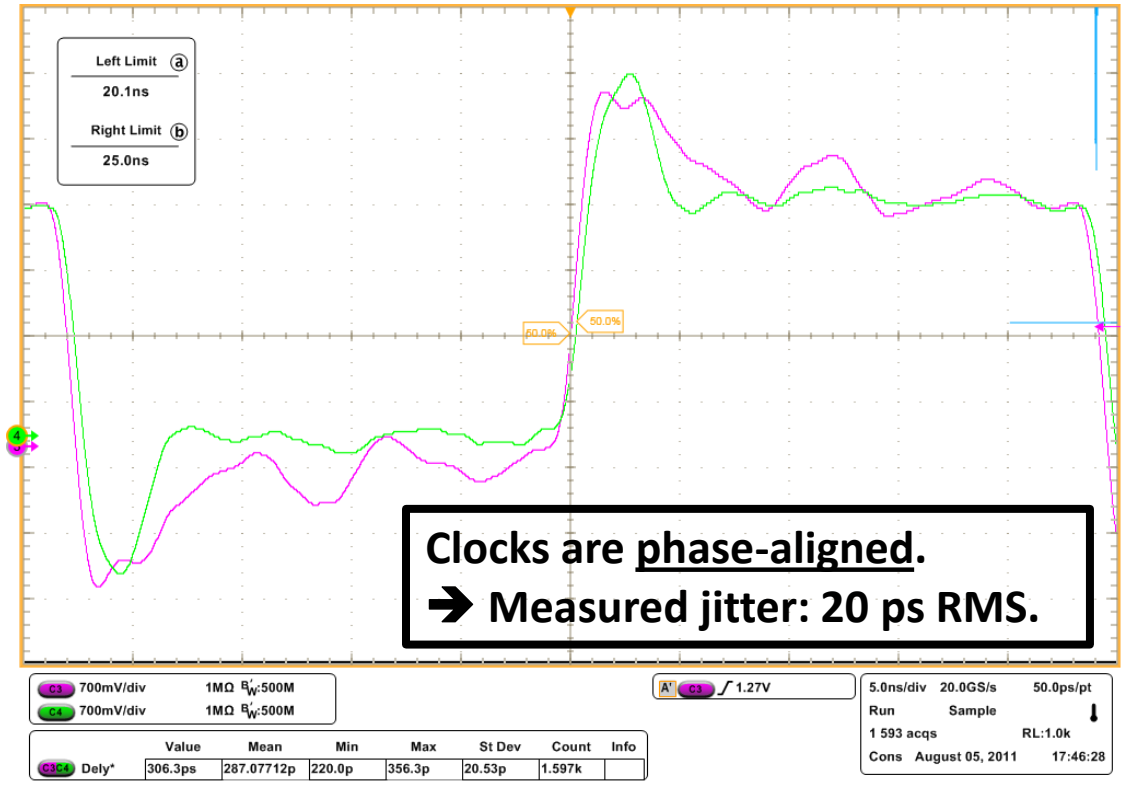
  - If this timing link is ever lost (cable unplugged, high noise, etc.), it never recovers. Could be Spartan-6 limitation?
  - When timing link is down serial trigger stream decoder finds triggers constantly.
  - CAT-6 cable was found to be much more reliable than CAT-7.

*Thanks to Nakao-san for this code!

Timing/Trigger Distribution

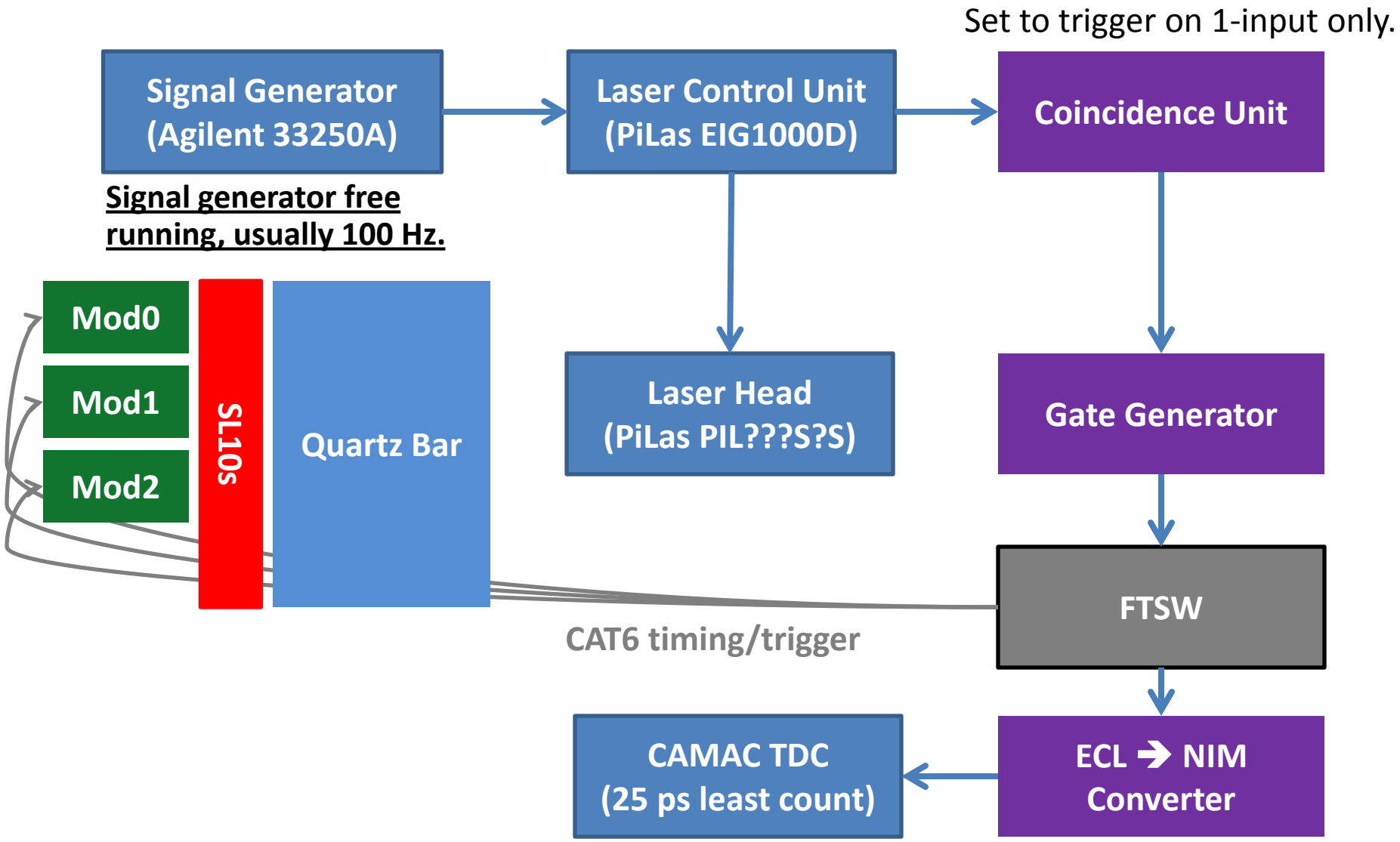
- Timing results from bench test between two SCRODs in August 2011:





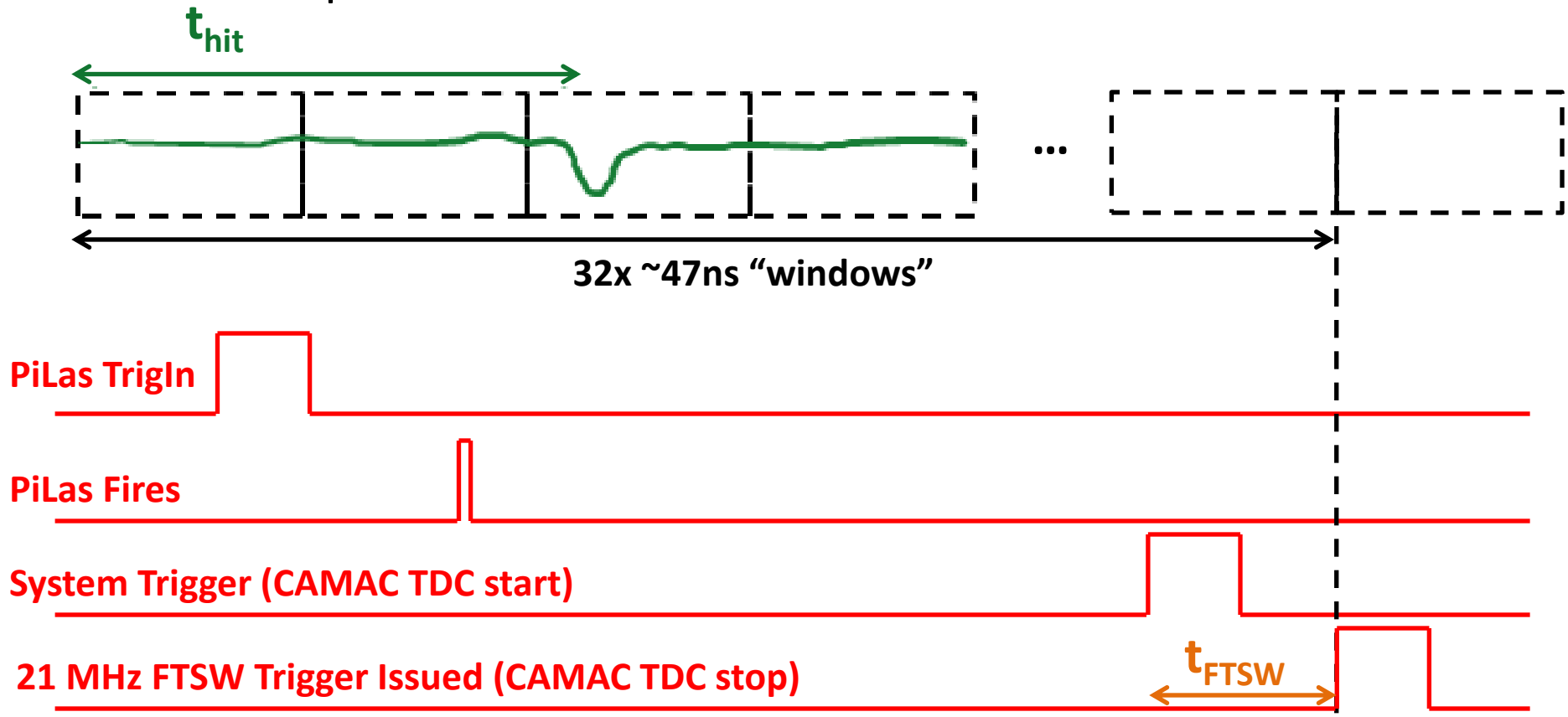
Measured phase and jitter of 21.2 MHz clock from two SCRODs (on oscilloscope)

Beam Test Timing - Standard Laser Runs



Standard Laser Runs - FTSW Timing

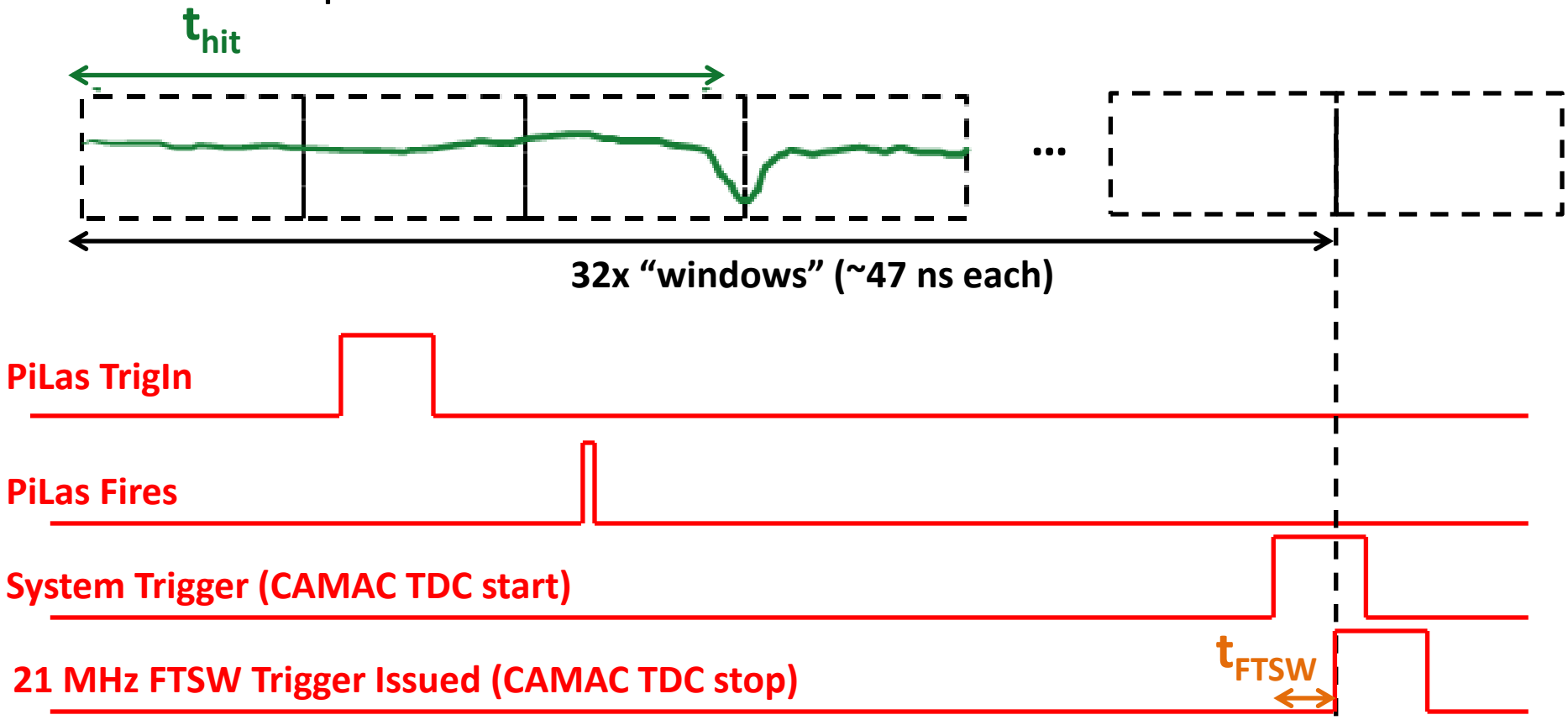
- Events are random with respect to FTSW trigger…
  - …but laser fires at a fixed time relative to the global trigger.
  - Example 1:



Smaller t_{hit} ➔ larger t_{FTSW}

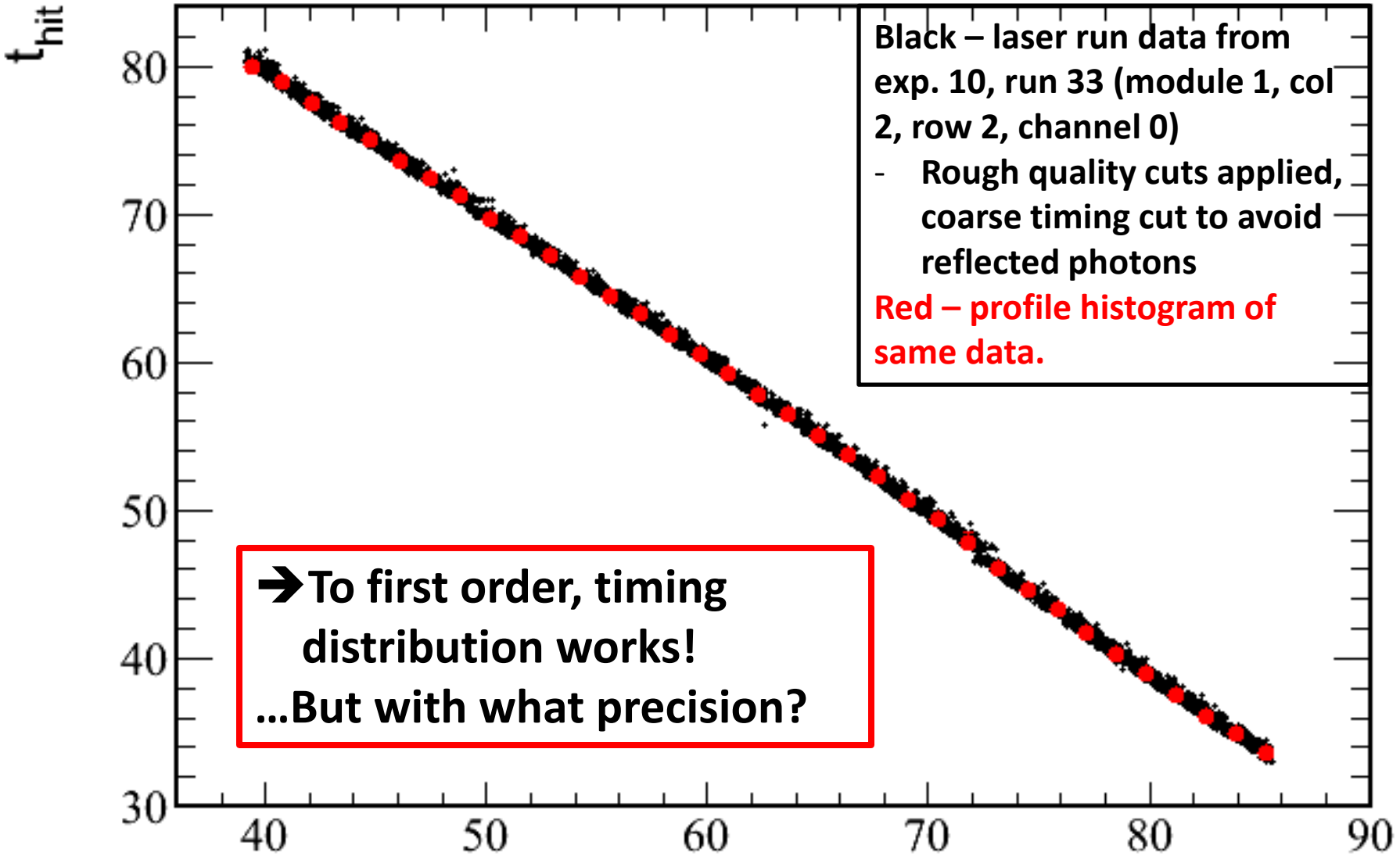
Standard Laser Runs - FTSW Timing

- Events are random with respect to FTSW trigger…
  - …but laser fires at a fixed time relative to the global trigger.
  - Example 2:



Larger t_{hit} ➔ smaller t_{FTSW}

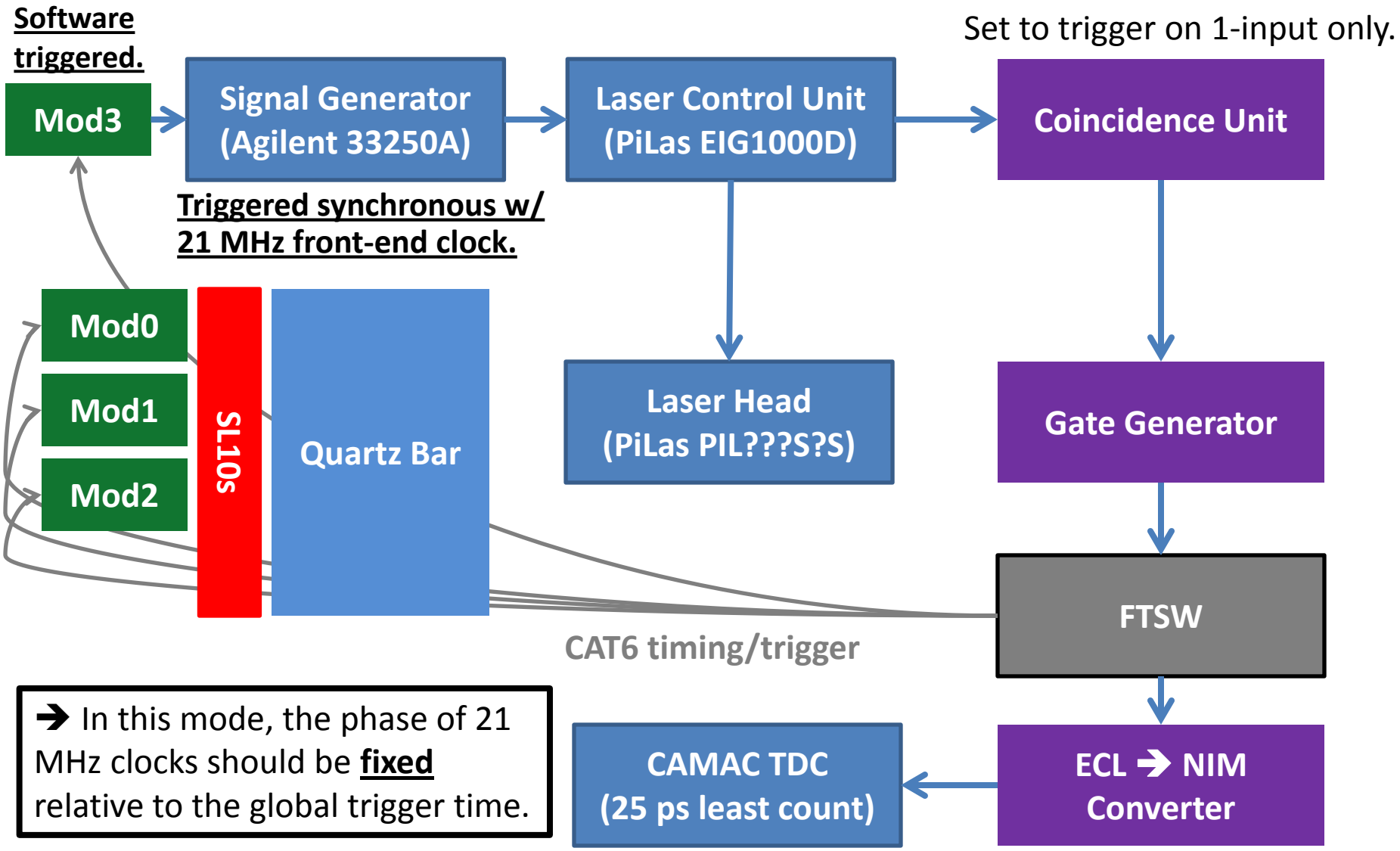
Standard Laser Run - Distributions



No fine calibration applied: assumed 2.7 GSa/s for all samples; 25 ps / count for CAMAC TDC.

Time extracted by software fixed threshold discrimination (-40 ADC counts).

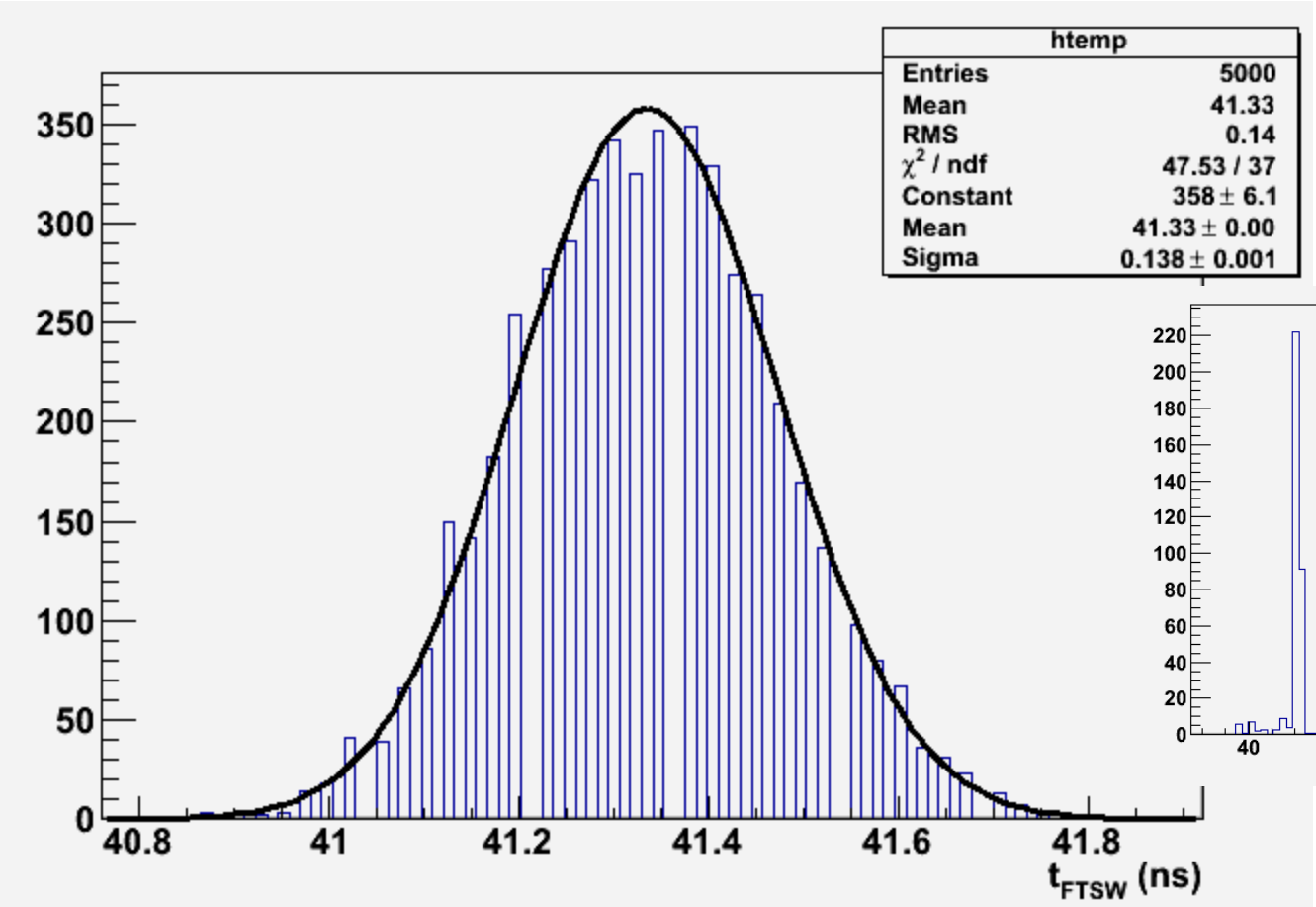
Beam Test Timing – "Special" Laser Runs



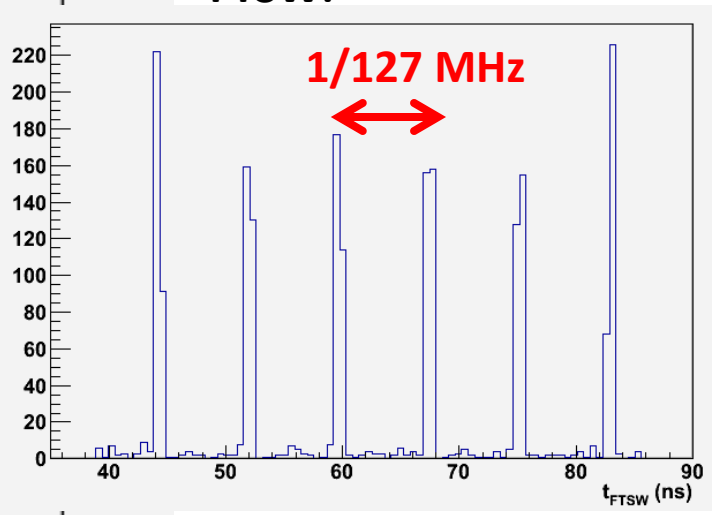
➔ In this mode, the phase of 21 MHz clocks should be **fixed** relative to the global trigger time.

Measured FTSW Timing - “Special” Laser Runs

- Typical TDC distribution of trigger phase:



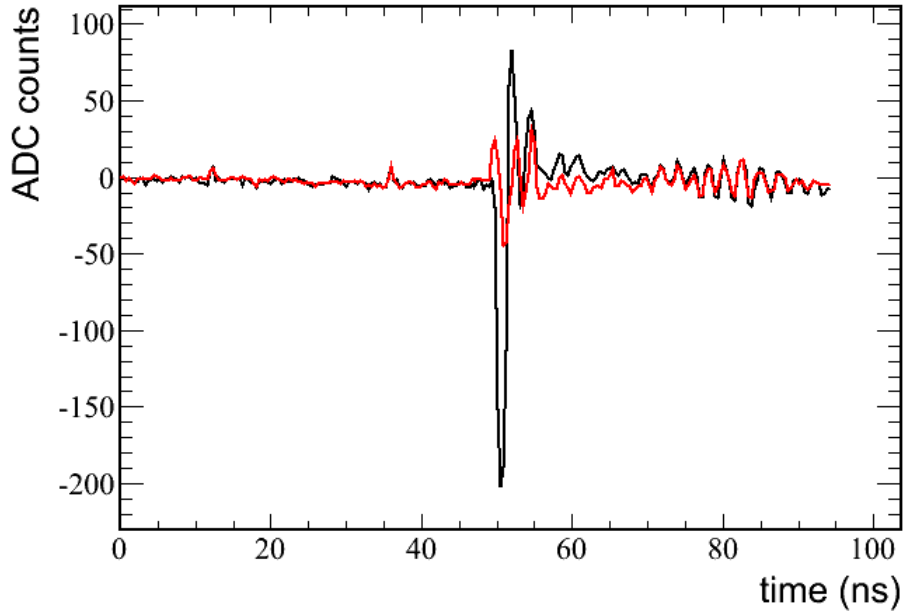
Trigger phase measurements when module loses its synchronization with FTSW:



➔ Absolute global time resolution will never be better than this!

Is this due to intrinsic jitter in timing distribution, or jitter in the measurement?

Other issues: Waveform Processing



Example SL10 waveform froms beam data:

Black – primary hit

Red – cross talk on an adjacent channel

- Simplified waveform processing plan:
  - Each DSP core feature-extracts hits from a single SCROD.
    - Hits are processed independently. Pedestal subtraction, timing calibration are applied. Then Calculated charges/times are sent on to final system.
- More realistic plan:
  - Pedestal subtraction, timing calibration applied.
  - DSP cores need to be aware of potential cross-talk hits from other anodes in the MCP-PMT. Feature extraction proceeds based on all available waveforms from a given PMT.

Plans for Jitter and Waveform Studies

- When equipment returns from Fermilab (in transit now):
  - Replicate test beam setup as closely as possible.
  - Run with pulser as input to front-end:
    - Take an auxiliary calibration sample for further timing calibrations and controlled timing studies.
  - Run with laser:
    - Determine main sources of jitter in timing phase measurement.
      - Is it in the timing distribution itself or in the phase measurement?
  - Waveform analysis campaign:
    - Identify different types of PMT-hits, cross-talk, and pathologies.
    - Develop methods for identifying each in the data stream.
    - Determine best possible timing resolution in laser runs.
    - Reprocess raw beam test data with improved calibrations and methods.

➔ Waveform studies will feed into future work on DSPs.

TOP Summary

- TOP beam test at Fermilab:
  - First system-level test of many components & features.
  - Lots of data, millions of photon candidates.
  - Analysis will be ongoing for some time… but we already some valuable feedback:
    - Remote programming can be tricky. Slower programming speed can help.
    - Timing distribution issues: tight timing requirements in firmware, no recovery when timing "lock" is lost (Spartan-6 issue?).
    - Distributed timing jitter: still under investigation… much worse than originally thought? If so, why?
    - DSP waveform processing scheme for final configuration may need to be considerably more complicated.
  - Great progress over the past year, but lots of work left to do before we're ready for "prime-time."