Status of Aerogel RICH Readout

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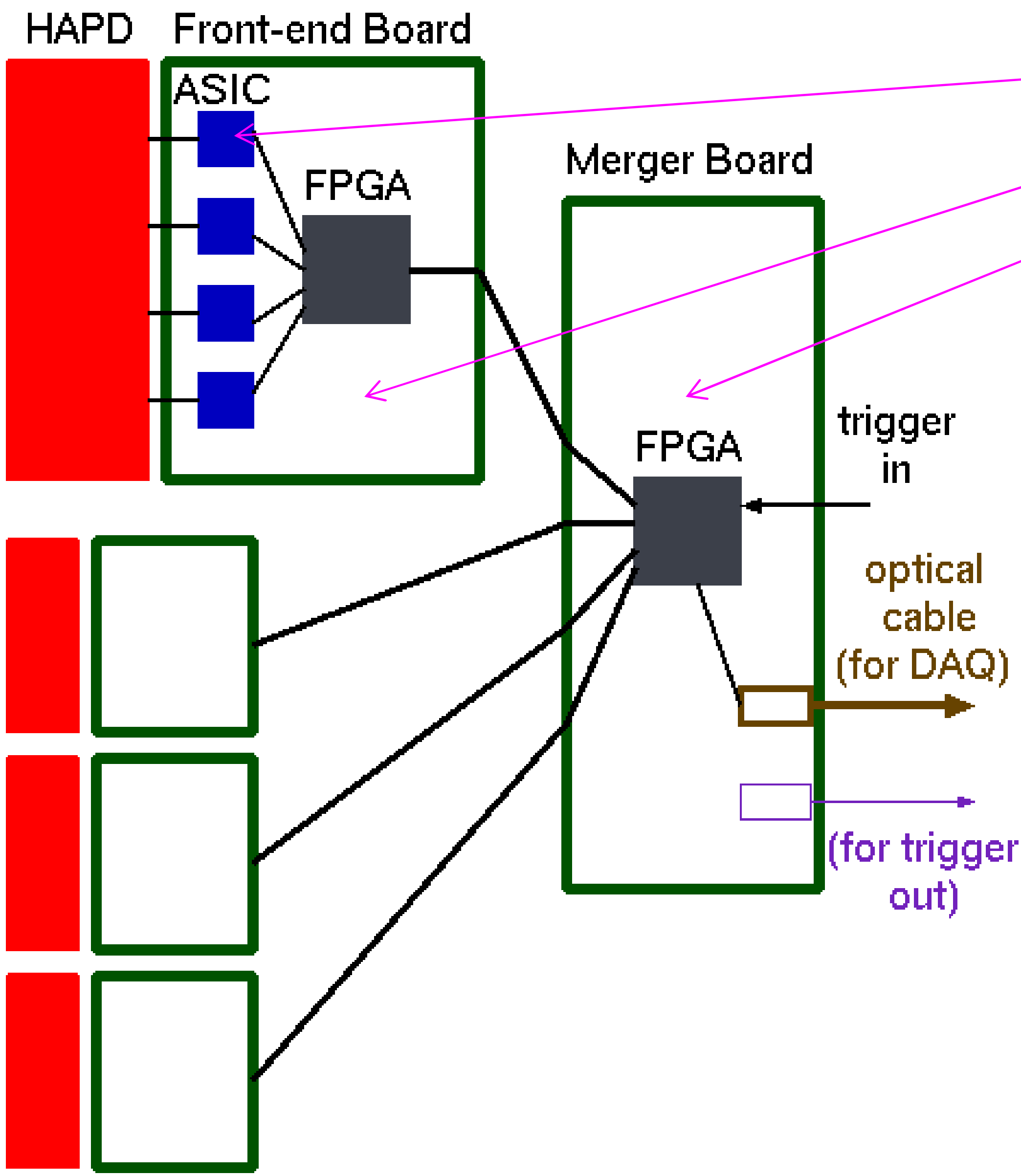
KEK

Belle II Trigger DAQ Meeting in Hawaii

Jan. 16, 2012

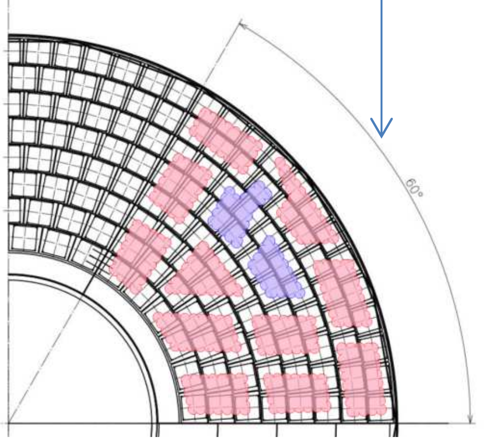
Aerogel RICH Electronics



Development Items:

- ASIC
- Front-end Board
- Merger Board

- Total 456 HAPDs.
- 456 Front-end (FE) Boards.
- 78 Merger Boards
  - ✓ 1 Merger ↔ 5-6 FE Board
- ASIC: 36ch per chip (i.e. 4 chip / HAPD).
- Quite limited space (~5cm) behind HAPD.



Aerogel RICH Electronics

	#ch	occ [%]	#link	/link [B/s]	FNS	#CPR	ch sz [B]	ev sz [B]	total [B/s]	/CPR [B/s]
PXD	8M	2	40	364M	—	—	4	320k	14.4G	—
SVD	243456	1.9	40	13.8M	HSLB	40	4	18.5k	555M	13.8M
CDC	15104	10	302	0.6M	HSLB	75	4	6k	175M	2.3M
BPID	8192	2.5	128	7.5M	DSP	16	16	4k	120M	8M
EPID	77760	1.3	138	0.87M	HSLB	35	0.5	4k	120M	15M
ECL	8736	33	52	7.7M	HSLB	26	4	12k	360M	15M
BKLM	21696	1	86	9.7M	DSP	6	8	2K	60M	10M
EKLM	16800	2	66	19.5M	DSP	5	4	1.4k	42M	5.3M
TRG					HSLB	60				

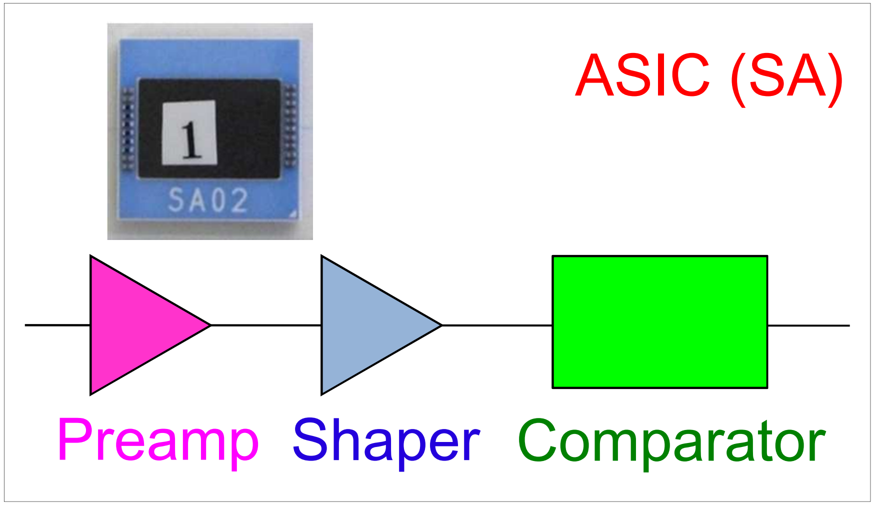
65664 1.5 78 1.1M 20? 2.8 2.8k 86M 2.2M?

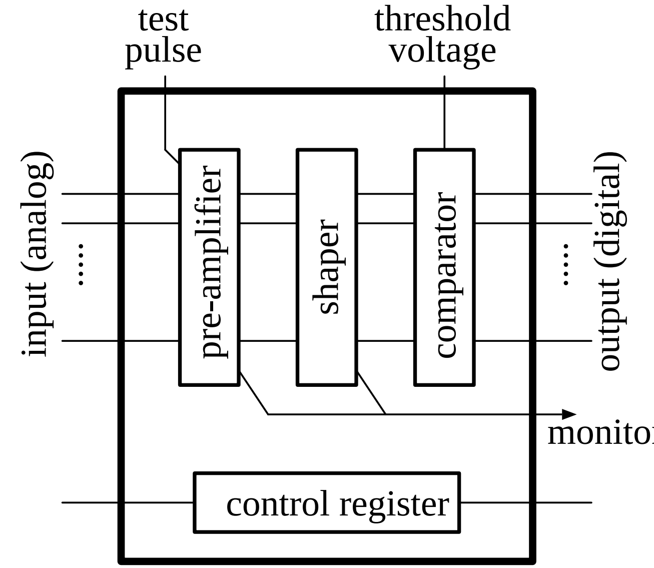
Change due to

- Reduced number of HAPD (540 → 456: forgot to update from long ago).
- Update of merger configuration.
- Some mistake in the previous calculation?

Readout ASIC (SA)

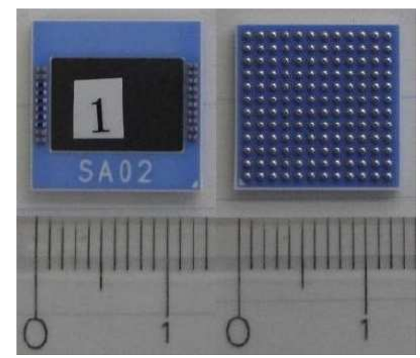
HAPD
(144ch)





- SA01 (2007)
  - ✓ 12ch only. QFP package.
  - ✓ Gain too high.

- SA02 (2009)
  - ✓ 36ch only. Gain adjusted (1/4 of SA01).
  - ✓ Low-temperature cofired ceramic (LTCC) package.
  - ✓ Front-end board produced and tested (later).



- SA03 (2011)
  - ✓ Shorter shaping time for neutron irradiation of HAPD.

QFP version

SA03

SA03

- Shorter shaping time.
  - ✓ Larger noise (worse S/N) in neutron irradiated HAPD.
  - ✓ SA02 : 250ns – 1000ns
  - ✓ SA03 target : reduce to half of SA02
- Tolerance to a single event upset (SEU).
  - ✓ ASIC itself is radiation tolerant (tested with SA02).
  - ✓ SEU may affect parameters in SA02.
  - ✓ Dual interlocked cell (DICE) for registers.
  - ✓ Non-destructive parameter readout.

First samples by TSMC were delivered in Sep. 2011.
Production at X-FAB is also going.

Available SA03 at 2012 Mar. (expectation)

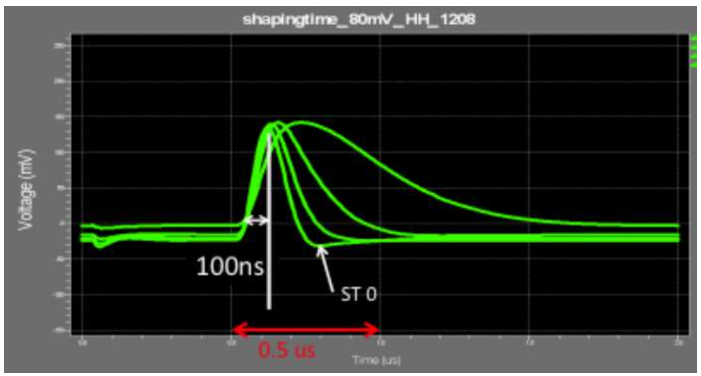
	bare chip	QFP	LTCC
TSMC	40	5	30
X-FAB	~30	5	

LTCC package for SA03 is also in production.

SA03 Shaping Time

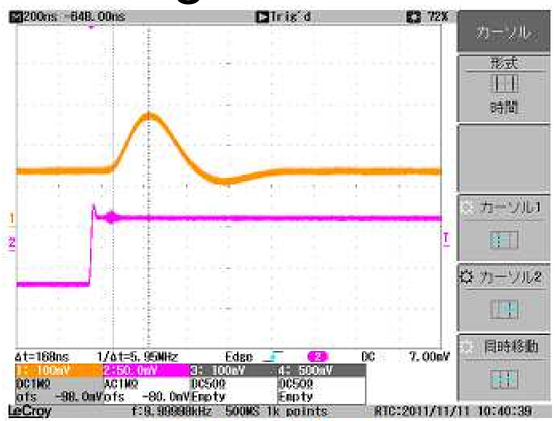
- Basic function of SA03 basically looks O.K.
  - ✓ Non-destructive parameter readout.
  - ✓ Noise level, linearity, offset adjustment.
- However, shaping time may not be as short as expected.

Simulation



Minimum shaping time = 100ns

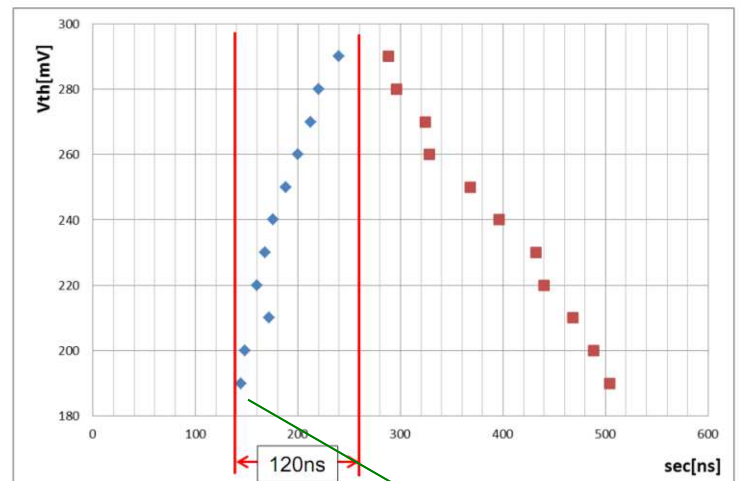
Analog monitor



ST0 : 170 ns

170ns

Vary threshold and check the digital output



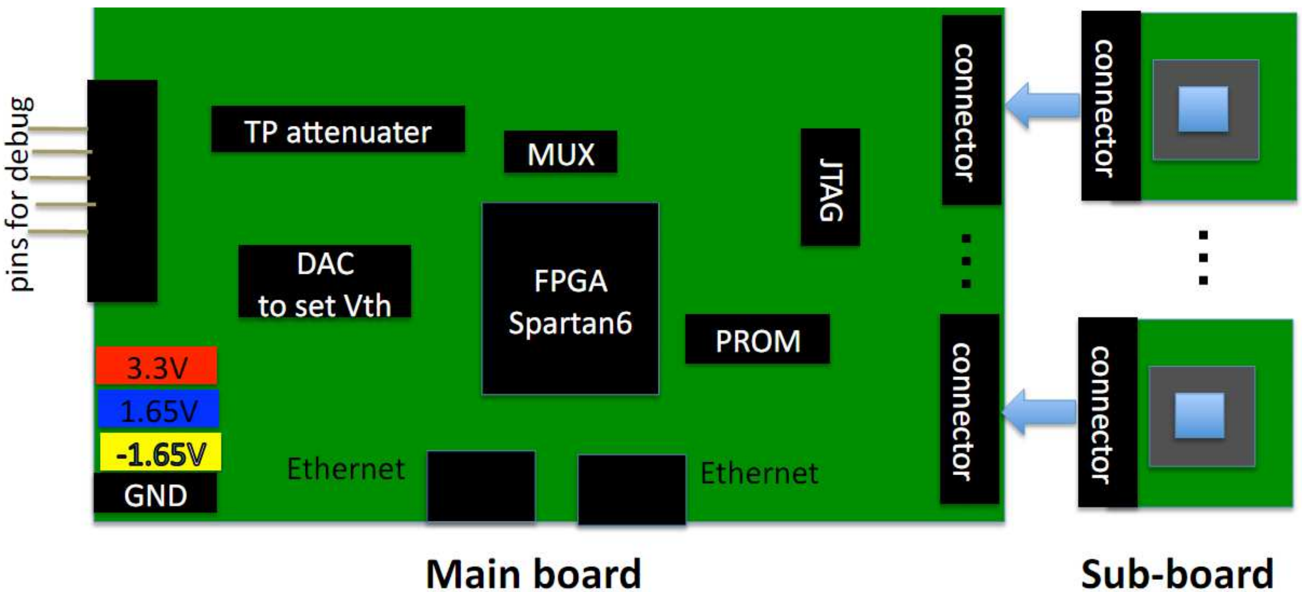
120ns-150ns

this level is not the ground level of this channel.

SA03 Plan

- Test of SA03 with (neutron-irradiated) HAPD.
  - ✓ S/N difference between SA02 and SA03 for neutron irradiated HAPD (higher leakage current).
- If the performance of SA03 is O.K., we will move to mass production.
  - ✓ Depends on final decision of HAPD specification (2012 summer) and neutron irradiation test.
  - ✓ TSMC or X-FAB ?
  - ✓ Mass production of packaging (LTCC) still needs more investigation.
- Test system of SA03 (after mass production) is also in development

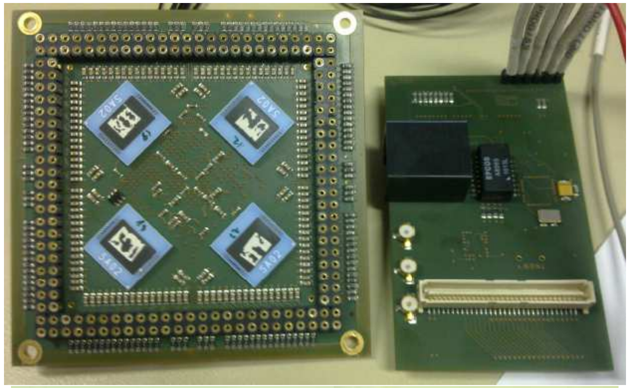
[H. Takagaki]

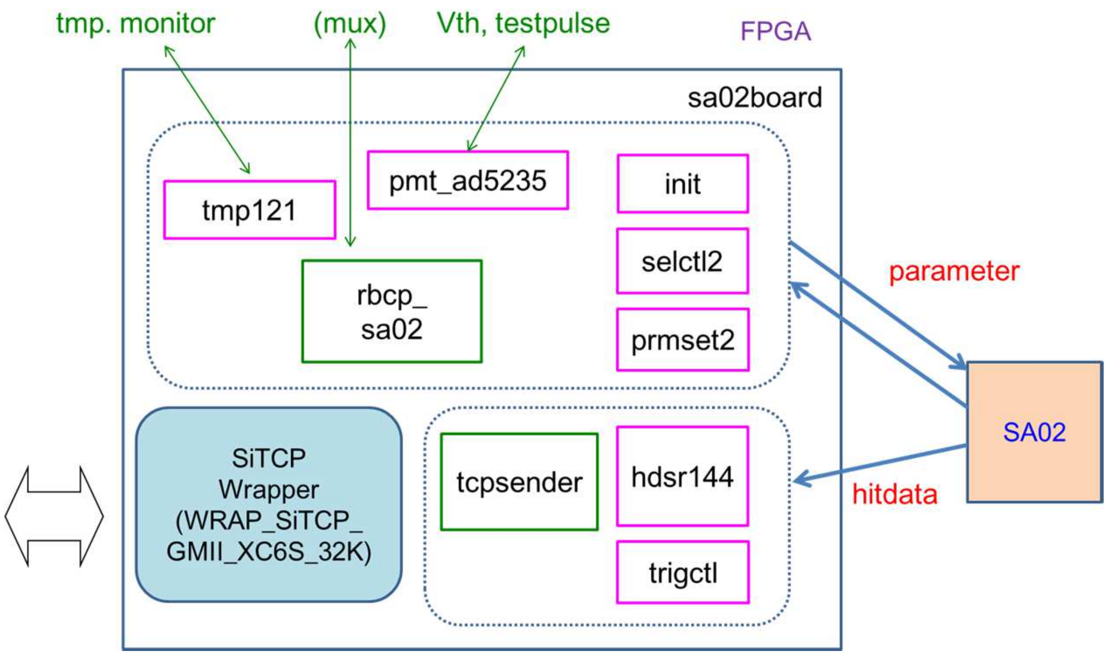


6 sub-boards (6 ASICs can be checked at the same time).

Front-end Board

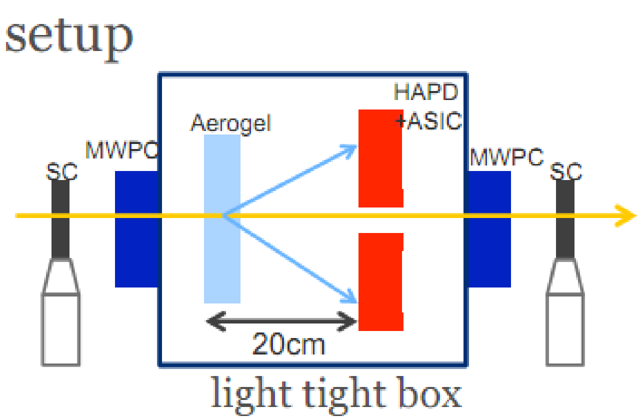
- 2nd version of the prototype front-end board was developed in Ljubljana.
  - ✓ Main board with 4 SA02 ASICs and 1 FPGA (Spartan6).
  - ✓ Sub-board for SiTCP (stand-alone readout).
  - ✓ Production at Elgoline (Slovenia).
  - ✓ Fit in the actual available space.
- Logic for FPGA was developed and tested.

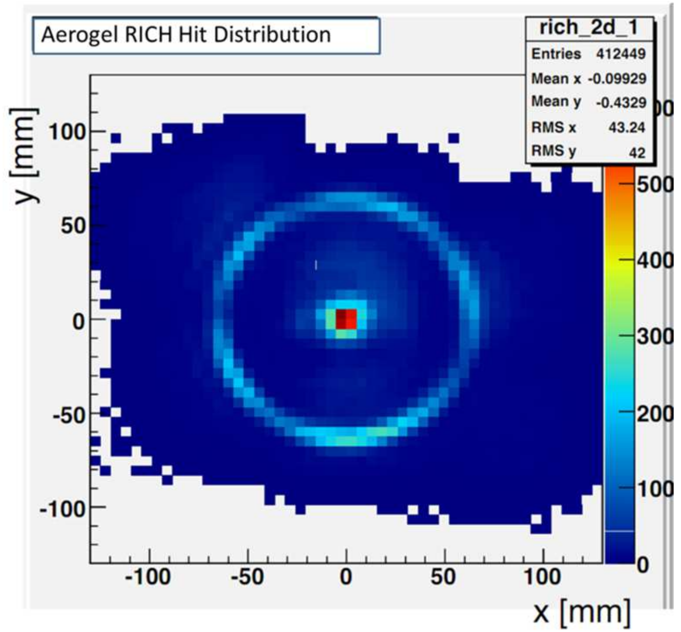




Front-end Board

Beam test at CERN SPS (12 GeV proton)



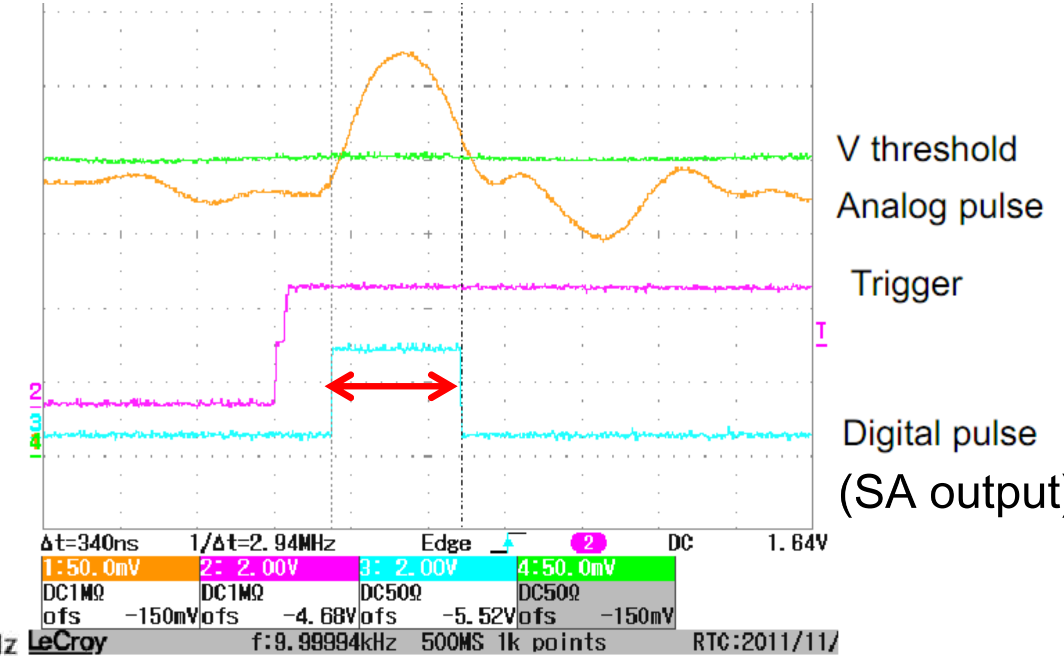


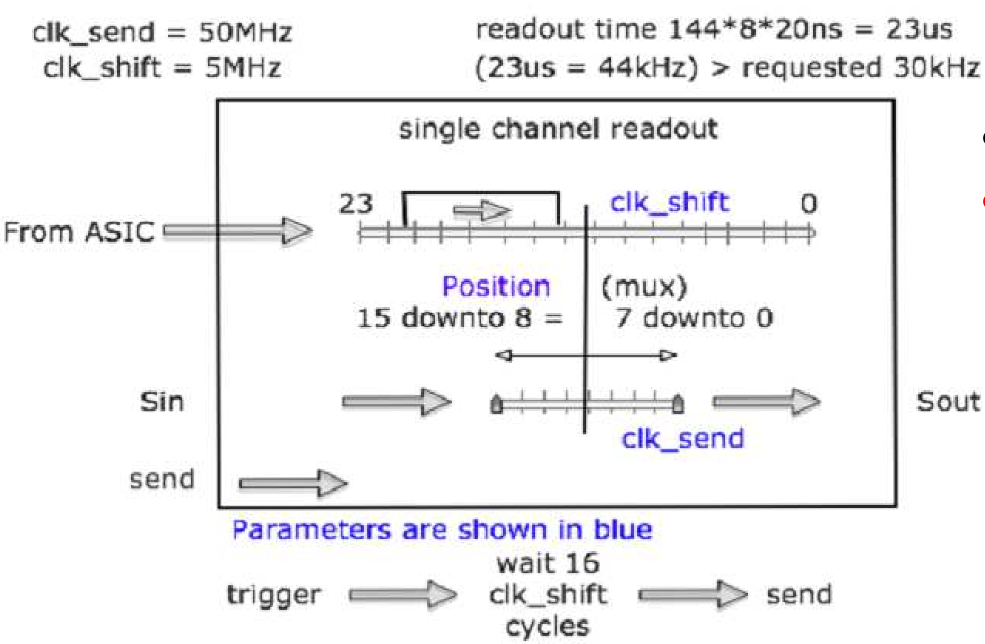
- In the beam test, the data was readout through I/O port of the FE board by VME I/O module (PTS module), in order to synchronize with other VME modules.
- SiTCP was used only for parameter setting.
- Clear Cherenkov ring is observed. O.K.
- Known problem: one of 4 chips has larger noises. Not yet solved.

Front-end Board

Possible improvement

- Now, we only readout on/off information for each channel (4 timings every 2us).
- If we measure the time over threshold, we may be able to distinguish single and multiple photons.



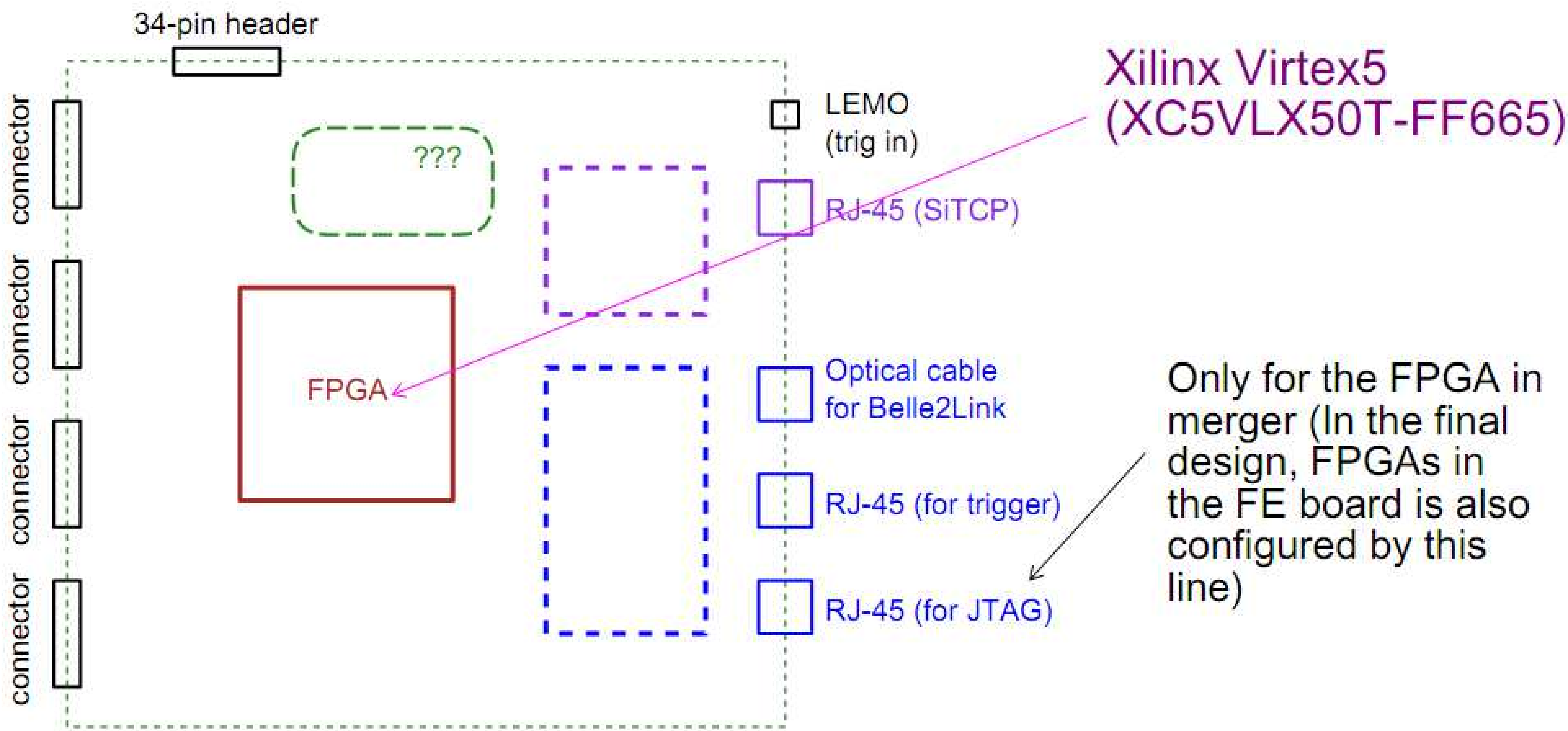


- The logic is in study in Ljubljana.
- This increases the data size.
  - ✓ 1 hit : 18(chID) + 4(hit)
    = 22 bit
    → 18 + 4 +8(?) = 32 bit
  - ✓ Not significant to Belle2Link
  - ✓ More impact on the connection between FE and mergers.

Merger

Prototype merger board was produced.

[shown in the Trig/DAQ meeting last year]

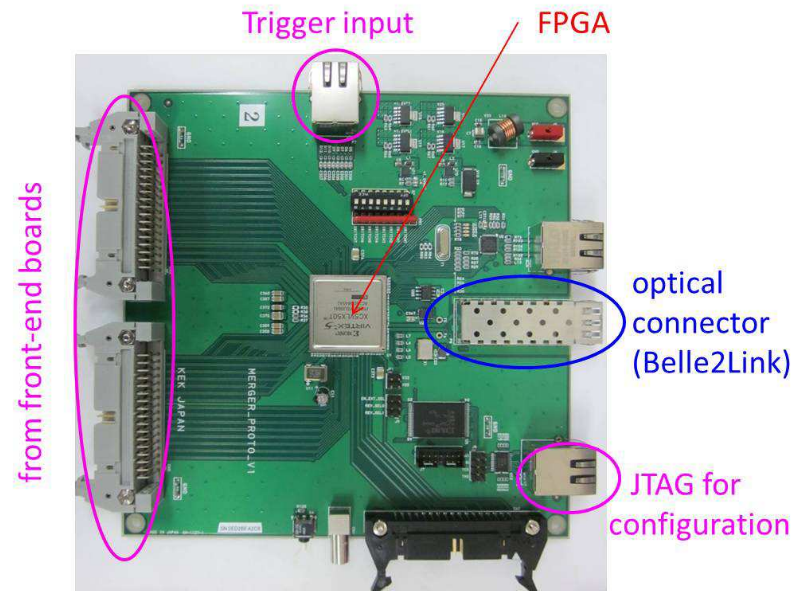


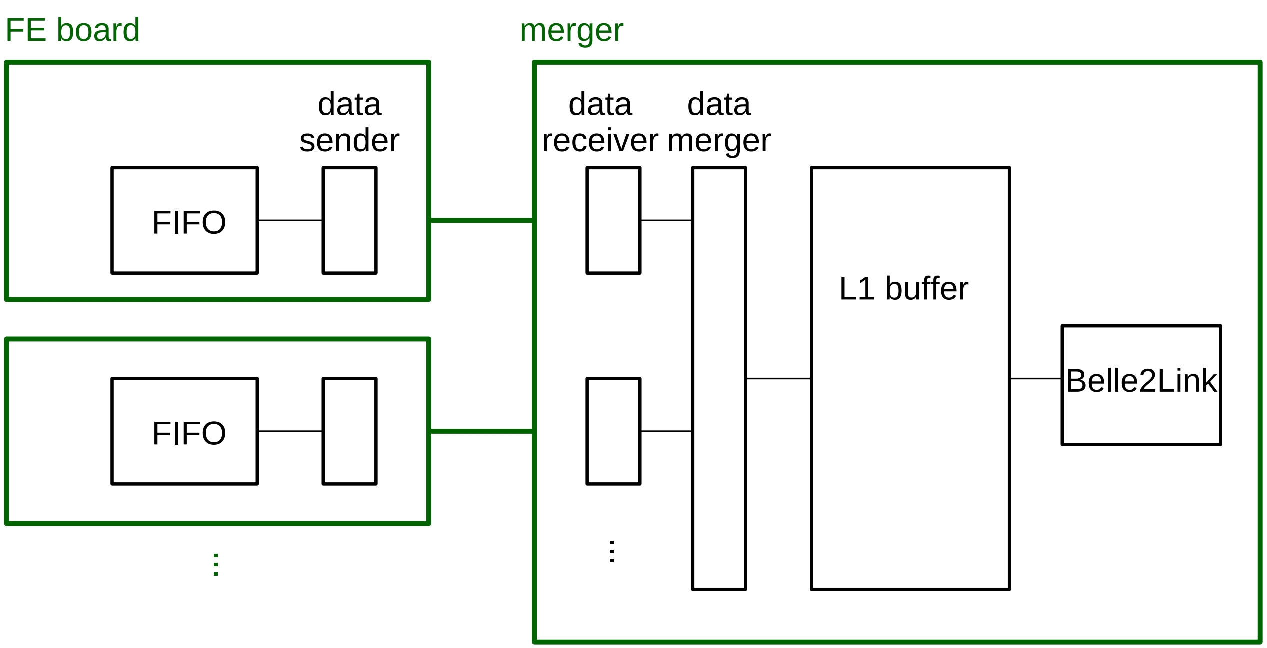
Only for the FPGA in merger (In the final design, FPGAs in the FE board is also configured by this line)

Merger

Status

- The board was produced last year, and simple test has been done.
- However, not so much progress on the firmware development.
- Still need some time for implementing. Start test with Belle2Link in Feb. ?





Zero suppression is necessary, but not included at first.

Summary and Plan

- ASIC (SA03).
  - ✓ SA03 is almost ready for the mass production. Need decision whether SA03 can be the final version (related to the specification, performance of HAPD. Neutron damage is an issue).
- Front-end Board.
  - ✓ Almost final, though still need minor update.
  - ✓ More productions (with SA03) for HAPD test.
- Merger
  - ✓ First prototype board is ready, but the development of the FPGA logic is in delay.
  - ✓ System test with Belle2Link.
  - ✓ Need to move to next prototype in JFY2012.
    - ➢ Smaller size.
    - ➢ Up to 6-FE board.
    - ➢ FPGA download (configure FE-boards through merger).

Backup

About Event Size

- #(ch) : 144 (ch/HAPD) × 456 (HAPD) = 65664
- Occupancy : 1.5% (assuming 1000 hits per event)
- Event size / ch: 18bit (to specify channel ID) + 4 bit (hit info.) = 22 bit
- Event size / event : 65564 × 4 = 262 Mb = 33 kB (w/o reduction)
  1000 x 22 = 22 Mb = 2.8 kB (w/ reduction)
- Link (B/s) : 33 kB × 30 kHz / 78 = 12.7 MB/s (w/o reduction)
  2.8 kB × 30 kHz / 78 = 1.1 MB/s (w/ reduction).

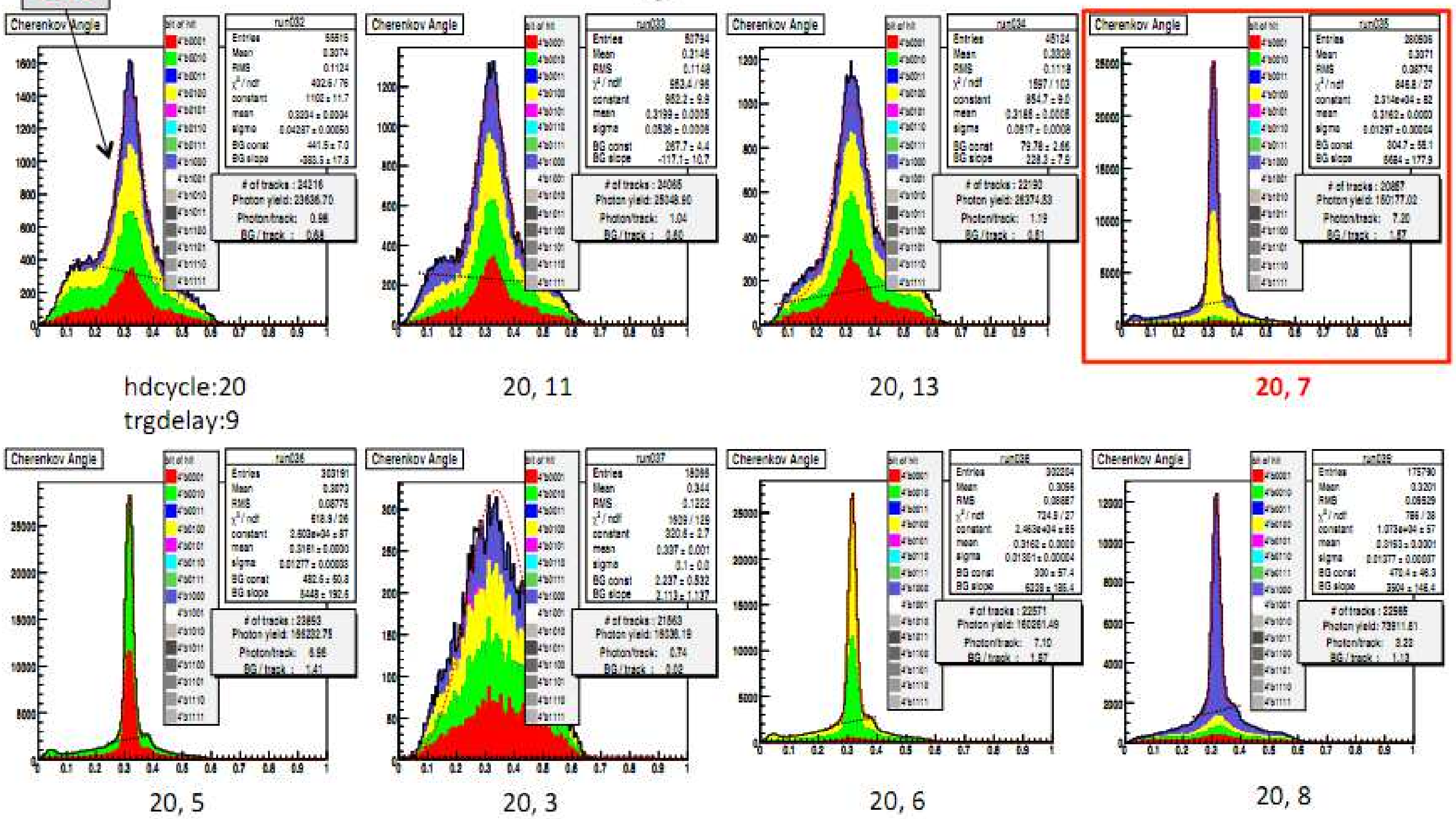
Cherenkov Angle distribution when we change the timing (delay of trigger).

Color indicates timing of signal (units of ~2us)

1000
0100
0010
0001

[S.Iwata]

Hit timing distribution



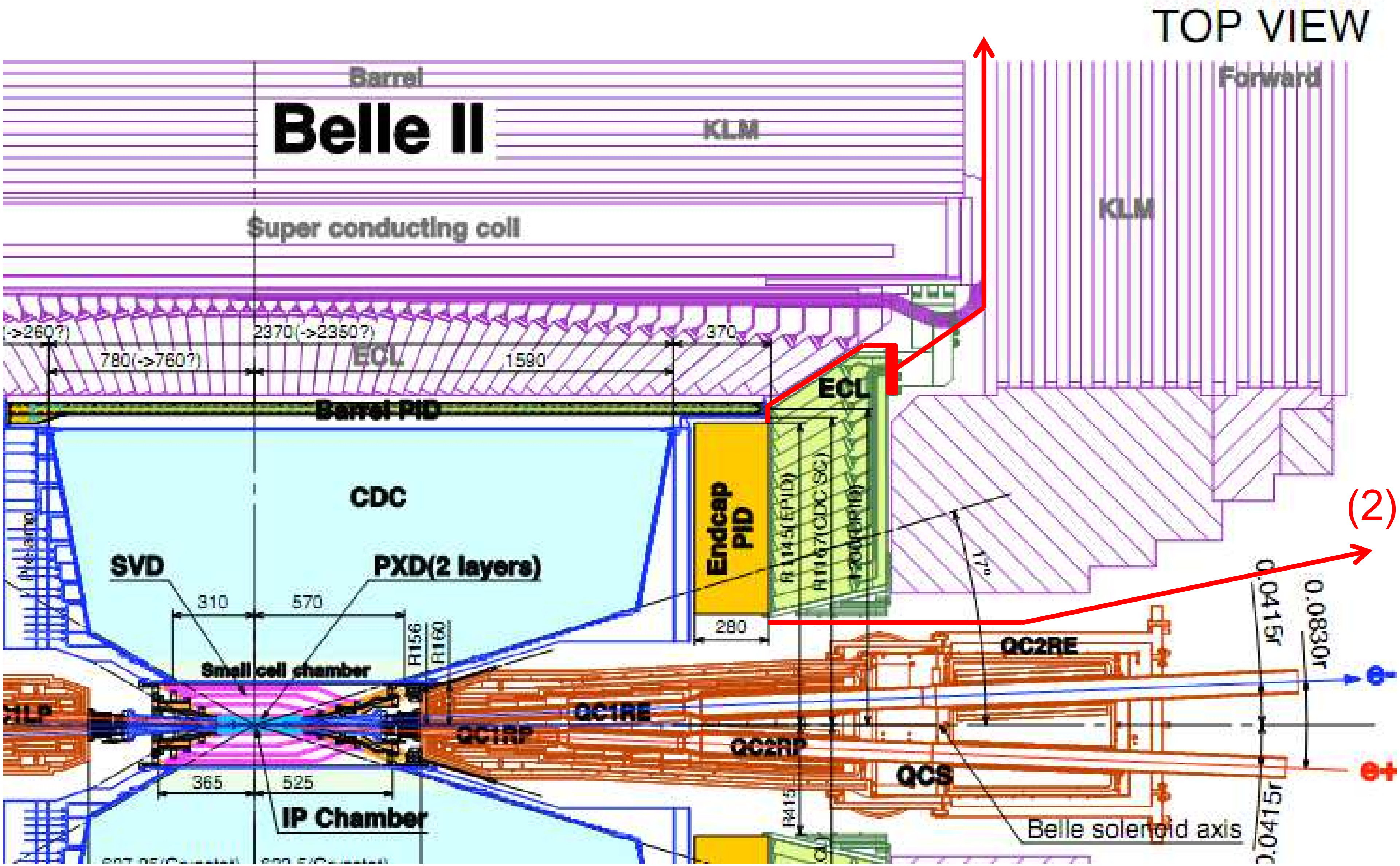
Cables for ARICH

Cables for ARICH

	ch		cross-section [mm^2]	comments.
HV	456	104mm^2 / ~12	4368	−8kV; 7 cables / sector
bias + guard	2280	6mm^2 / HAPD	2736	400V / 200V
LV	6 × 78	10mm^2 / merger	780	1.2,1.5,2.5,3.3 V / ±1.65 V
optical fiber	78	8mm^2	624	DAQ
UTP cable	156	~~3mm^2~~ 22 mm^2	~~468~~ 3432	trigger, JTAG
(sum)			~~(10976)~~ (11940)	

In addition, we need pipes for cooling water and air, fibers for calibration.

ARICH Cabling



- Original idea was to use the space between the endcap and barrel for the cabling (1).
  - ✓ In this case, cables need to be disconnected when the endcap is extracted. Joint box is necessary
  - ✓ However, we have O(1000) ch for bias, LV. Preparing removal connectors is not trivial.
- However, it is more convenient (or maybe inevitable) to extract the cables from the inner side (2).
  - ✓ If we make the cables longer to have some margin (several meters?), we may be able to move endcap or QCS without disconnecting the cables.
  - ✓ A small station near the detector is necessary, but no need to disconnect the cables whenever we open the endcap.
  - ✓ Maybe difficult to do the same thing for (1), because of no space behind the endcap.
  - ✓ Bias/HV/LV from inner side ?; Radiation Tolerance.