Barrel KLM RPC Front-End

Requirements, Design, and Status

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Belle II Trigger and Data Acquistion Workshop -- 2012
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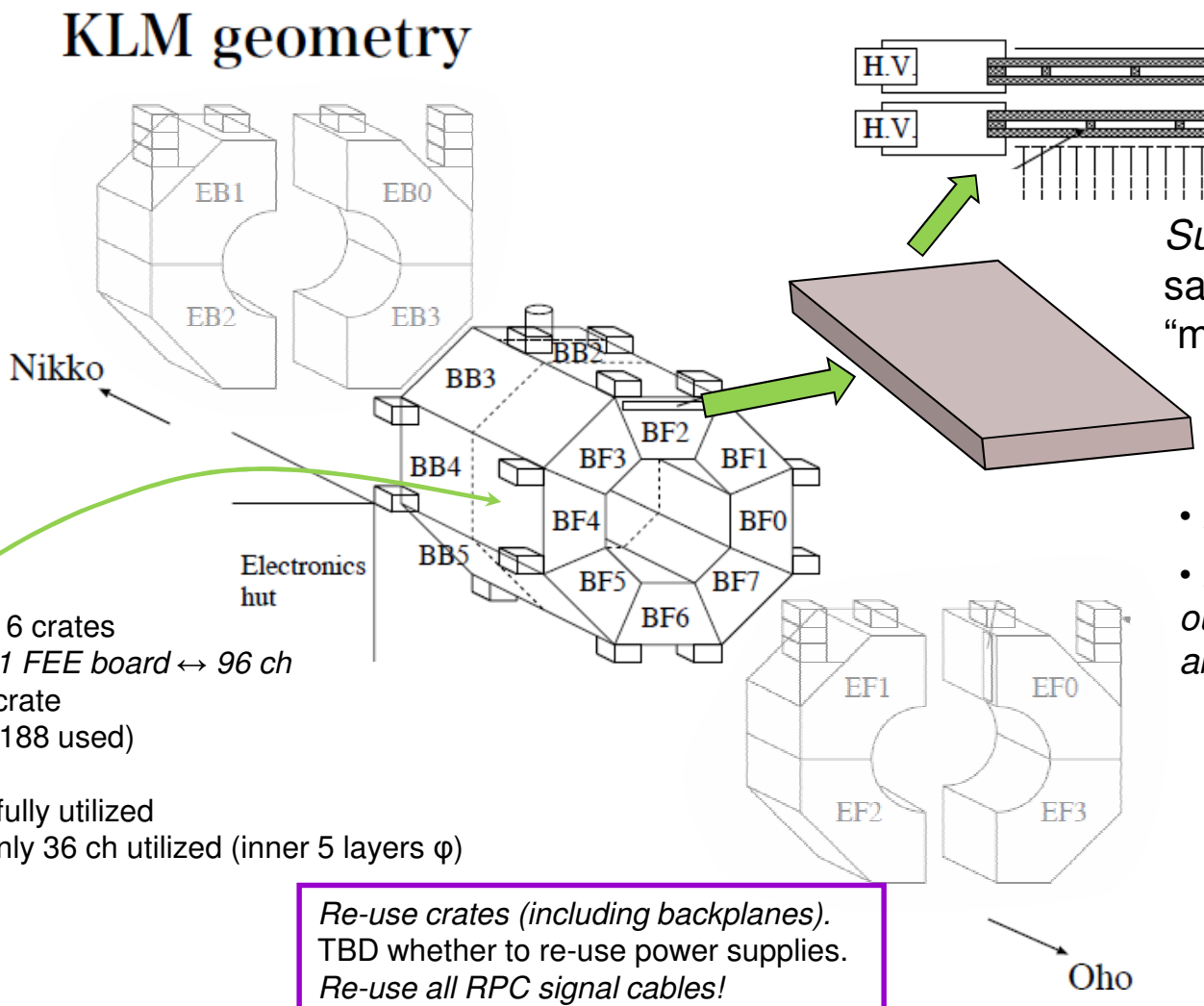
INDIANA UNIVERSITY

bKLM RPC Overview



Superlayer = 2× RPC sandwiched between "microstrip" planes

48 channels z
48 or 36 channels φ

- ***Belle:*** *15 superlayers*
- ***Belle II:*** *Keep only outer 13 superlayers, about 19k readout ch.*

16 "octants" ↔ 16 crates
1 superlayer ↔ *1 FEE board* ↔ *96 ch*
13 FEE boards/crate
1248 ch/crate (1188 used)
2 cables/board
21 cables/crate fully utilized
5 cables/crate only 36 ch utilized (inner 5 layers φ)

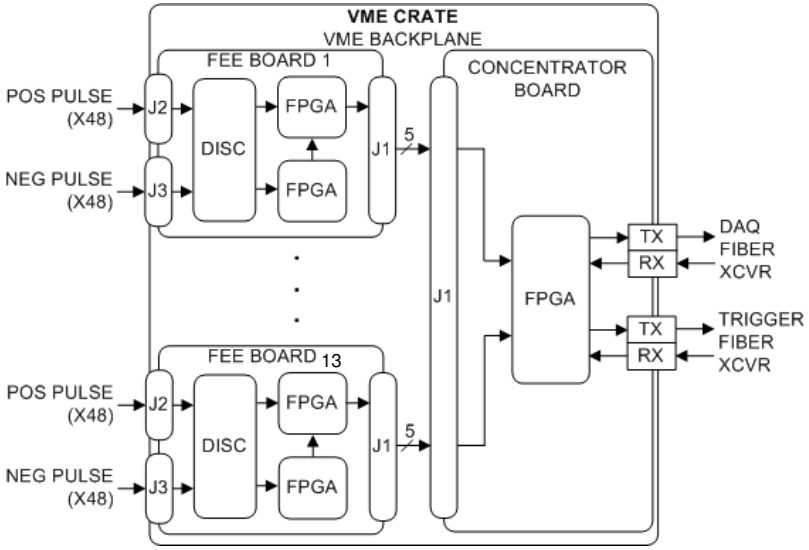
Re-use crates (including backplanes).
TBD whether to re-use power supplies.
Re-use all RPC signal cables!

(figure credit to Yusa-san)

Principal Requirements of the RPC FEE

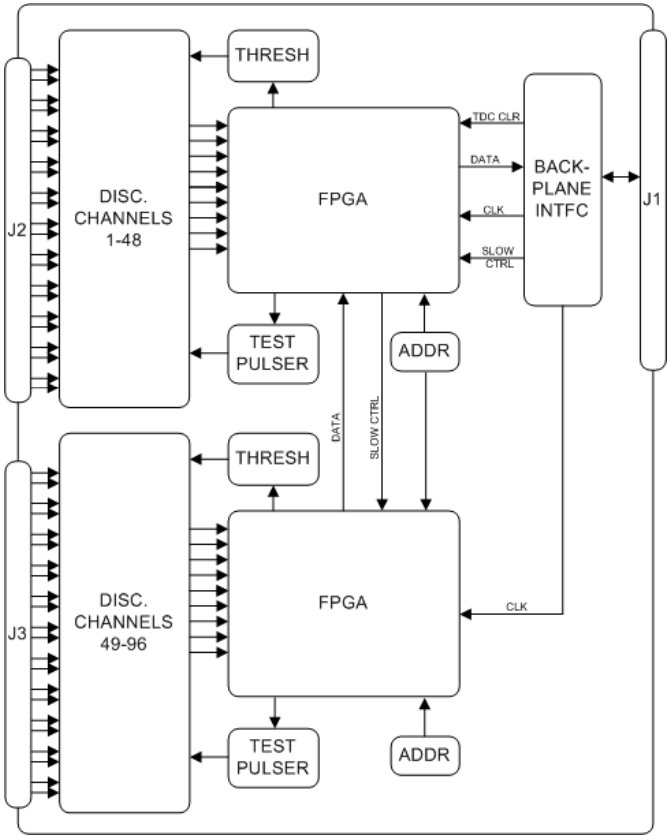
- Sensitivity <4 mV (10% of typical MIP signal)
- Time resolution <5 ns, walk <5 ns, double-pulse resolution <20ns. These values are modest improvements over the old system, which will improve rejection of afterpulses or other backgound.
- Analog test pulser
- Programmable discriminator threshold *(will be per channel, 8 bit*)
- Input protection circuit
- Termination to match RPC/signal cable characteristics, this is especially important as the detector is not a proper impedance match to the cable
- Interface with DAQ through B2Link standard, and with Belle II trigger processor. *A primary goal for us for this meeting is to understand the trigger requirements.*
- Latency from hits to trigger data output as low as reasonably achievable (is 1 μs ok?)
- *(Design goal):* Re-use of existing investment in RPC signal cables, readout crates (including backplanes and if feasible, power supplies)

System Level Design



- Crate contains 13 FEE boards and 1 concentrator board connected by a VME-J1 backplane.
- High performance differential line receiver and discriminators (96 channels).
- TDC's implemented in FPGA's (48 channel, 3.94 ns resolution from 2× 127 MHz ref clock).
- Fast and efficient 5 bit point-to-point interface from each FEE board to concentrator board. Total 13 x 62.5 MB/s.
- The concentrator prepares and transmits data to trigger system (augments time, matches hits/tracks), as well as buffering data to send to DAQ system upon triggers.
- The concentrator has fiber connections (1 each per crate) to the DAQ and Global Trigger systems.

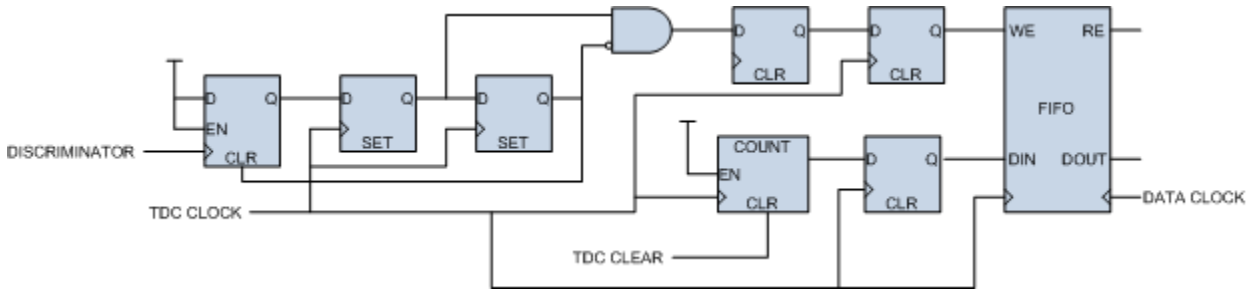
Front End Board



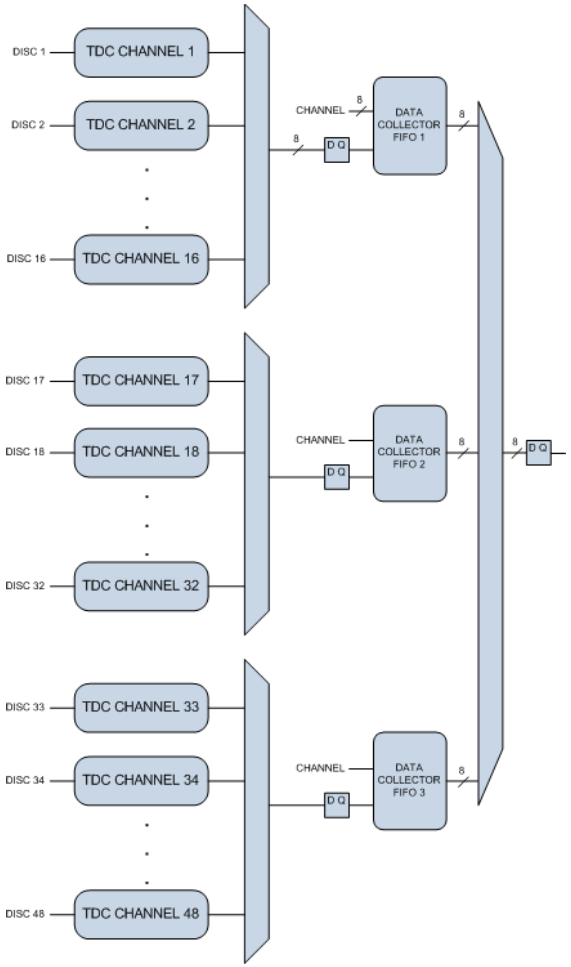
- Contains 96-discriminator channels, 48 positive polarity and 48 negative.
- Each FEE board serves 1 superlayer module
- Two FPGAs digitize fine time and multiplex data
- Discriminator threshold controlled by 8-bit DACs
- Test pulser for built in test; can be loaded with an arbitrary pattern of channels to fire synchronously
- A 48 channel discriminator & TDC FPGA prototype is now in fabrication; bare board received today

Prototype Front-End FPGA TDC Channel

- Each channel consists of:
  - Counter
  - 16-deep FIFO
  - Rising edge detector
  - Pipelining
  - Metastability protection
- Counter clear is used for synchronization
- Four 250MHz clock cycles to store a hit



Prototype Front-End FPGA

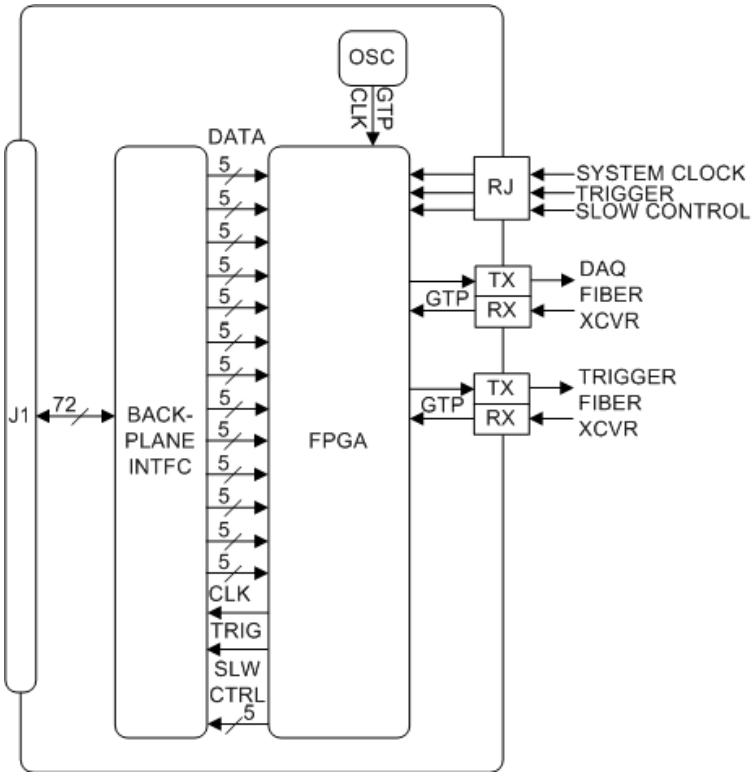


- Prototype design simulated and meets timing
- 48 TDC channels operate at 250 MHz (4ns)
- Simple, scalable data collection at 125 MHz (8ns)
  - One sample from one channel read each clock cycle at first mux stage
  - One value (channel and time) from one channel read in two clock cycles at second mux stage
  - First stage mux inputs may be decreased to minimize latency
  - Multiple samples may be read from each channel for further optimization
- Fits in small Spartan-6 (XC6SLX25-2CSG324)

Prototype Front-End FPGA Performance

- 4 ns time resolution
- 10 +/- 2 ns double pulse resolution
- 528 ns maximum single channel latency due to processing and pipelining
- Simultaneous hit on each channel processed with 948 ns latency
- Simultaneous hit on 4 channels processed with 347 ns latency
- Data output is 8-bit channel value followed by 8-bit time value

Concentrator Board

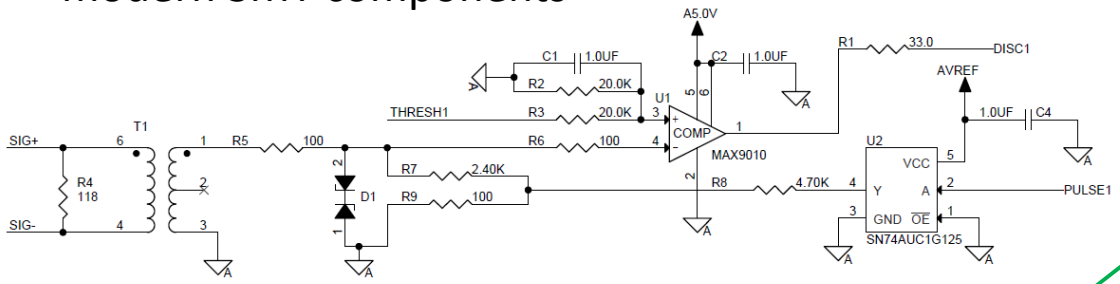


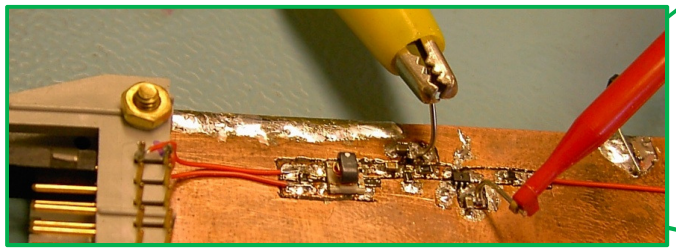
- Processes/packages data from 13 front-end boards.
- Contains RJ45 connector for timing system interface.
- Uses Virtex-5 gigabit transceivers and SFP optical modules to communicate with DAQ and Global Trigger system.

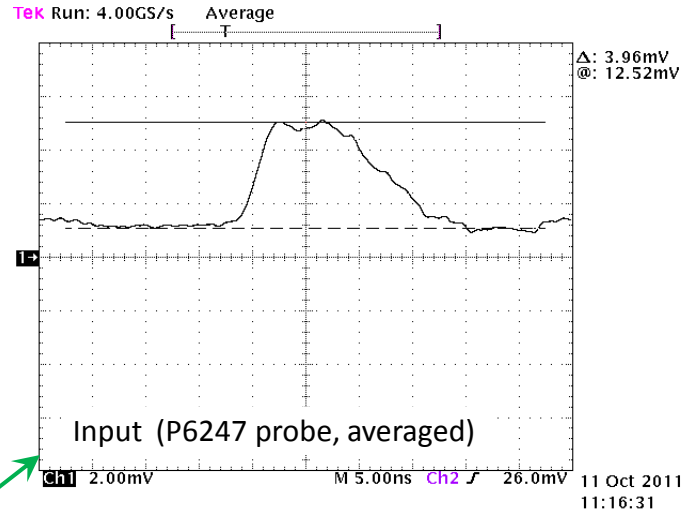
New Line Receiver and Discriminator

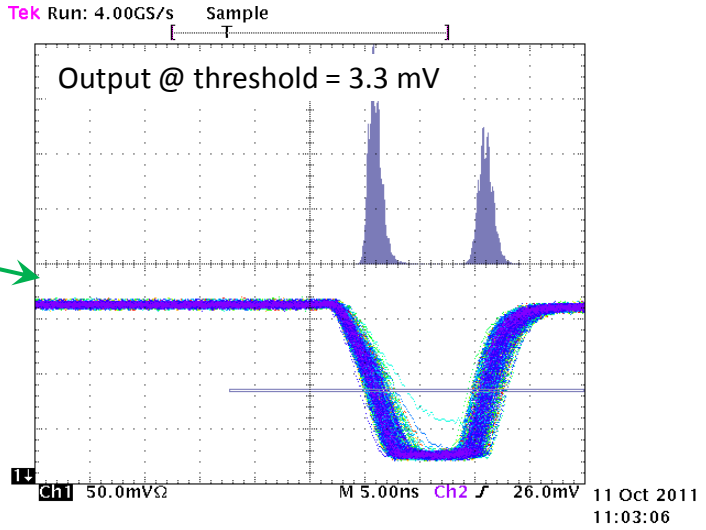
similar in spirit to original design of Belle, but now:

- lower power, single supply
- balanced line receiver
- robust input protection
- modern SMT components
- *analog* test pulser
- V_{TH} DAC per channel



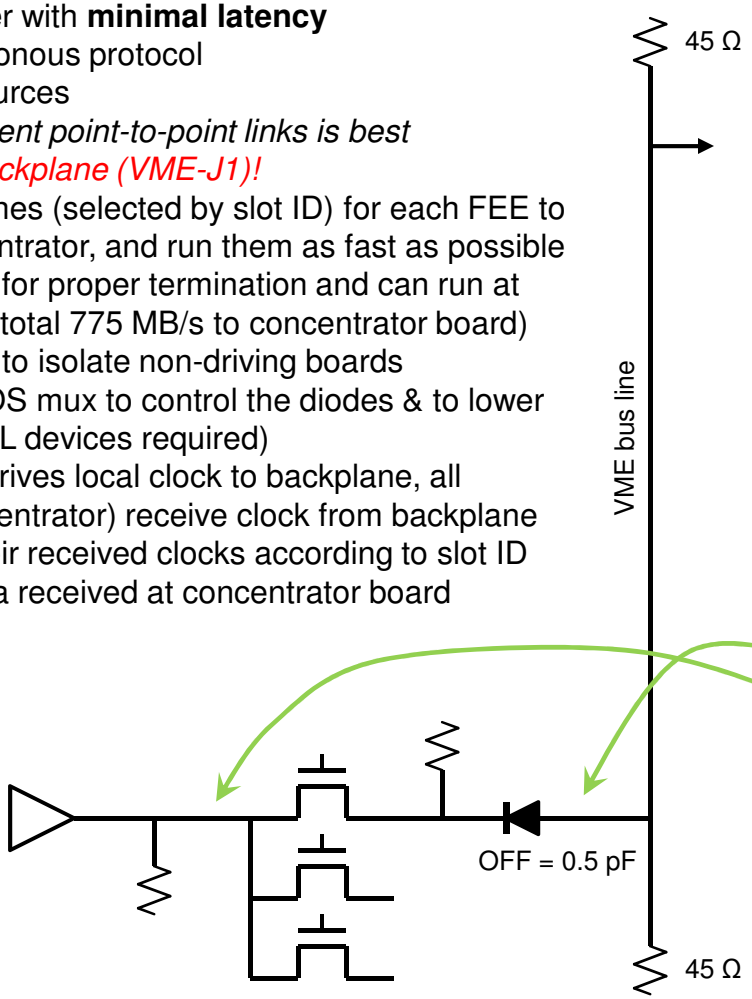


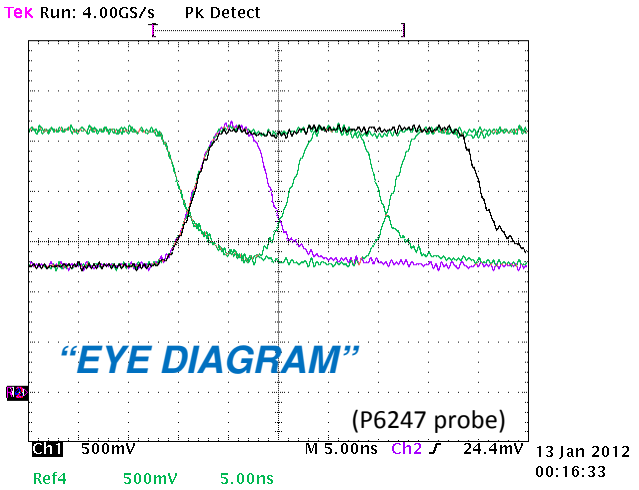


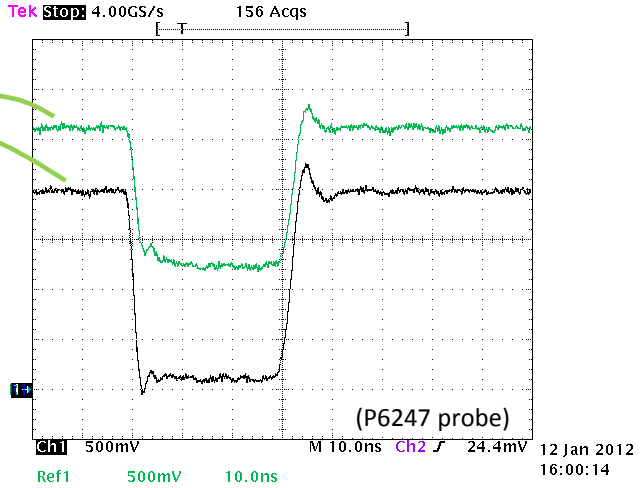


FEE to Concentrator Data Transfer

- All FEE boards feed data to one concentrator board
- We require to do this transfer with **minimal latency**
  - Use a simple, synchronous protocol
  - Don't share any resources
  - → *Thirteen independent point-to-point links is best*
- *But we should re-use old backplane (VME-J1)!*
  - → *Dedicate* 5 VME lines (selected by slot ID) for each FEE to communicate to concentrator, and run them as fast as possible
    - → GTL allows for proper termination and can run at over 100 MHz (total 775 MB/s to concentrator board)
    - → Use diodes to isolate non-driving boards
    - Also: use NMOS mux to control the diodes & to lower costs (fewer GTL devices required)
  - Concentrator board drives local clock to backplane, all boards (including concentrator) receive clock from backplane
  - FEE boards skew their received clocks according to slot ID in order to deskew data received at concentrator board







Status

- Breadboard prototypes have been used to evaluate and optimize the discriminator performance, input protection circuit, and backplane physical layer interface
- A prototype 48-channel front-end board now in fabrication
- The prototype front-end FPGA is nearing completion
  - Non-sorted data multiplexing complete
  - Adding some external interfaces specific to proto-type
- The prototype will be evaluated with actual bKLM RPC at Belle II in a few months
- Concentrator board design underway
- We are in need of input on trigger algorithm for concentrator board, whether that requires time-sorted input hits, and what are the latency limits for trigger data

BACKUP SLIDES

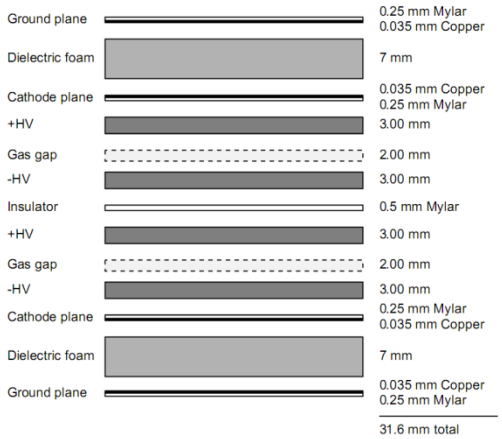
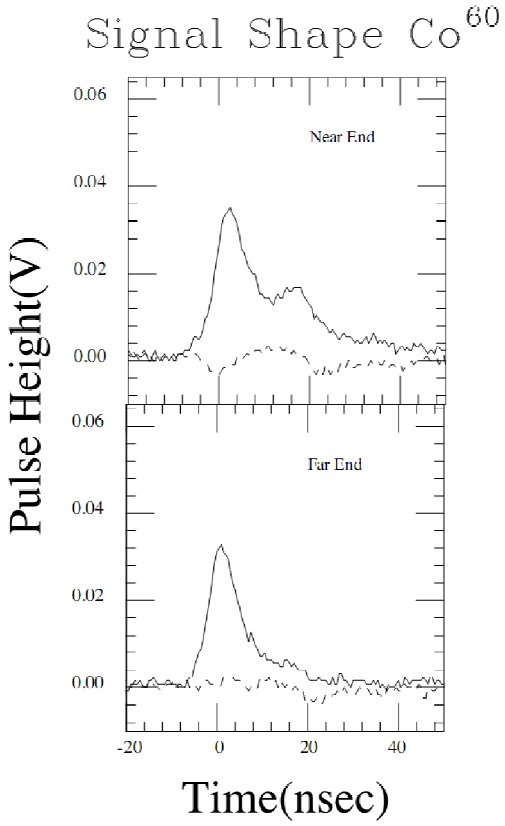
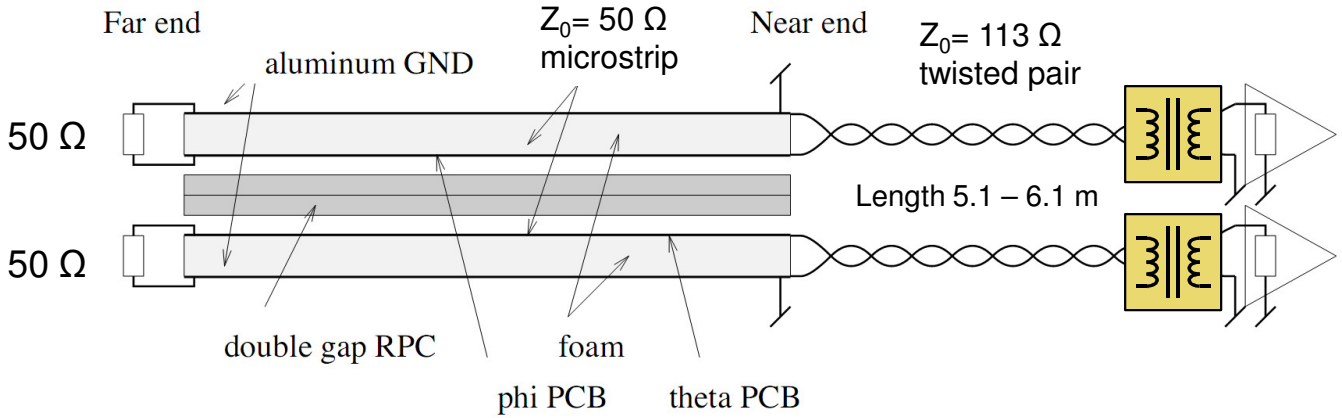
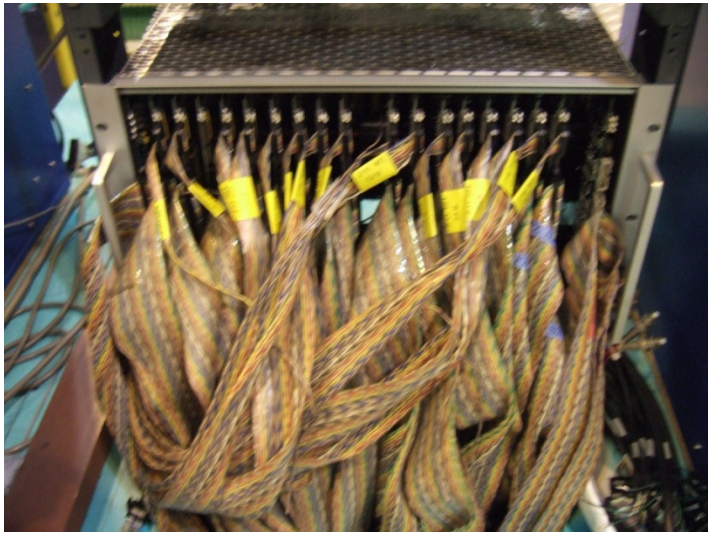
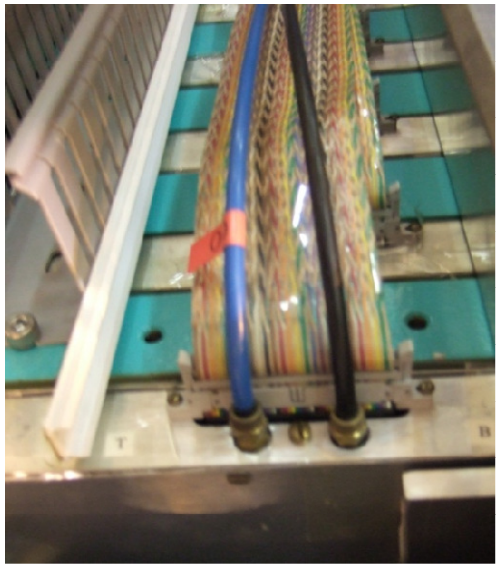


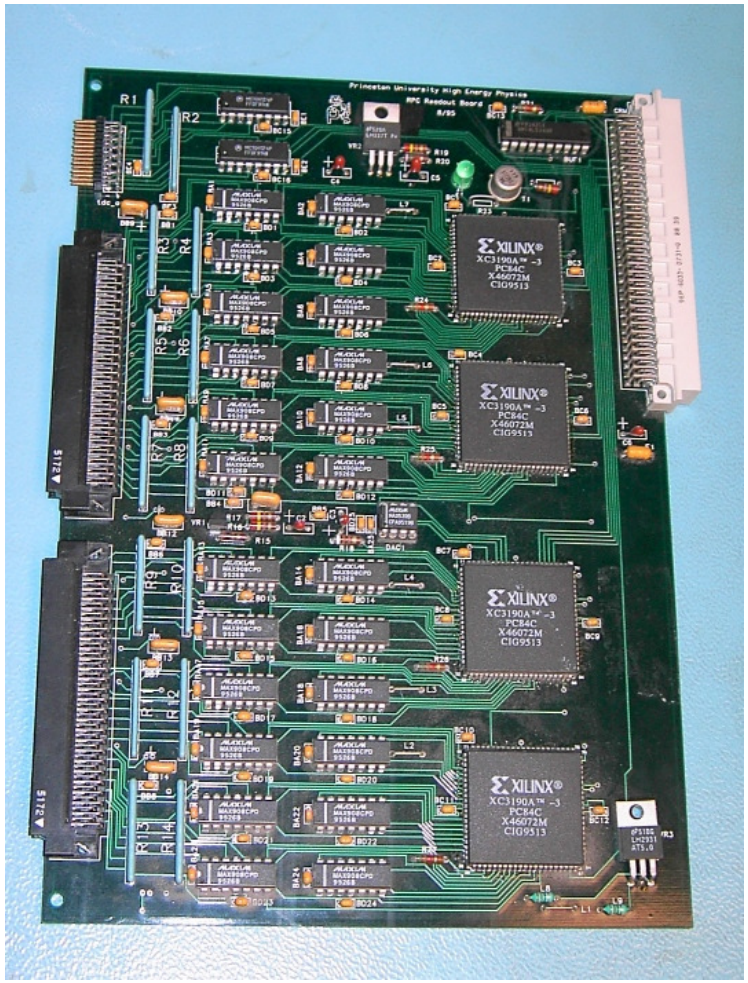
Figure 10.2: Exploded cross-section of an RPC superlayer.



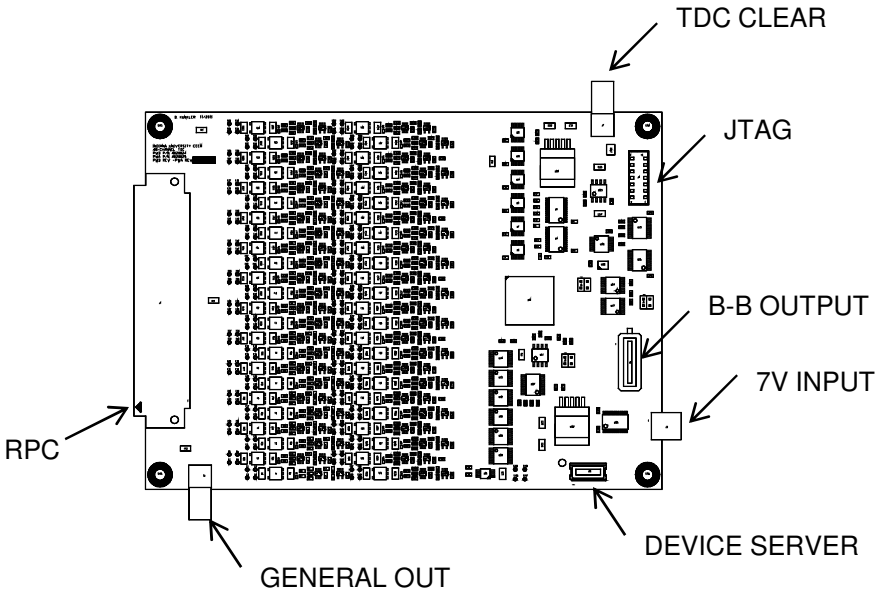


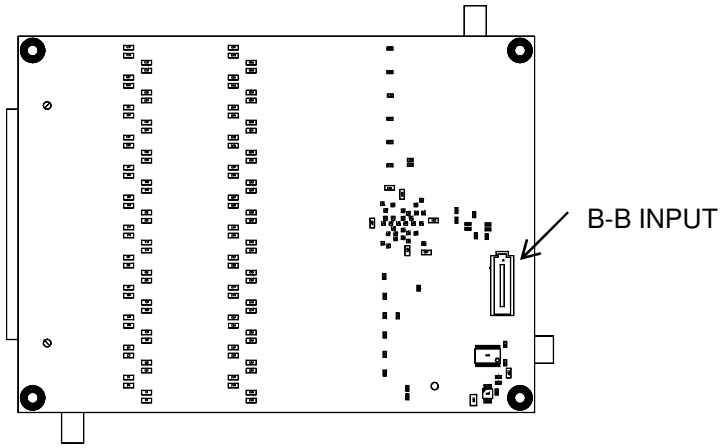





Princeton University High Energy Physics
RPC Readout Board
XILINX
XC3190A -3
PC84C
X46072M
CIG9513

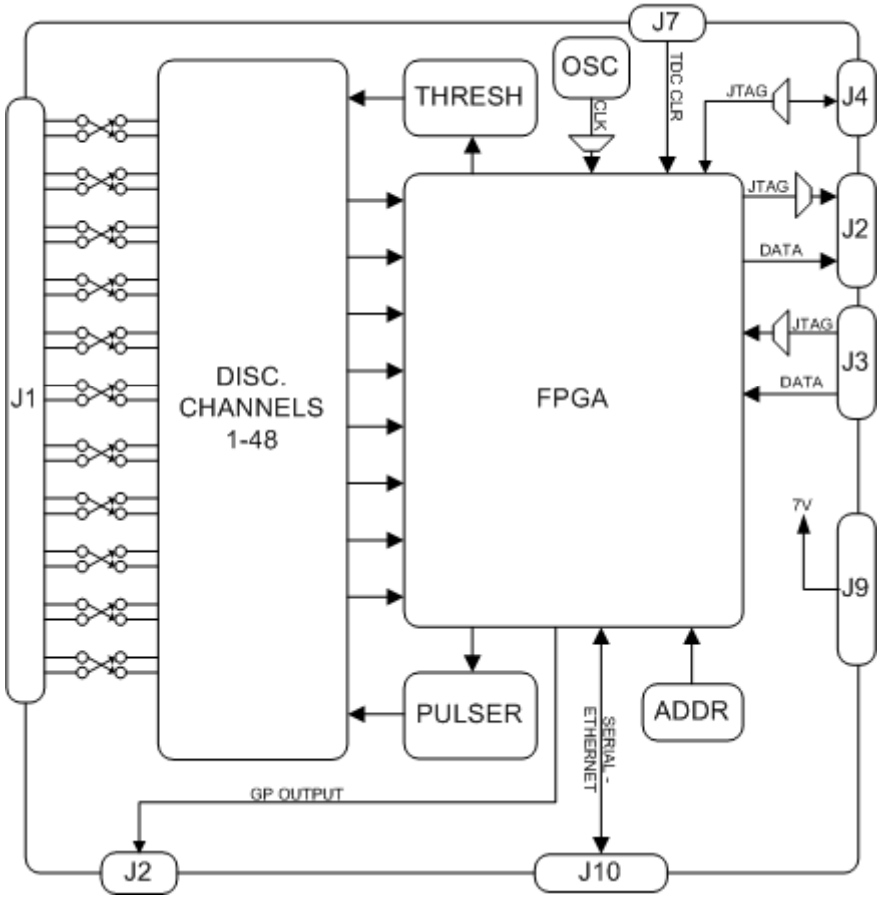
Prototype Assembly





- TDC Clear and General Out are Lemo connectors.
- The board-to-board-connectors (B-B) allow the boards to be stacked.
- The device server connector allows an Ethernet module to be installed.

Prototype Functional Diagram

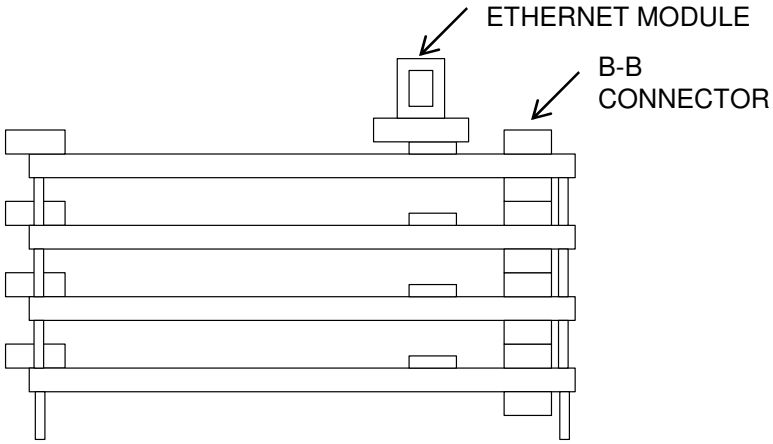


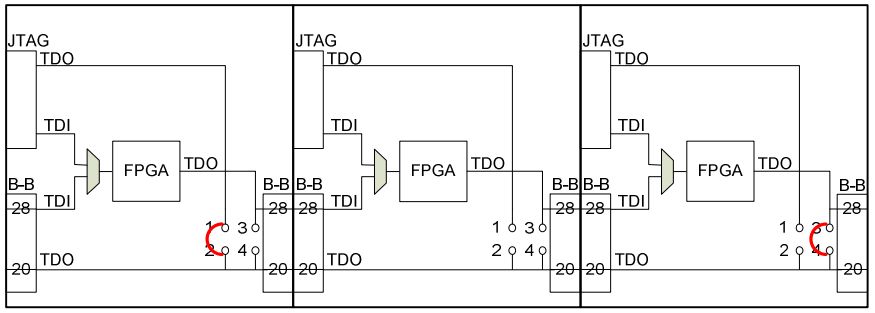
- RPC output polarity can be swapped.
- One B-B connector is input (J3), the other is output (J2) allowing data to be moved between boards.
- The B-B connectors are high-speed so the signal integrity will be similar to final 96-channel board.
- JTAG, clock, and data are multiplexed so there is one master in the stack.
- At least one board in stack may contain a Etherne module (serial-Ethernet device server).
- The threshold (THRESH) is controlled by six 8-channel DACs.

Nano LANReach 3-24Mbps Ethernet module with server.

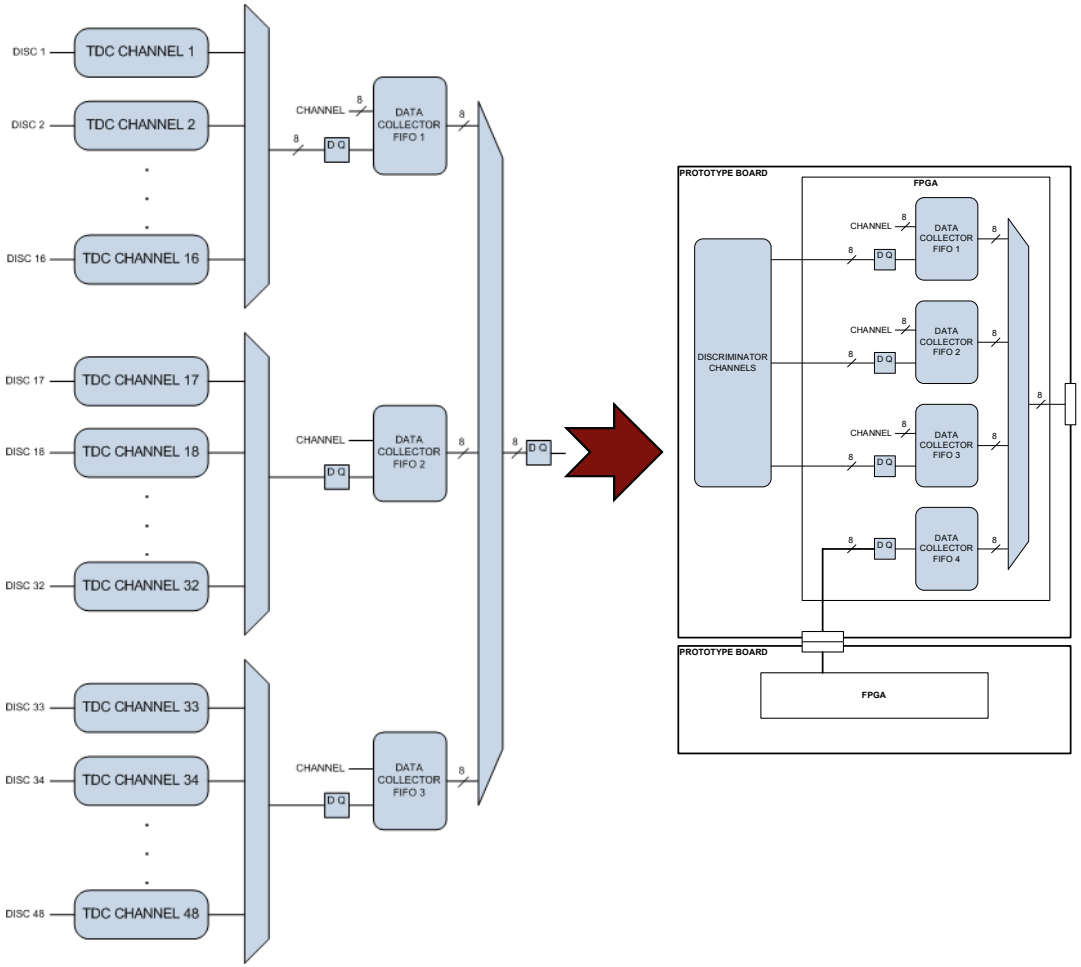
Prototype Stack-Up

- The top B-B connector is output and the bottom is the input.
  - Allows communications between boards
- The idea is we can stream data from the last board in the chain (bottom) to the first (top).
- Top board can contain an Ethernet module for streaming data to a PC.
  - Only requires crossover cable.
  - TeraTerm or Wireshark can be used to collect data.
- Top and bottom boards are special.
  - Jumpers allow use of ChipScope to collect data.



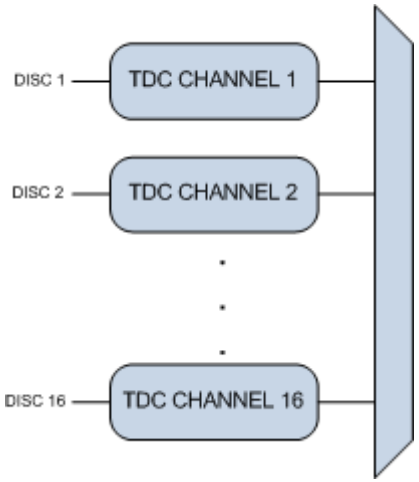


Prototype Top Level TDC



- Adding a fourth FIFO easily allows data to be streamed to next board.
- The TDC Channel contains a 16 deep FIFO with 8-bit input and 8-bit output.
- The Collector FIFOs are 256 deep with a 16-bit input and 8-bit output.

Prototype Front-End FPGA Data Collection



- Each mux is connected to 16 of 48 channel
- The mux is addressed with a shift register such that one channel value processed each 125MHz clock cycle
- Reduce latency with parallel processing
- Very simple and scalable – channels per mux and samples per write can be adjusted
- Reasonably low latency

Prototype Performance

- Existing design – no board stack
  - 4 ns time resolution
  - 18 +/- 2 ns double pulse resolution
  - 528 ns maximum single channel latency due processing and pipelining
  - Simultaneous hit on each channel processed with 948 ns latency
  - Simultaneous hit on 4 channels processed with 347 ns latency
  - Data output is 8-bit channel value followed by 8-bit time value
- Board stack
  - Single channel latency increases to (528+4)*4 = 2128 ns if Ethernet module is used.
  - Simultaneous hit latency will increase accordingly.
  - Data output is 4-bit board address then 8-bit channel values followed by 8-bit time values.