

Status of the ECL DAQ subsystems

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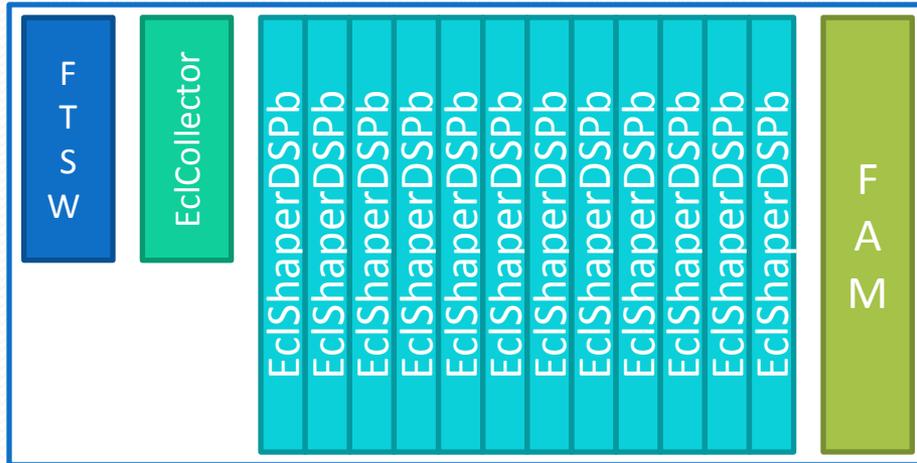
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Output

- Overview and status of ECL electronics
- Report on Belle2link integration test (Dec 2011)
- Belle2link FPGA design remarks

ECL electronics Infrastructure

VME crate



Modules:

- EclShaperDSPb – shaping pulses from CsI preAmps, digitizing and digital processing.
- EclCollector – merges data from EclShaperDSPb modules and sends the data to the DAQ system
- FTSW – provides timing & trigger information for EclCollector
- FAM – provides arguments for global trigger from ECL.

There are 52 ECL VME crates
We don't plan to install VME controller at the crates

The crates have non-standard power supplies!

± 7.5 V (instead of ± 5.0 V)

± 15 V (instead of ± 12 V)

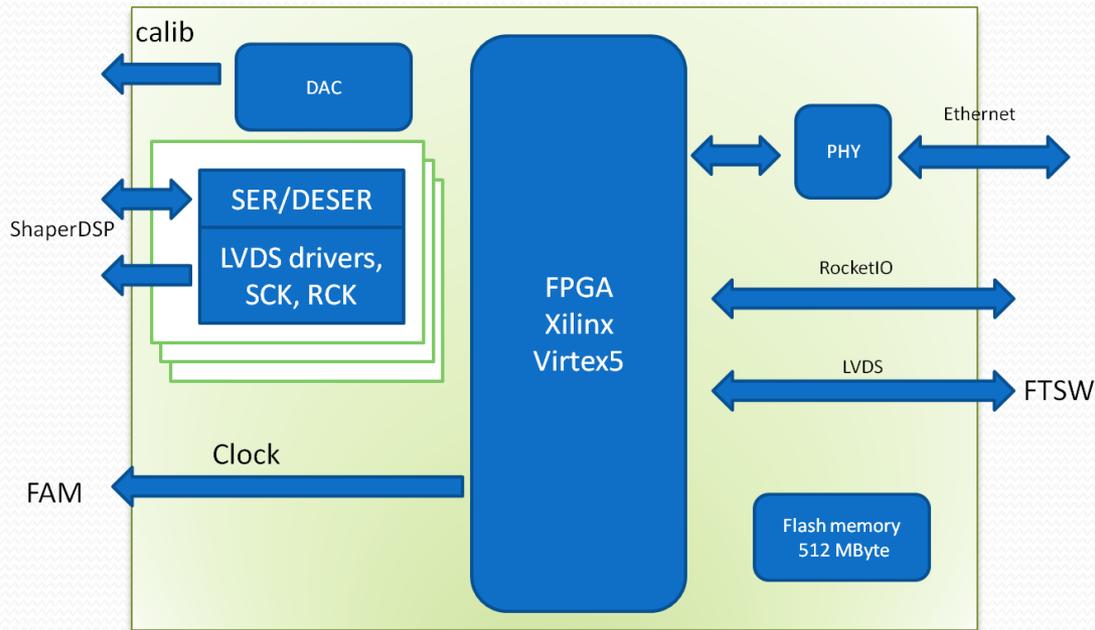


ShaperDSPb



EclCollector

Tasks of the ECL collector module.

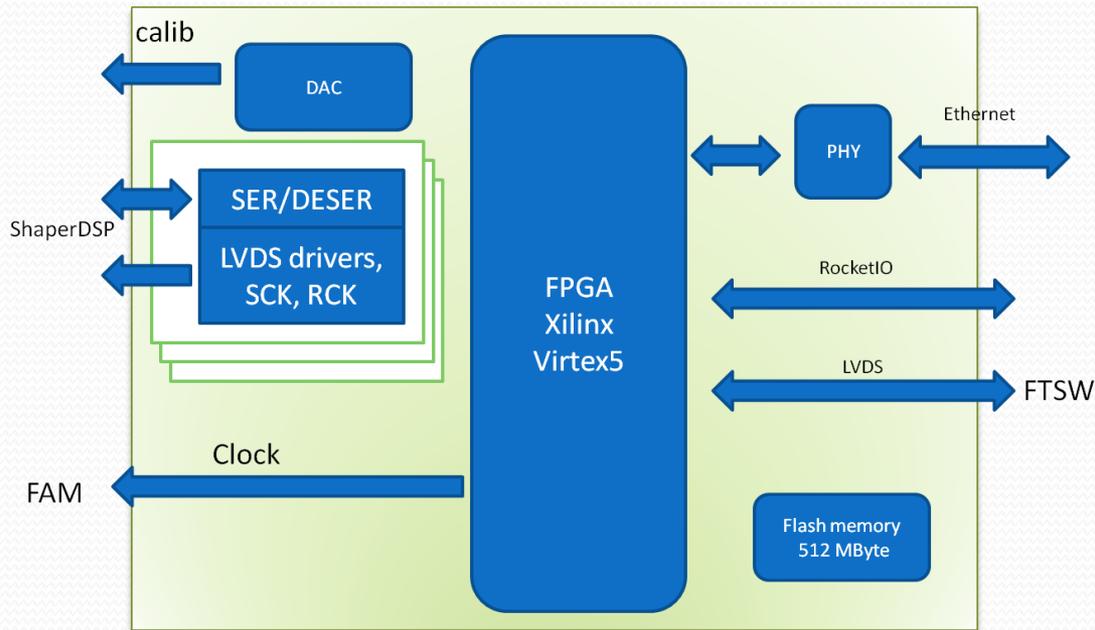


1. **Collect and merge data from 12 connected ShaperDSPb modules**
2. **Provide interface with Belle II TTD and DAQ**
3. **Configure Xilinx FPGA on ShaperDSPb modules**
4. **Synchronization of sampling process in ShaperDSPb modules**
5. **Generation of a calibration signal**
6. **Ethernet interface for stand-alone operation and upload of DSP coefficients**
7. **Store coefficients for DSP processing**

EclCollector modification

- Virtex5 XC5VLX110 (1900\$) => Spartan6 XC6SLX150T (200\$)
- 100M to 1000M Ethernet (for faster initialization and coefficients upload)
- JTAG-over-LVDS
- 127 MHz on-board oscillator
- On board DDR3 memory for embedded CPU
- Use of more capable Flash chips => only 4 chips for 512 Mbyte flash memory
- Photodiodes HV Current and Voltage monitoring
- 8 kbit of EEPROM
- Temperature control
- Fix of small bugs

Report on belle2link integration test (Dec 2011)



Currently we have only first prototype of EclCollector based on Virtex5 FPGA. Its FPGA design allows to work with EclShaperDSP modules (init ADC sampling, readout data and many other tasks) through Ethernet connection.

The task for the integration test was to implement interface with FTSW for trigger information and with HSLB for event data output.

Integration with FTSW

- The VHDL design files for decoding trigger signal from FTSW were successfully embedded in EclCollector FPGA design – the signal is decoded and ADC sampling sequence is initiated
- The simulation testbench is prepared – now I can model event generation from FTSW module and look how event processing is carried out inside FPGA of EclCollector in simulation.

Integration with HSLB

- The VHDL, verilog design files and NGC implementation files for belle2link were embedded in EclCollector as they are in CDC FPGA design. **Several issues raised** in hardware tests
 - There is no automatic byte=>16-bit words alignment. One should reconfigure FPGA until correct alignment is approved by ChipScope tool.
 - The data transfer from HSLB to EclCollector is OK, the idle data transfer in opposite direction is OK also, but actual data transferred to HSLB are not recognizable on HSLB side.
- Simulation is impossible because NGC files are not supported by simulator.

Belle2link FPGA design remarks

- Add default value for VHDL signals:
 - `signal sig : std_logic := '0';`
 - `signal sig_vec: std_logic_vector (4 downto 0) := (others=>'0');`
- Distribute source files – no NGC files



Thank you for your attention!

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