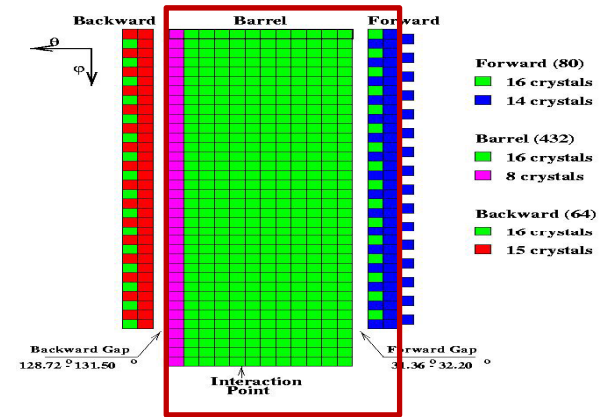# ECL TRG

B.G. Cheon

(Hanyang Univ)

@ Belle II TDAQ Workshop, UH, Jan/16-18/2012

Belle2 ECL Trigger

- Basic element(576): Trigger Cell (4x4 crystal sum)

- Main hadronic event triggers

  - Energy trigger : $E_{TOT} > 1GeV$ & Bhabha-veto

  - Cluster trigger : ICN > 3

- In case of high trigger rate upon the early stage

  - Turn on cosmic veto trigger

  - Increase TC threshold (100MeV →)

  - Increase E_{TOT} threshold (1GeV →)

 - Increase ICN clusters (3 →)

  - Reduce physics trigger region

Backward   Barrel   Forward

θ
φ

Forward (80)
16 crystals
14 crystals

Barrel (432)
16 crystals
8 crystals

Backward (64)
16 crystals
15 crystals

Backward Gap
128.72 º 131.50 º

Forward Gap
31.36 º 32.20 º

Interaction
Point

Physics trigger region

ECL Trigger outputs to GDL

Item	Number of bits
Trigger timing (Final, Fwd, Barrel, Bwd)	4
Total Energy (>0.5, 1.0, 3.0 GeV)	3
Isolated cluster	4
Bhabha-type	11
OR-ed Bhabha	1
Barrel Bhabha	1
Prescale Bhabha	1
Cosmic veto	1
TC hit pattern	576
Total	26+576

Hardware configuration
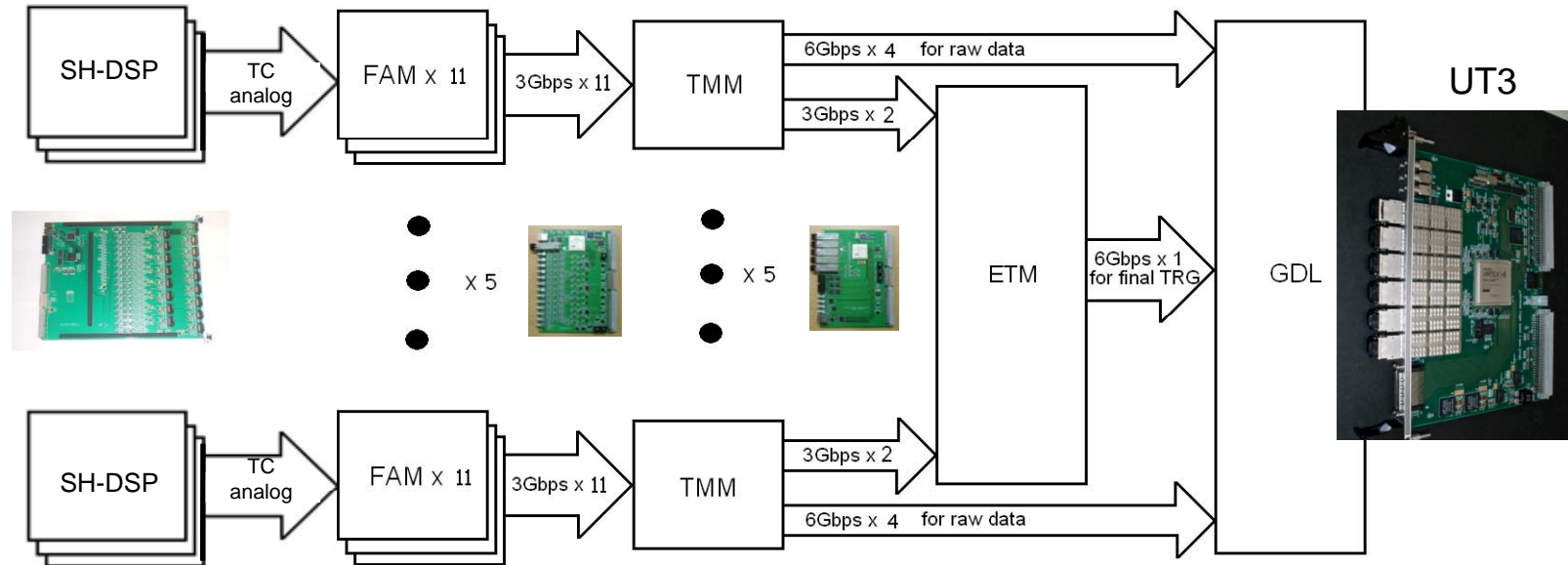
Peaking time of TC	700
ADC pipeline	100
Peak finding process	300~400
Programmable delay	300
Gbit transfer(200bits)	100
Optical cable length	200~300

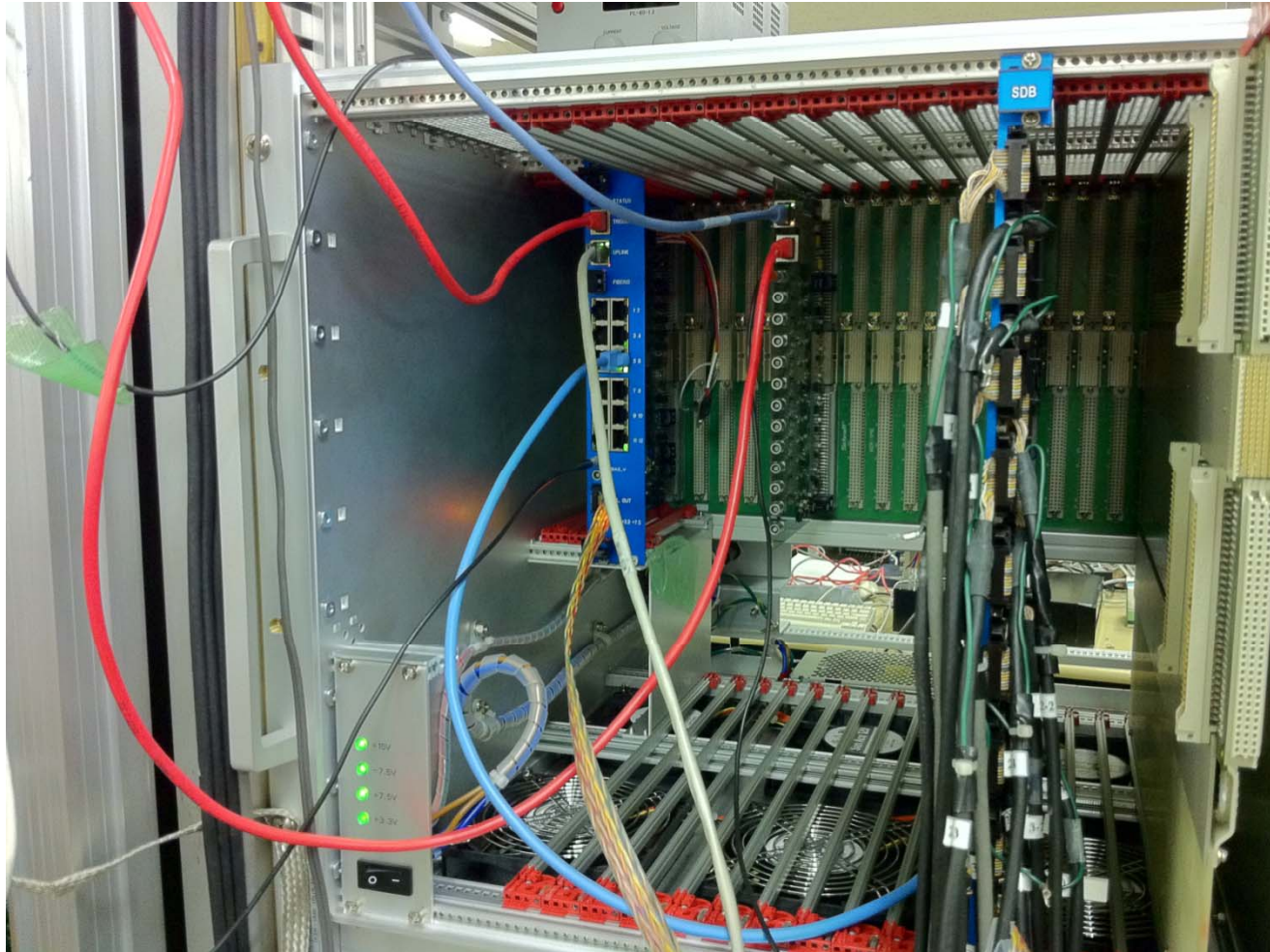| Bridge delay	200~300
Gbit transfer(~ 1100bits)	400

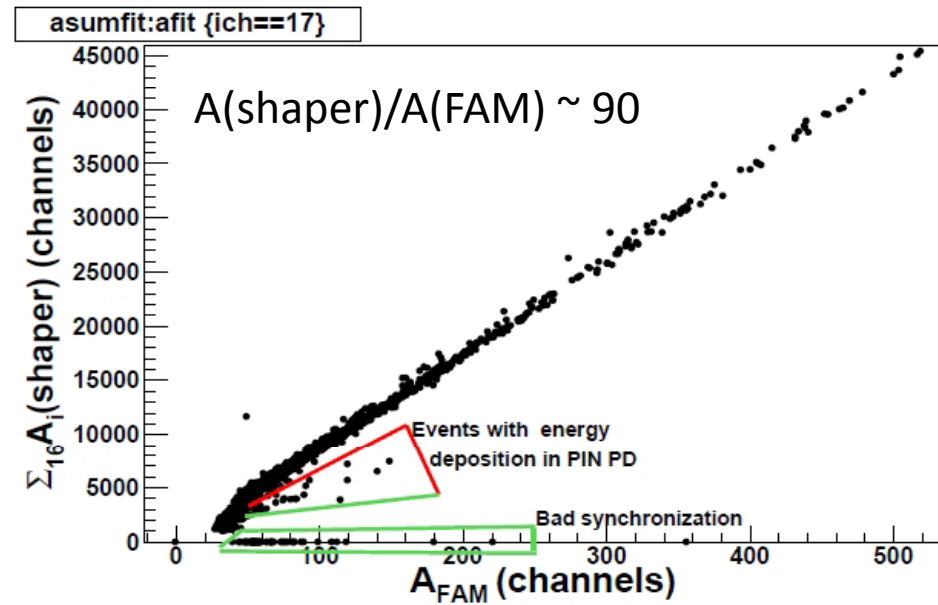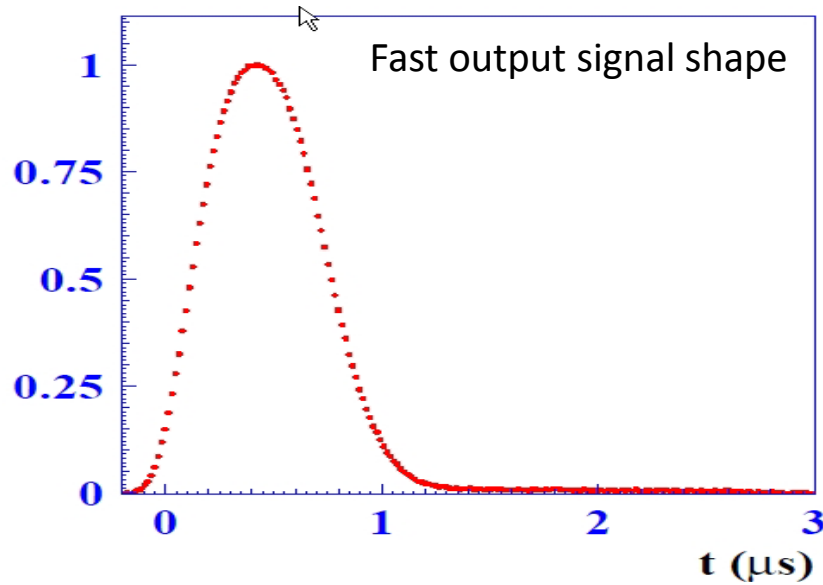| Input alignment	100
Trigger decision	200~300

* Total latency = 2600 ~ 3000 ns

** TMM FPGA = XC6VLX130T-1FF1156C

- **Flexible trigger configuration by FADC + FPGA architecture.**
- **rather easy to accommodate endcap detector upgrade.**
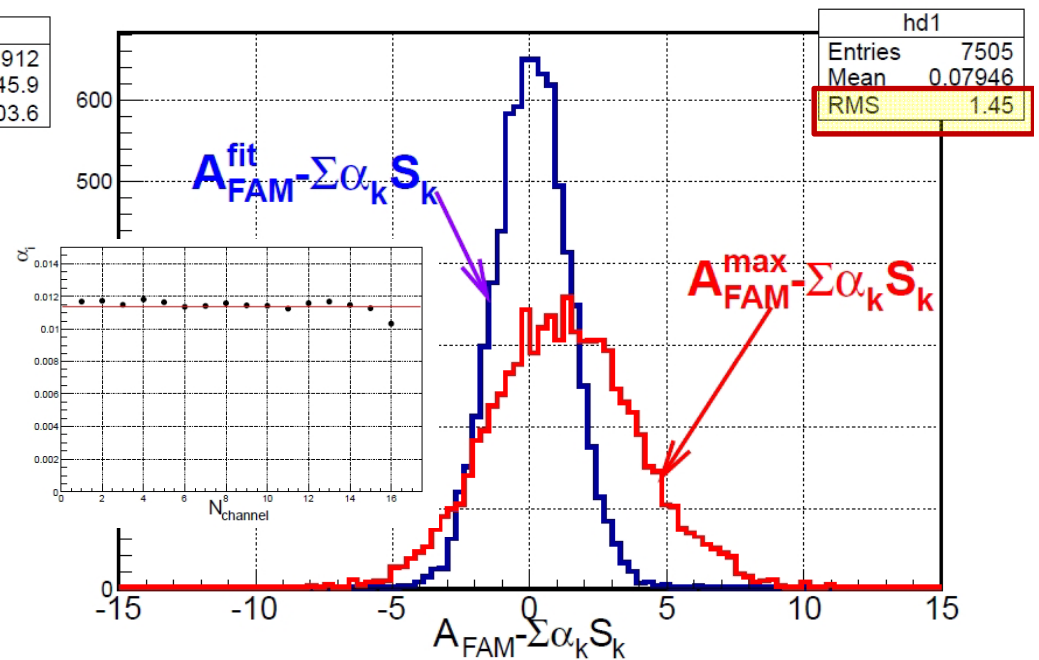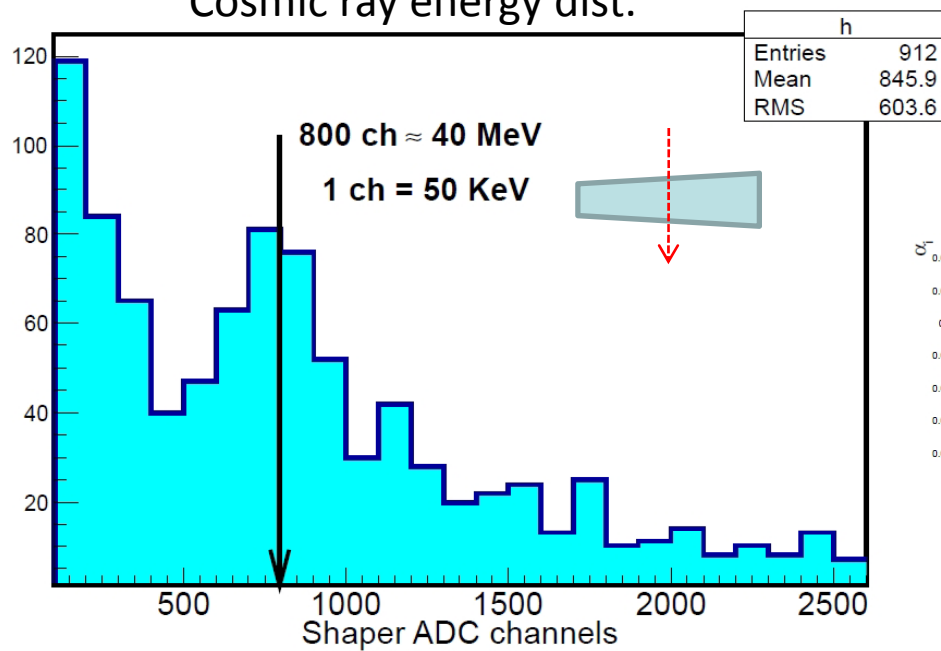 - ◆ **pulse-height and timing correction @ FAM**

Collector/FAM/Shaper-DSP
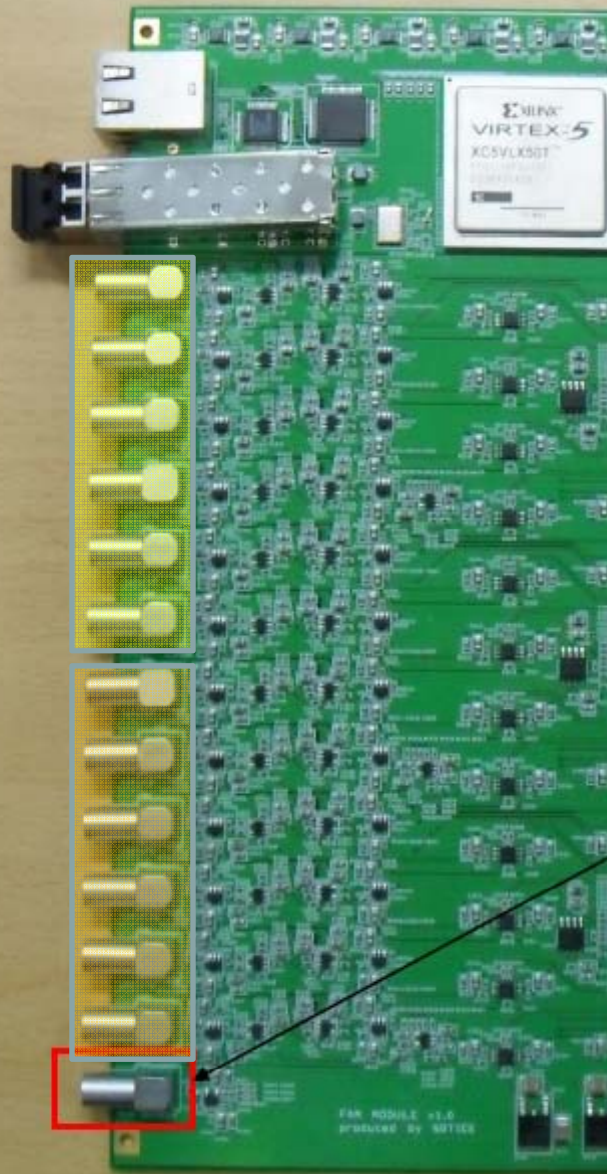

- VME crate system test with realistic readout electronics chain.
- Barrel crystal test setup to check out all the crystal condition.

D. Epifanov (BINP)

Fast output signal shape

asumfit:afit {ich==17}

A(shaper)/A(FAM) ~ 90

Events with energy deposition in PIN PD

Bad synchronization

$\Sigma_{16} A_i$(shaper) (channels)

A_{FAM} (channels)

Cosmic ray energy dist.

h	
Entries	912
Mean	845.9
RMS	603.6

800 ch ≈ 40 MeV

1 ch = 50 KeV

Shaper ADC channels

hd1	
Entries	7505
Mean	0.07946
RMS	1.45

$A_{FAM}^{fit} - \Sigma \alpha_k S_k$

$A_{FAM}^{max} - \Sigma \alpha_k S_k$

$A_{FAM} - \Sigma \alpha_k S_k$

$N_{channel}$

Analog out of FAM

Two outputs needed, so limited space : 6U → 9U

Two analog sum outputs will be used for online LUM monitor independent to DAQ system

Y. Unno (Hanyang)

Status on tsim-ecl

- 1st step

  - Port current Belle tsim-ecl to basf2 package.
  - Prepared same algorithm as Belle tsim-ecl.
 - Check/compare the performance with it.

- 2nd step

  - Implement timing information
  - Try to improve trigger logic
    - Implement new Bhabha veto logic(2D→3D)
    - Optimize threshold of TC, Bhabha*, etc(?).
    - Beam bkg veto(utilize θ).

Simulation with current basf2 code

- 100 events are generated just for check.
  - 10 γ tracks per one event.
  - Each γ has just 1.0 GeV.
  - Uniform in ϕ (ϕ=0°-360°).
  - Uniform in θ (θ=12.4°-155.1°).
  - Inner detectors are included.
  - No background.

> - ECL trigger is based on TC
>   - 1TC consist of ~16Xtals
>   - 576TCs in total
>   - TC threshold = 100 MeV

Output of tsim-ecl
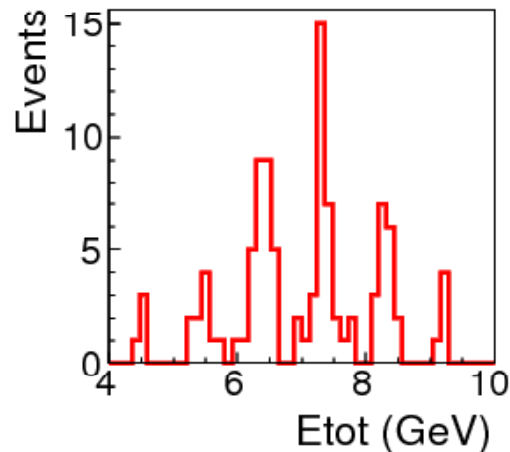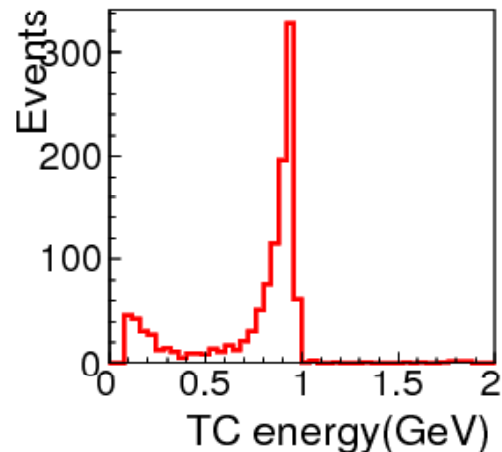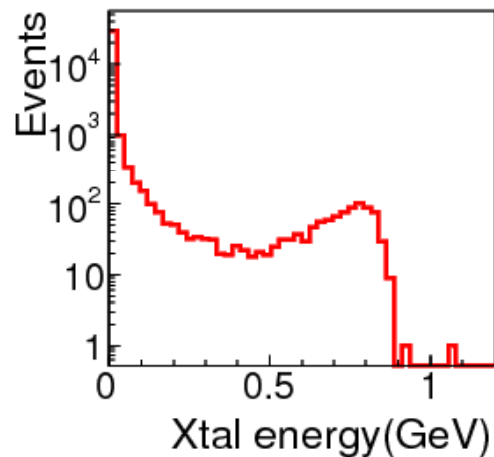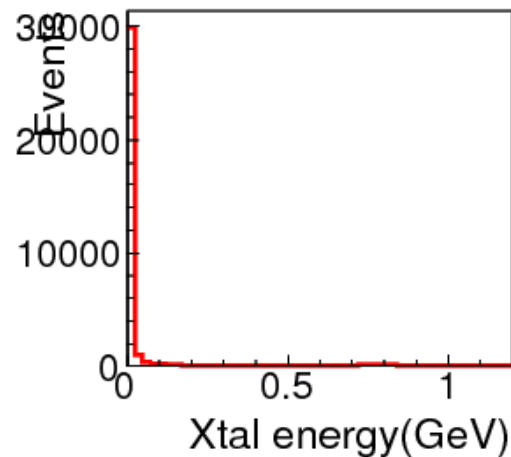
- 100MeV threshold is applied for each TC.
- Etot = barrel + f-endcap(extreme forward is excluded)

Output of tsim-ecl (ICN)
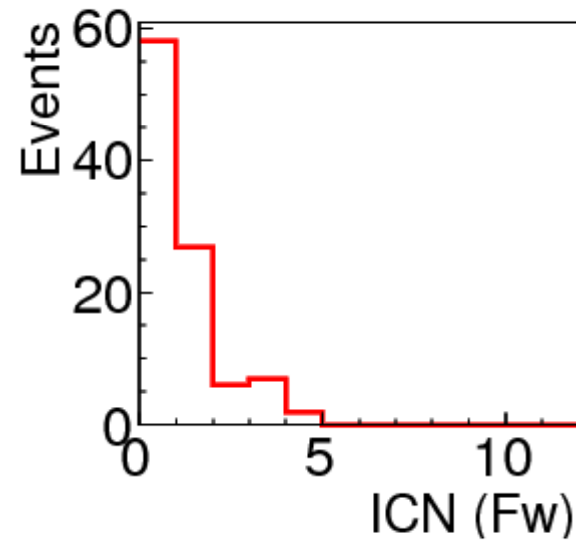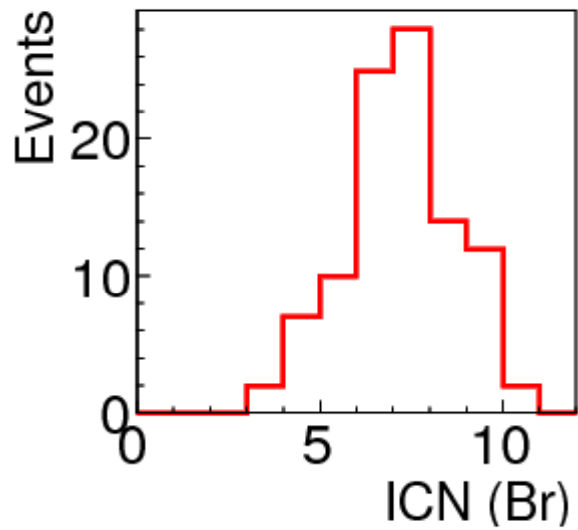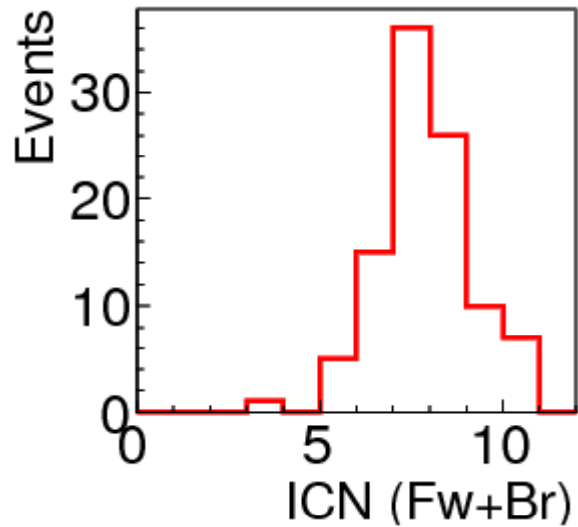
Summary

- Belle2 ECL trigger : FADC/FPGA–based flexible architecture.
- Shaper-DSP, FAM, TMM prototypes are available.
- Fast output in Shaper-DSP :
  - 1μs pulse-width, noise-level < 10MeV
  - Almost final stage to mass-production.
- FAM :
  - 6U → 9U for analog online LUM monitor.
  - Apply TC signal fitting process to get better noise and timing.
- 1st version of basf2 tsim-ecl is ready, but on investigation .

BACKUP

Fast Shaper

New Shaper-DSP Prototype
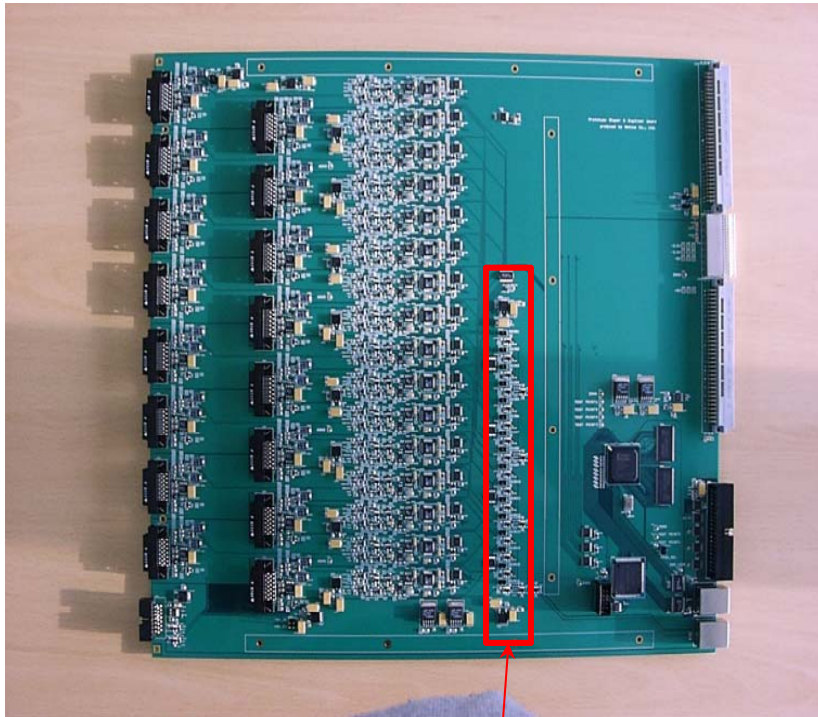
Fast shaper circuits

- Located in Shaper-DSP board
- 576 boards
- Input : 16 counter signals
- Output : 1 TC analog sum
- Fast shaping time = 100ns
- Pulse height correction
- Channel-by-channel calibration
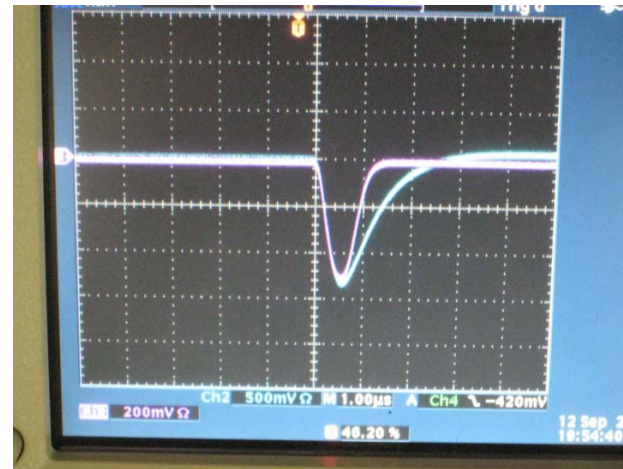
The Cosmic Stand
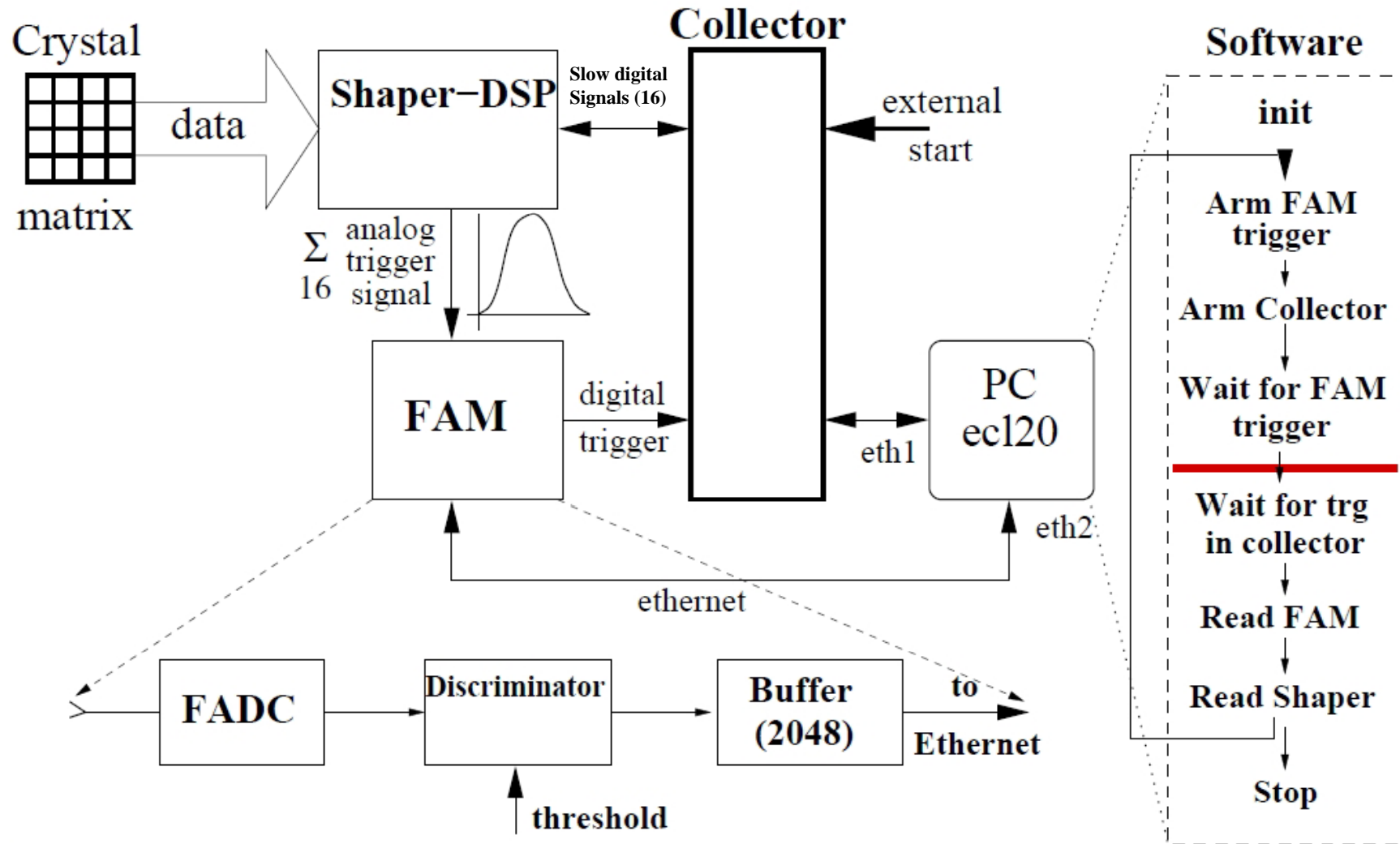
FAM

- 52 boards (one/VME crate)
- Input : 12 x TC analog sum signals
- Output : 1 optical digital signal
  - 12 x TC peaks + discriminator bit
- Operation :
  - Continuous signal digitization @ FADC
  - Find a pulse peak value per each TC @FPGA
  - Compare with threshold (100 MeV) @FPGA
  - Align 12 TC outputs @ FPGA
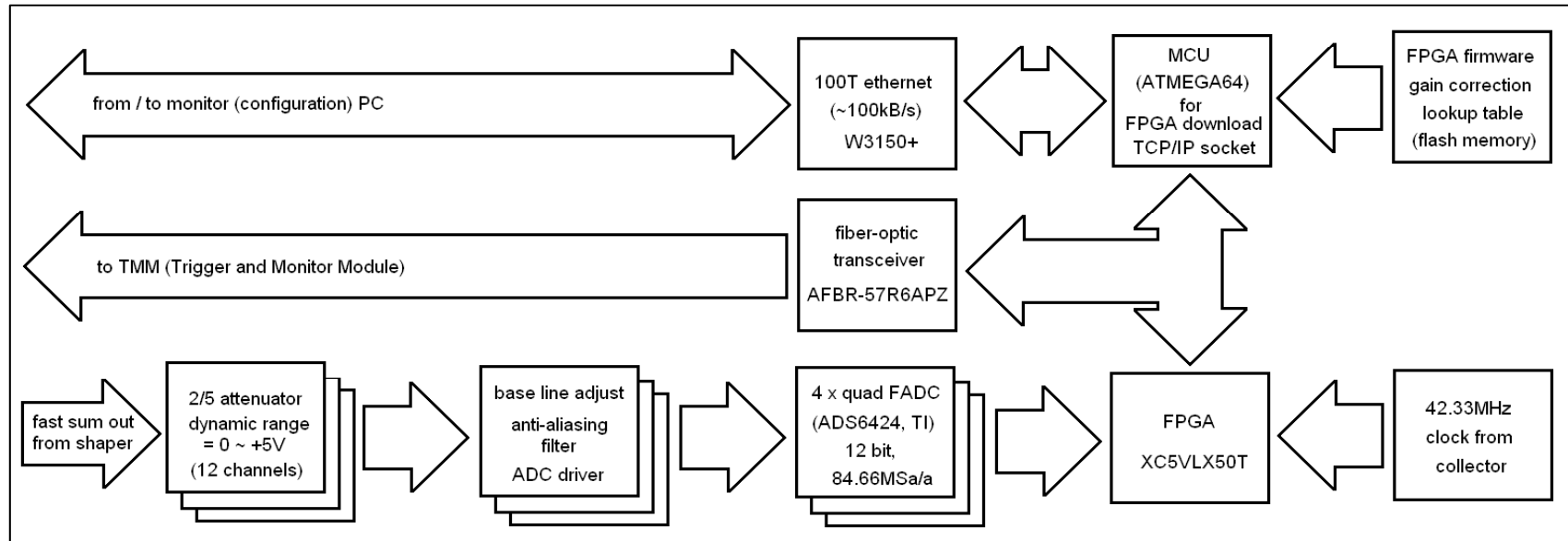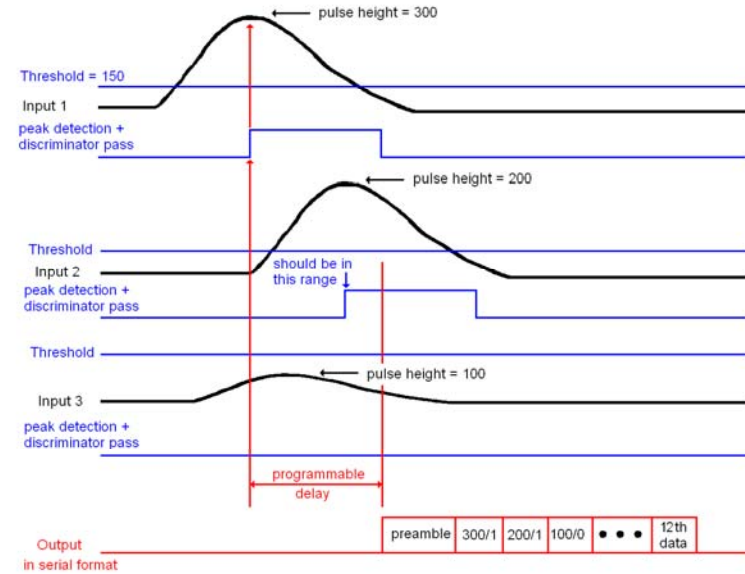
TMM

- 6 (L-1:Merger) + 1(L-2: Master) : same board
- Input : 576 TC signals from 52 FAM modules
- L-1 : 9 inputs from FAM / 2 outputs to L-2 + 4 outputs* to GDL
- L-2 : 2x6 inputs from L-1 / 1 output* to GDL
- Output * : 576 TC raw data to GDL for matching w/ CDC trigger
- Output* : 25 final ECL trigger output to GDL

    4   Calorimeter trigger timings (Final, Fwd, Barrel, Bwd)

    3   Total Energy (> 0.5, 1.0, 3.0 GeV)

    4   Isolated Cluster Number (3 bits + 1 carry-bit)

  13 Bhabha triggers / Barrel Bhabha / Prescaled Bhabha

    1   Beam-BG veto

  ** More useful triggers will be added after TSIM study.

Schedule

	Oct.10	Jan.11	Apr	Jul	Oct	Jan.12	Apr	Jul	Oct	Jan.13	Apr	Jul	Oct	Jan.14
Hardware														
SH-DSP (576)	2nd prototype			final prototype			mass produciton				installation & debug			ready
FAM (52)	1st prototype				final prototype			mass production			installation & debug			ready
TMM (5)	1st prototype					final prototype		mass prod.			installation & debug			ready
ETM (1)	1st prototype					final prototype		mass prod.			installation & debug			ready
Cable								mass production			installation & debug			ready
Cosmic stand			1st integration test				2nd integ. test							
Firmware														
FAM		simple version			full version			final version			debug			ready
TMM		simple version			full version			final version			debug			ready
ETM		simple version			full version			final version			debug			ready
Online software														
FAM/TMM/ETM						code preparation					debug			ready
GDL/DAQ interface						code preparation					debug			ready
Offline software														
Raw data format						consult w/ DAQ group								
Recon code								preparation				debug		ready
TSIM														
Geant-4		code ready & trigger logic study												