Workshop Summary
– DAQ Part –

Takeo Higuchi (KEK)

According to my experience, a good summary starts with a beautiful photo of the workshop/conference site.

I try to make this summary so

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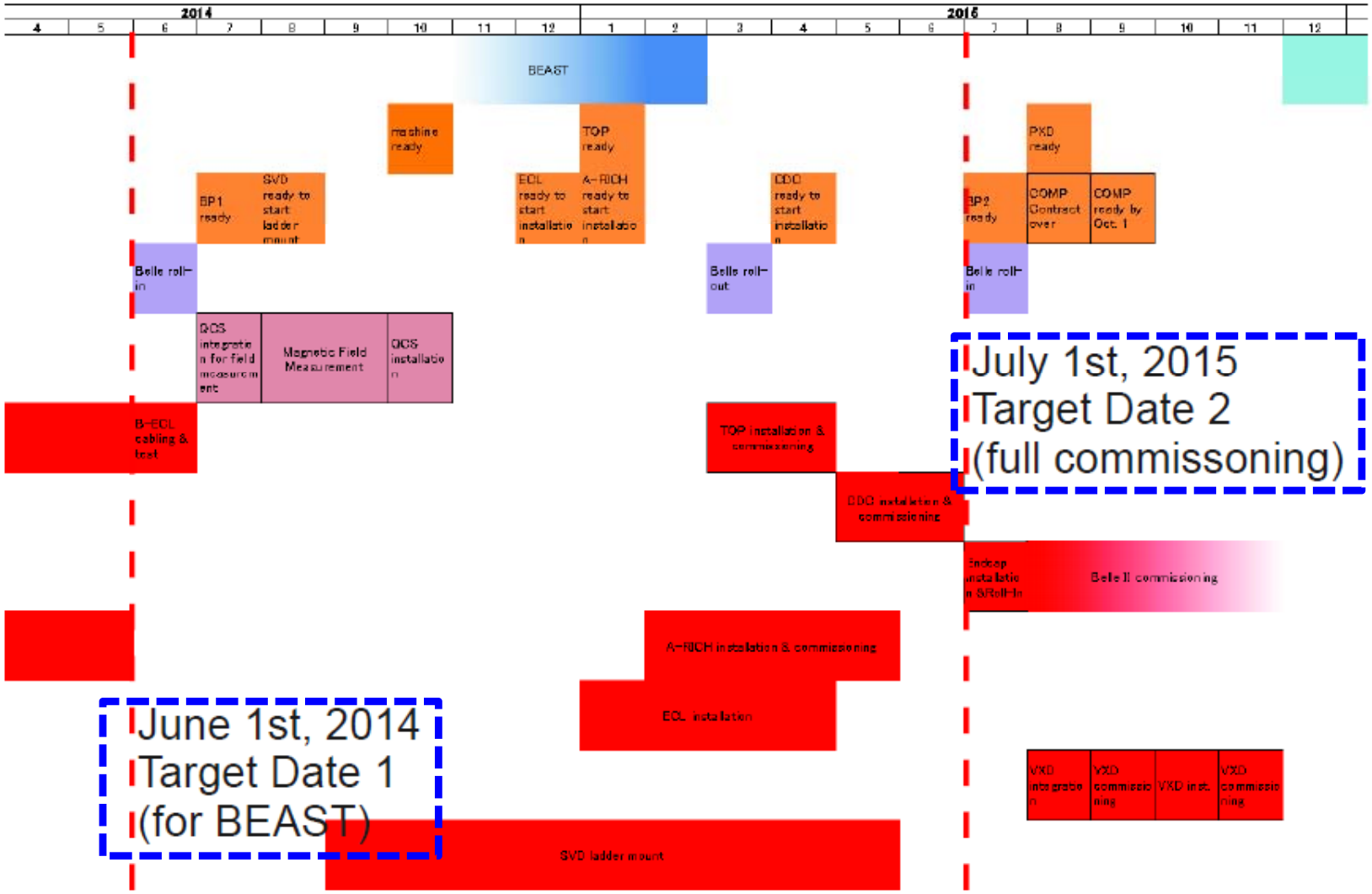
I try to make this summary so

Actually, I left my camera in my hotel room and cannot take the great view seen from Gary-san's house…

Schedule Issues – R.Itoh

- 2 target dates for Trigger and DAQ



Schedule Issues – R.Itoh

- **Toward the BEAST**

Trigger:
* ECL and KLM sub-triggers should be ready by the date
* GDL should also be ready with the special firmware for BEAST operation

DAQ:
* COPPER based readout system for ECL and KLM should be ready.
  - Interface between Trigger and Timing Distribution system
  - Full operaiton of Belle2link including slow control link
* (Partial) event building + (Partial) HLT operation + Public access to online storage for detector studies
* DQM/Monitoring/Run control (skelton) scheme should be ready.

Schedule Issues – R.Itoh

- **Toward the full commissioning**
  - The milestones should be carefully settled, for we have only one month to integrate the PXD to CDAQ.
    - August 2015 … VXD (PXD+SVD) outside the Belle II.
    - November 2015 … VXD (PXD+SVD) for cosmic-ray runs within the Belle II.

BKLM DAQ – G.Visser and B.Kunkler

Prototype Front-End FPGA Performance

- 4 ns time resolution
- 10 +/- 2 ns double pulse resolution
- 528 ns maximum single channel latency due to processing and pipelining
- Simultaneous hit on each channel processed with 948 ns latency
- Simultaneous hit on 4 channels processed with 347 ns latency
- Data output is 8-bit channel value followed by 8-bit time value

Requirement: <5ns

- **Amendments**
  - TDC buffer depth: a 5-µs buffer is to be implemented.
  - Number of Belle2Links = 16

EKLM DAQ – D.Liventsev

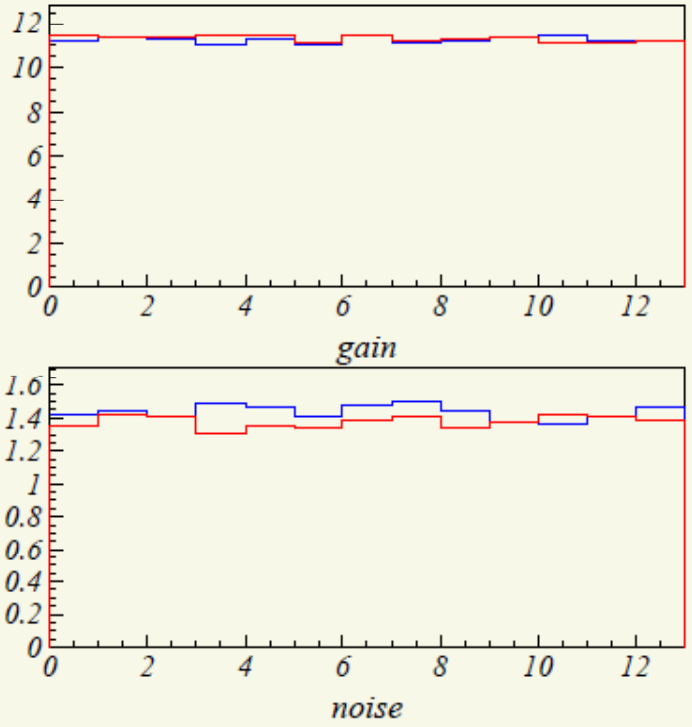
Amplifiers and carrier board are installed inside detector;

No maintenance is planned;

Amplifiers should survive ~ 15 years of Belle II operation.

12 amplifiers and the carrier board were irradiated in ITEP with 200 GeV protons.

100% corresponds to 10^{11} protons/cm^2, which is equal to 15 years of Belle II operation.



First bin – not irradiated, the rest in order of dose increase.

Blue – before irradiation, Red – after irradiation.

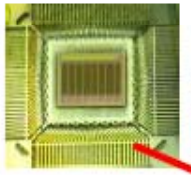
No significant radiation damage is observed.

ECL DAQ – V.Zhulanov

- **ECL collector module**
  - Mission
    - Collects and merges data from 12 connected ShaperDSPb modules.
    - Provides interface with Belle II CDAQ and FTSW.
  - Planned upgrades
    - Virtex5 → Spartan6 (cheaper option)
    - 100M → 1000M Ethernet
  - System test
    - The system is successfully integrated with the FTSW (trigger-signal decoding is working fine).
    - Integrated system test with HSLB shows some problems (the test was carried out in collaboration with Liu-san).

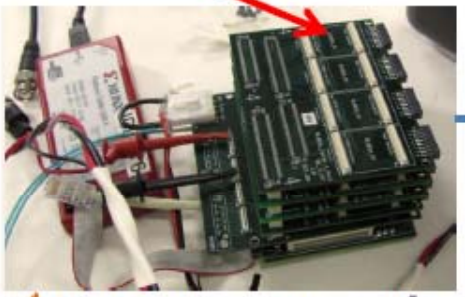
BPID Test at Fermilab
– M.Andrew and K.Nishimura

Beam Test Electronics Elements



Waveform sampling ASIC (IRS2/3)

Aurora-based fiberoptic data

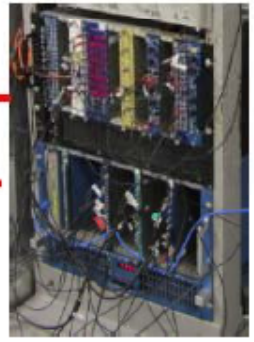


SCROD-based board stack (Spartan-6)

Timing/trigger distribution (CAT-6)

DSP_cPCI (Spartan-6)

FTSW



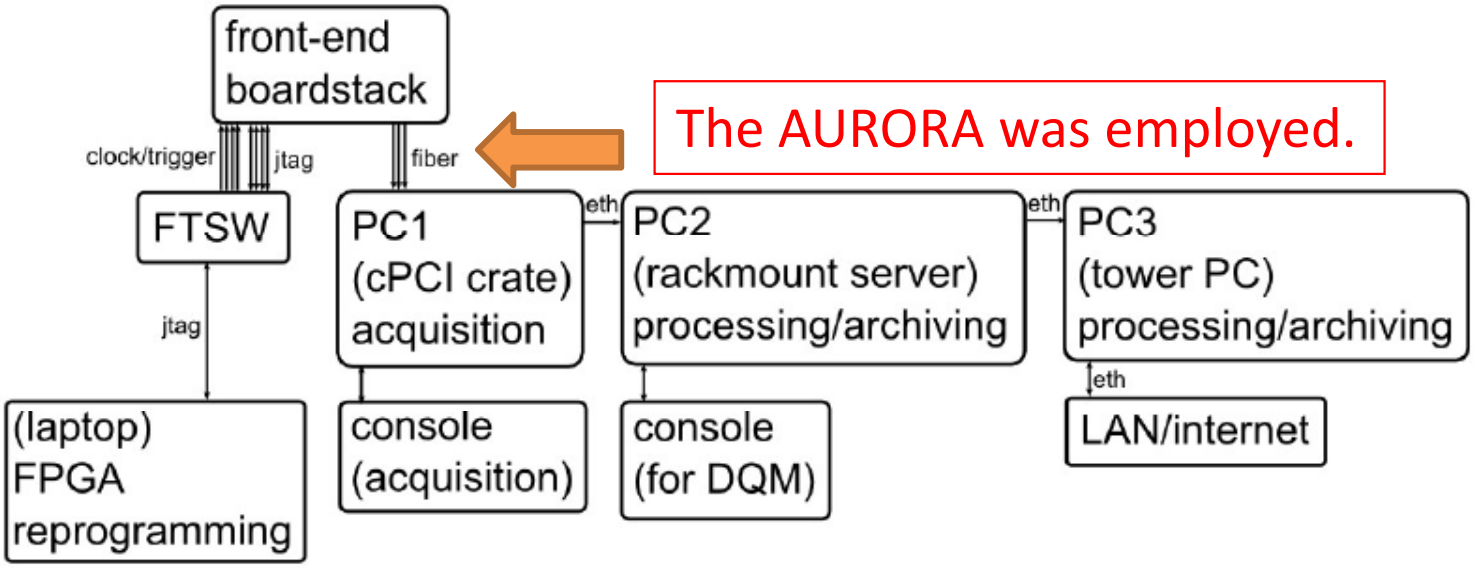
NIM trigger logic

CAMAC TDC (trigger phase alignment)

Remote programming link (CAT-6)

BPID Test at Fermilab
– M.Andrew and K.Nishimura

DAQ at T-1019
data transfer / processing topology

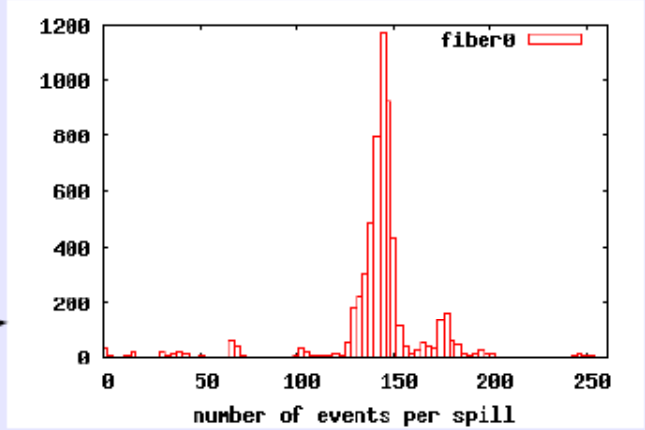


- no zero-suppression (record 256 sample waveforms from all 384 channels)
- trigger causes a gate generator to latch; not cleared until all data is readout

BPID Test at Fermilab – M.Andrew and K.Nishimura

DAQ at T-1019 statistics

- duration of beam test: 14 days * 12 hours/day
- spill structure: 4 s / 56 s
- number of spills: 5770 (out of 10080 possible spills)
- uptime: 57% (neglecting accelerator downtime)
- quantity of raw data acquired: 182 GB
- quantity of calibration data acquired: 179 GB
- average data collection rate during spill: ~8 MB/sec
- maximum instantaneous data collection rate: ~14.4 MB/sec (sans CAMAC)
- number of times a front-end module missed a trigger: 41 (99.3% of triggers were seen)
- number of times an FPGA needed to be reprogrammed (other than just after power-up): 18
- quantity of DST1/2/3/4 data: 215GB/319GB/?/?



Link with the FTSW was lost. No signal digitization any more.

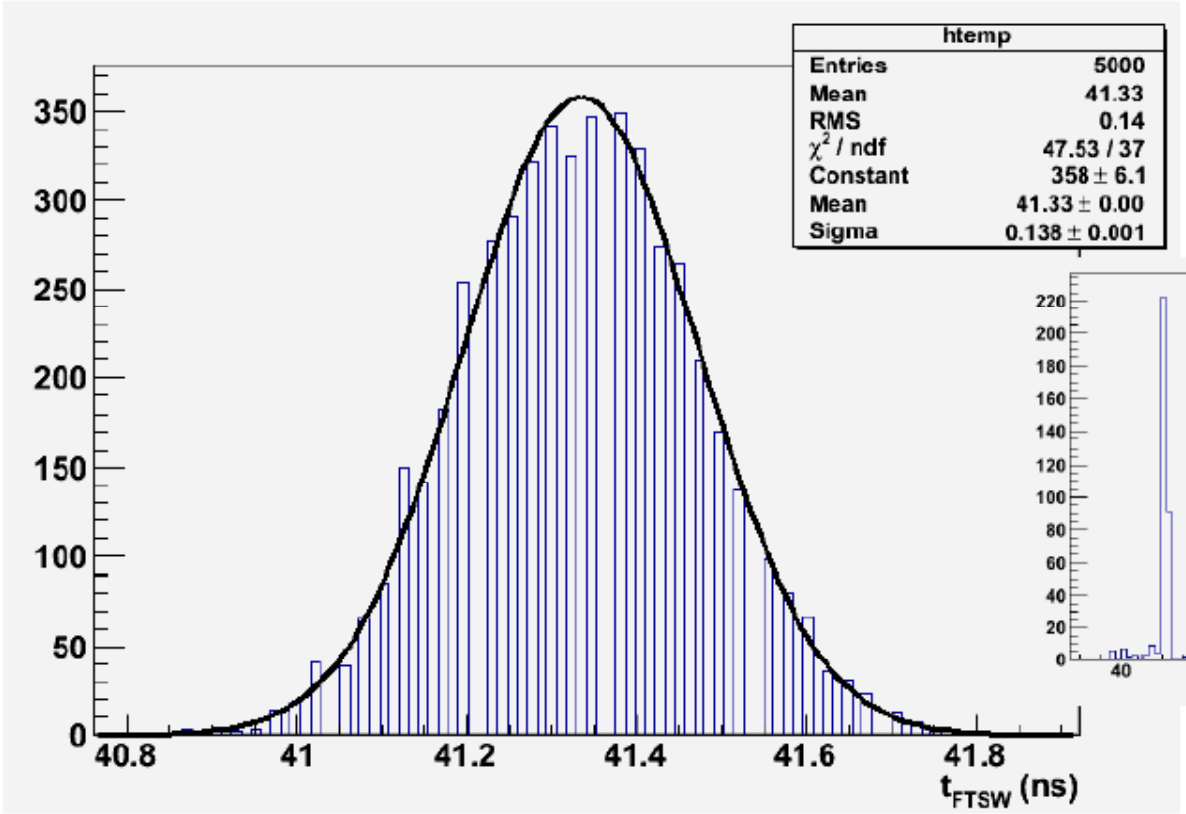
BPID Test at Fermilab – M.Andrew and K.Nishimura

- **Remote programming**
  - **Generally quite successful. A few issues:**
    - Programming sometimes worked at 6 MHz…
    - …but often had to be run at 1.5 or 0.75 MHz.
    - Sometimes failed completely. Reseating cables seemed to help, but there was never an obvious cause.

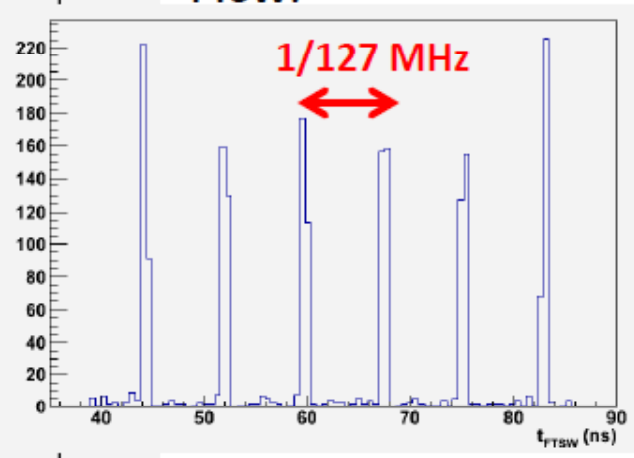
BPID Test at Fermilab
– M.Andrew and K.Nishimura

Measured FTSW Timing - "Special" Laser Runs

- Typical TDC distribution of trigger phase:



Trigger phase measurements when module loses its synchronization with FTSW:



- Distributed timing jitter: still under investigation… much worse than originally thought? If so, why?

EPID DAQ – S.Nishida

- **Update of expected # of B2links and COPPERs**

	#ch	occ [%]	#link	/link [B/s]	FNS	#CPR	ch sz [B]	ev sz [B]	total [B/s]	/CPR [B/s]
PXD	8M	2	40	364M	—	—	4	320k	14.4G	—
SVD	243456	1.9	40	13.8M	HSLB	40	4	18.5k	555M	13.8M
CDC	15104	10	302	0.6M	HSLB	75	4	6k	175M	2.3M
BPID	8192	2.5	128	7.5M	DSP	16	16	4k	120M	8M
EPID	77760	1.3	138	0.87M	HSLB	35	0.5	4k	120M	15M
ECL	8736	33	52	7.7M	HSLB	26	4	12k	360M	15M
BKLM	21696	1	86	9.7M	DSP	6	8	2K	60M	10M
EKLM	16800	2	66	19.5M	DSP	5	4	1.4k	42M	5.3M
TRG					HSLB	60				
	65664	1.5	78	1.1M		20?	2.8	2.8k	86M	2.2M?

EPID DAQ – S.Nishida

SA03

SA03

- Shorter shaping time.
  - ✓ Larger noise (worse S/N) in neutron irradiated HAPD.
  - ✓ SA02 : 250ns – 1000ns
  - ✓ SA03 target : reduce to half of SA02
- Tolerance to a single event upset (SEU).
  - ✓ ASIC itself is radiation tolerant (tested with SA02).
  - ✓ SEU may affect parameters in SA02.
  - ✓ Dual interlocked cell (DICE) for registers.
  - ✓ Non-destructive parameter readout.

Can the SA03 be the final version?

First samples by TSMC were delivered in Sep. 2011.
Production at X-FAB is also going.

The SA03 from two vendors are under competition.

Available SA03 at 2012 Mar. (expectation)

	bare chip	QFP	LTCC
TSMC	40	5	30
X-FAB	~30	5	

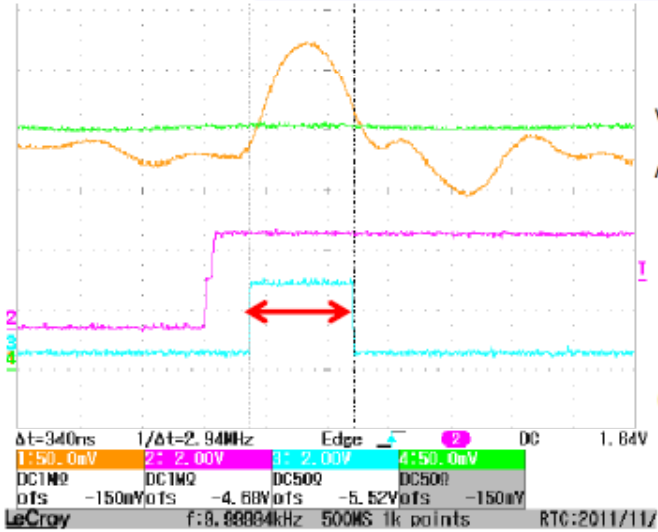
LTCC package for SA03 is also in production.

EPID DAQ – S.Nishida

Front-end Board

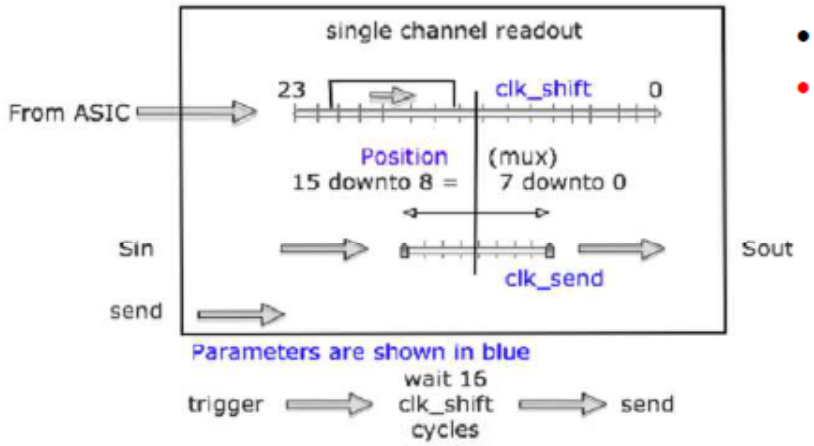
Possible improvement

- Now, we only readout on/off information for each channel (4 timings every 2us).
- If we measure the time over threshold, we may be able to distinguish single and multiple photons.



clk_send = 50MHz
clk_shift = 5MHz

readout time 144*8*20ns = 23us
(23us = 44kHz) > requested 30kHz



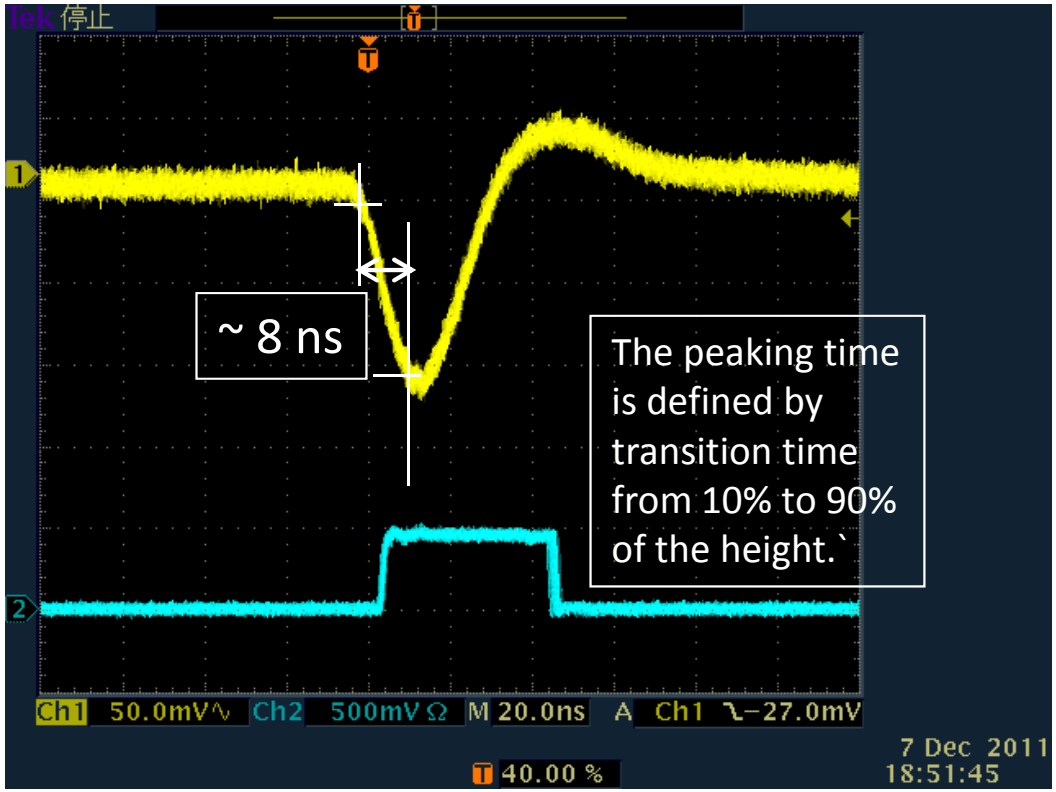
- The logic is in study in Ljubljana.
- This increases the data size.
  - ✓ 1 hit : 18(chID) + 4(hit)
    = 22 bit
    → 18 + 4 +8(?) = 32 bit
  - ✓ Not significant to Belle2Link
  - ✓ More impact on the connection between FE and mergers.

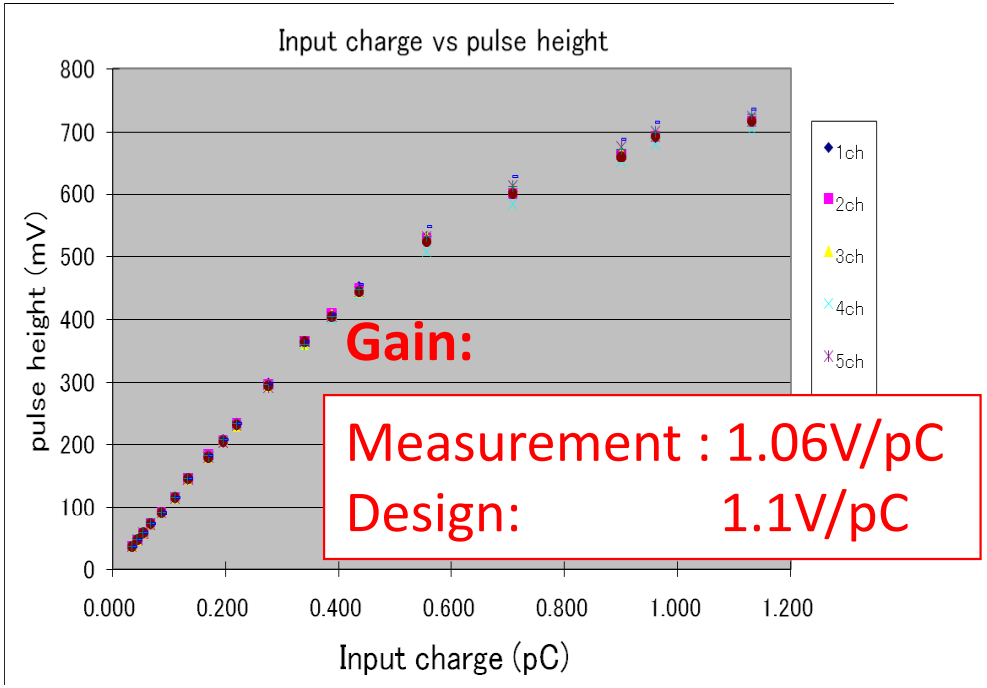
Readout of "time-over-threshold" is proposed.

CDC DAQ – S.Uno

ASIC (amplifier-shaper-discriminator (ASD) chip)

Input : 0.13pC

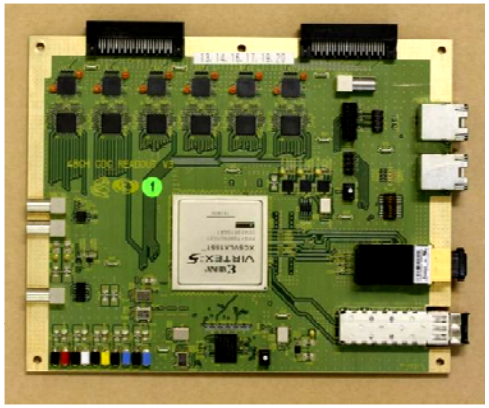


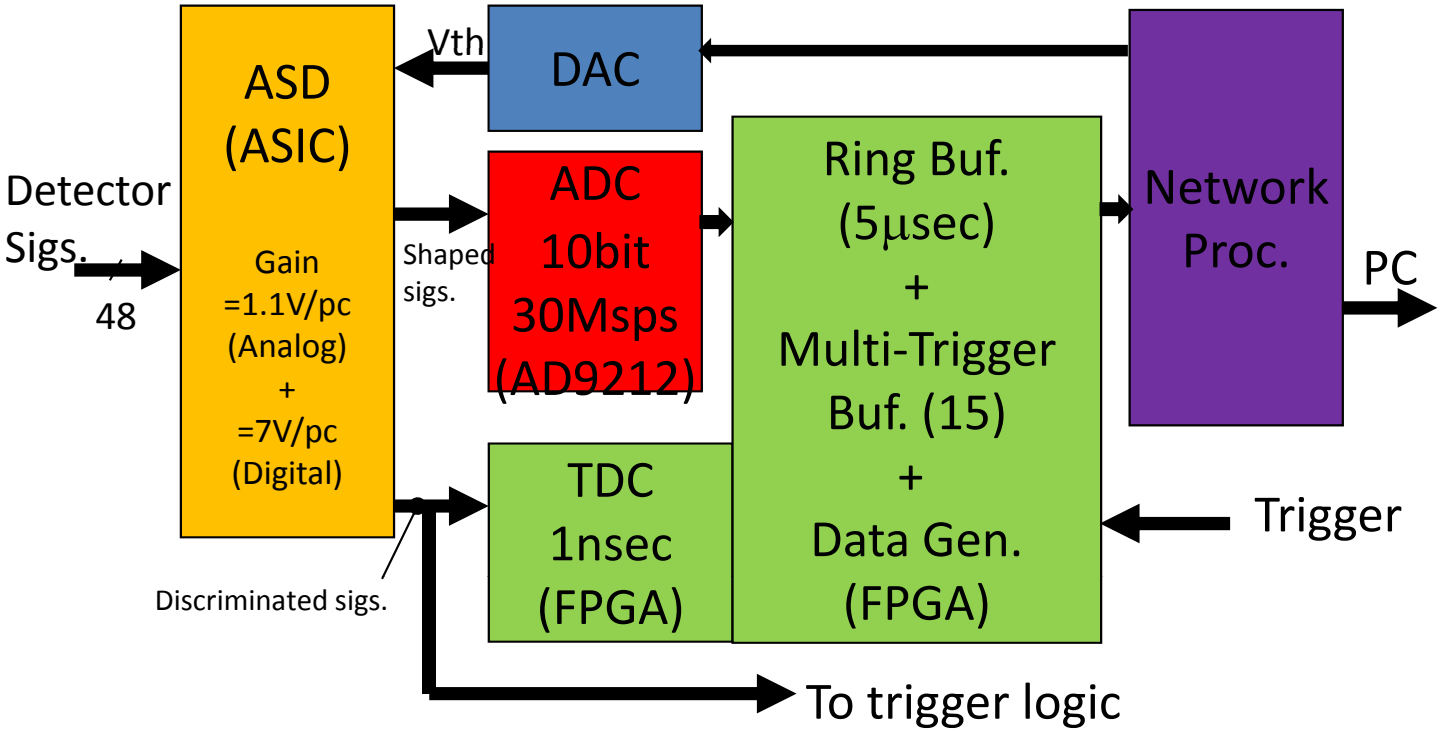


CDC DAQ – S.Uno

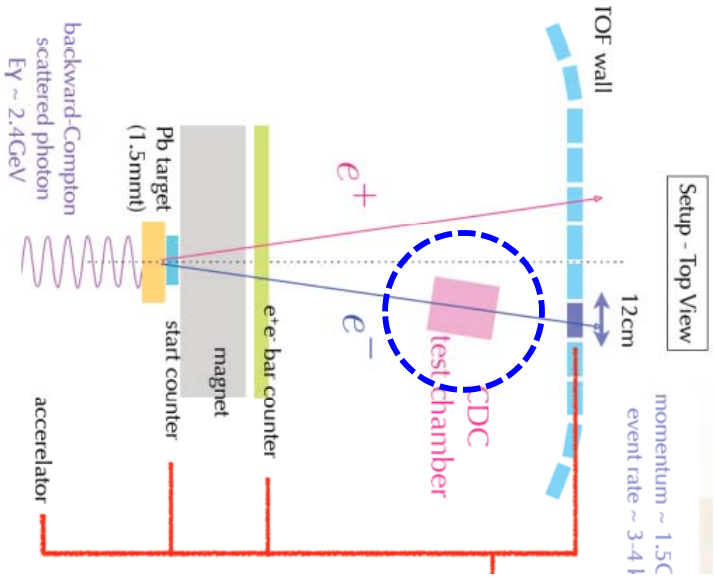
Readout board

Version 2&3 in 2011





CDC DAQ – S.Uno (& N.Taniguchi)

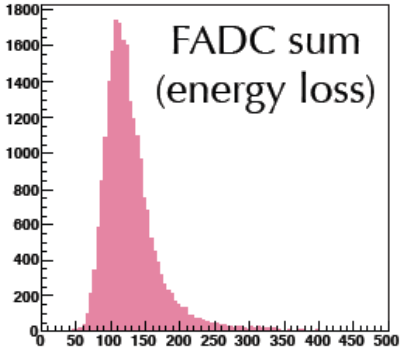


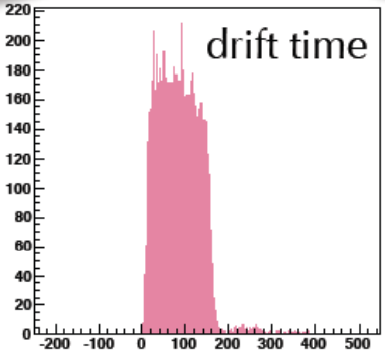
Beam test setup in Spring-8

t=0 by scintillator

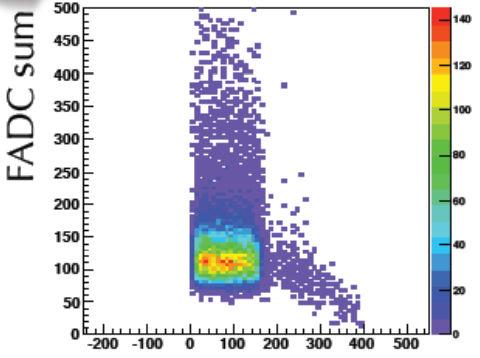
Prototype-CDC performance

track-associated hit



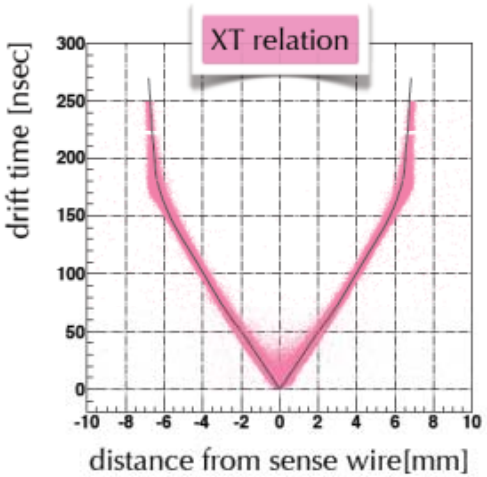


T₀ - TDC [nsec]



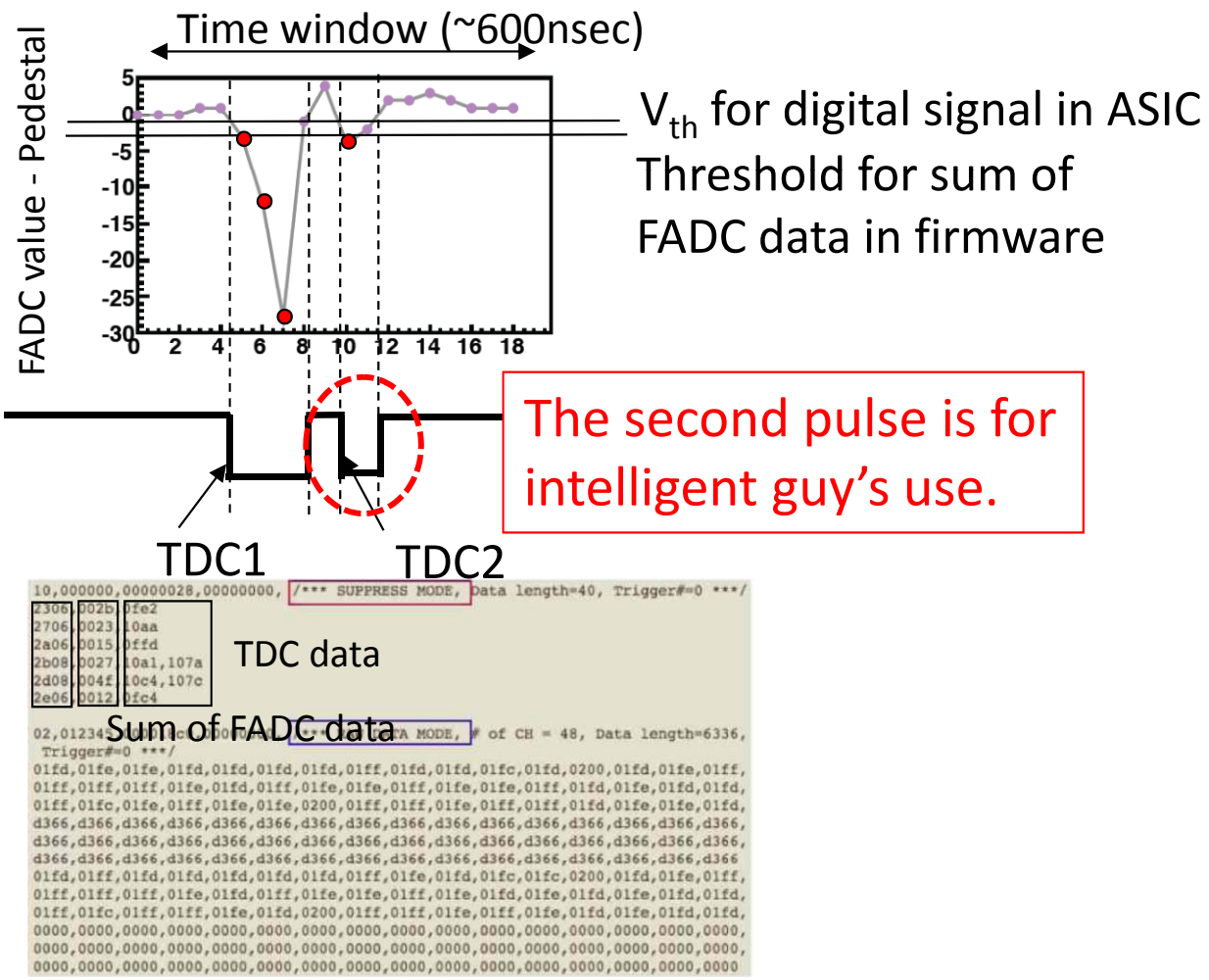
position resolution analysis

HV=2.3kV (Belle typical)



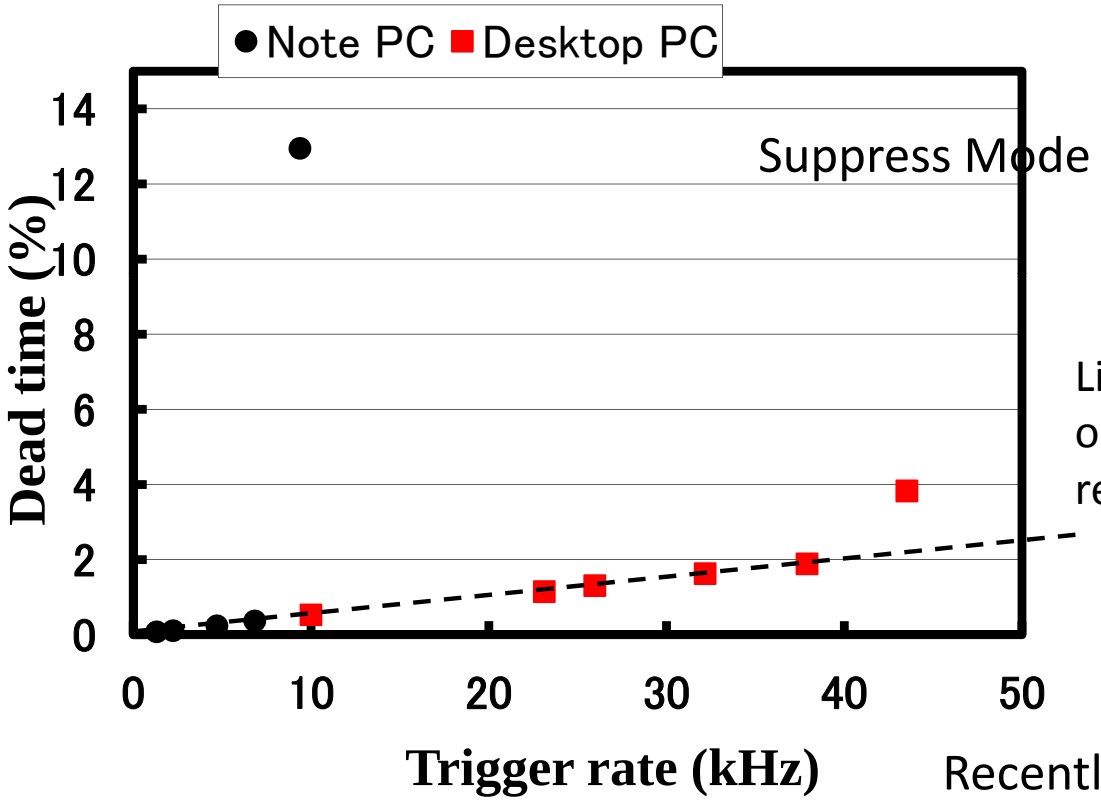
CDC DAQ – S.Uno

- **Two readout modes are proposed.**
  - Transparent mode
  - Suppressed mode
    - For the real operation?



CDC DAQ – S.Uno

Deadtime fraction



Linear part is independent on performance of readout PC

0.5%/10kHz

Recently, T. Uchida found a bug in the firmware. It will be reduced by factor ~10.

The system has at least ~500ns intrinsic deadtime. When the next trigger comes during this period, it was totally discarded → fixed.

CDC DAQ – S.Uno

- **Requests/suggestions to DAQ group**
  - It is better to implement the link by each detector group.
  - To implement the link by each detector group, providing an FPGA library of Belle2Link, their documents, and a test bench for the Belle2Link at KEK would be very helpful.

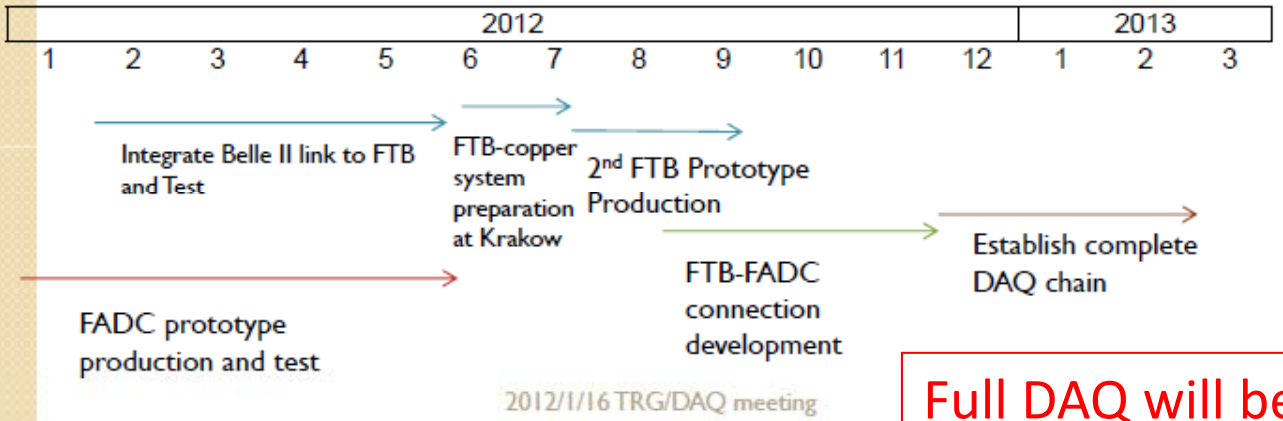
Z.Liu-san is working on the documentation.

SVD DAQ – K.Hara

2012-13 SVD DAQ Work Plan

- Establish FTB-Copper connection
  - Need to integrate Belle II link to FTB at KEK

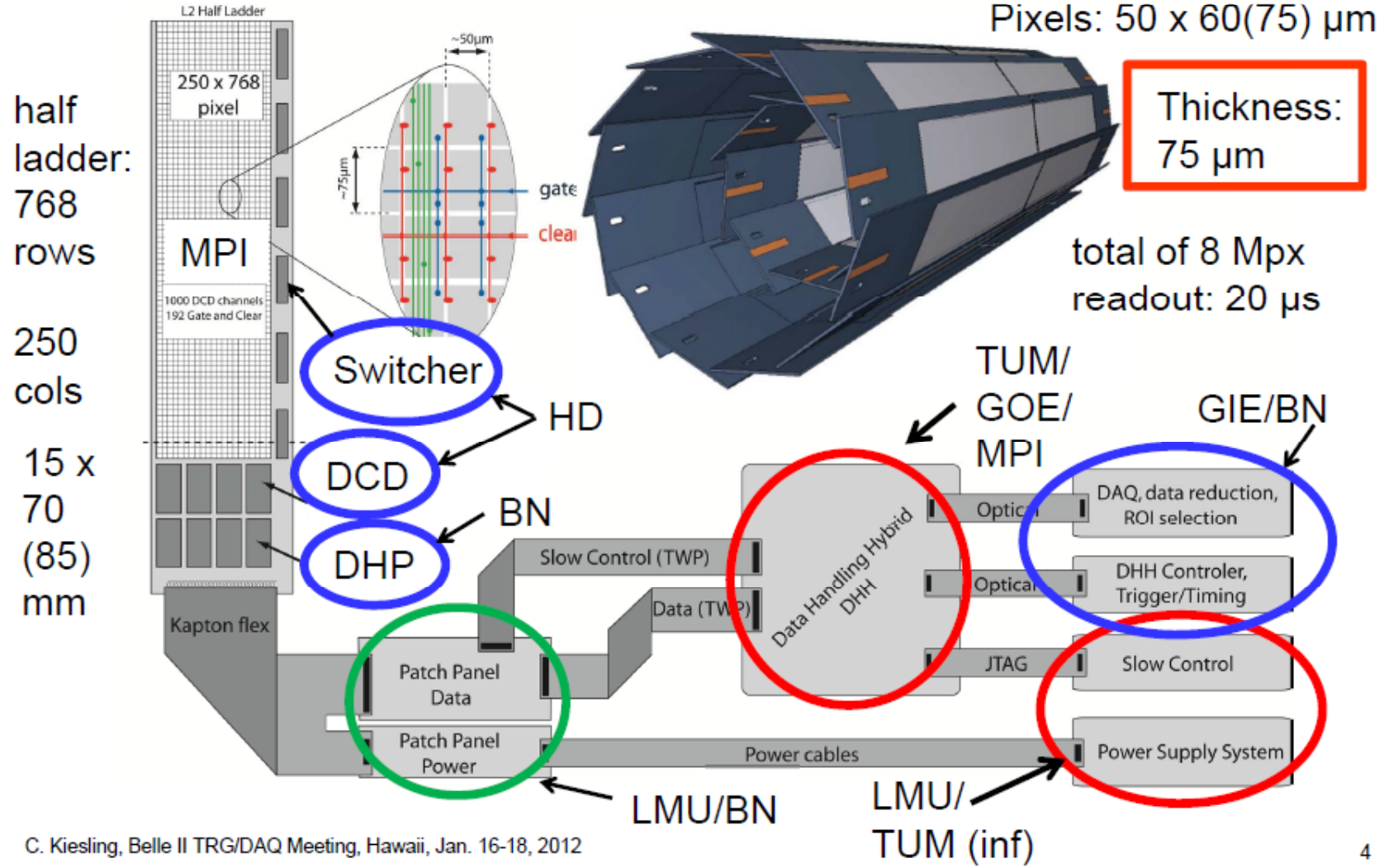
    Translation from virtex to spartan is necessary. → SVD
    - Hara, Ishikawa (Tohoku), Joo (SNU) and Wacek (Krakow) will work on that.
- Establish FTB-FADC Connection
  - FTB-FADC development at Krakow
- EstablishAPV25-FADC-FTB-Copper chain by 2013 BPAC



Full DAQ will be ready by 2014.

PXD DAQ – C.Kiesling

PXD DAQ-Chain - Layout



PXD DAQ – C.Kiesling

- **Data handling hybrid**

Incoming data 4x1.5Gb/s (4 DHP's per PXD half ladder)
Data buffering
Data Reformatting and Remapping

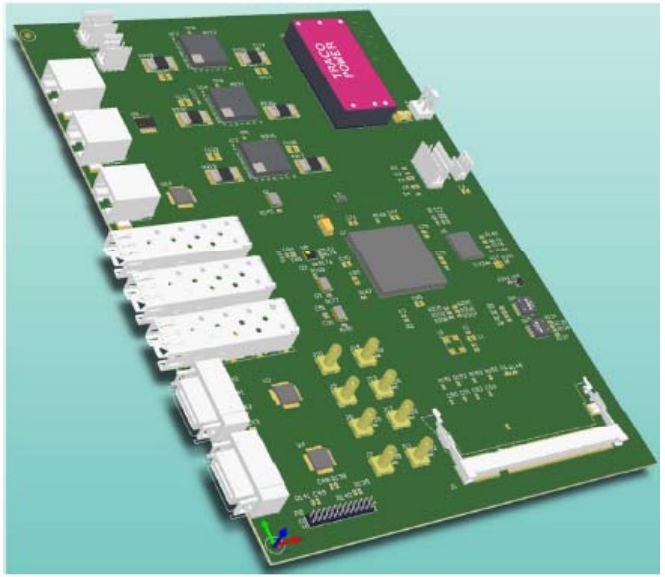
Housing clustering ASIC ("DCE") on piggyback card
(DDR2 SODIMM)

Further processing of cluster information in FPGA
Merging four DHP data streams into two streams 2x6Gb/s
Dead time generation to prevent data loss

Translate signal from copper to optical -> ATCA

Timing and Trigger Distribution

JTAG interface for slow control (JTAG master to Belle II)



DHH prototype
(2 modules delivered in mid november)

PXD DAQ – C.Kiesling

Revised Schedule of PXD

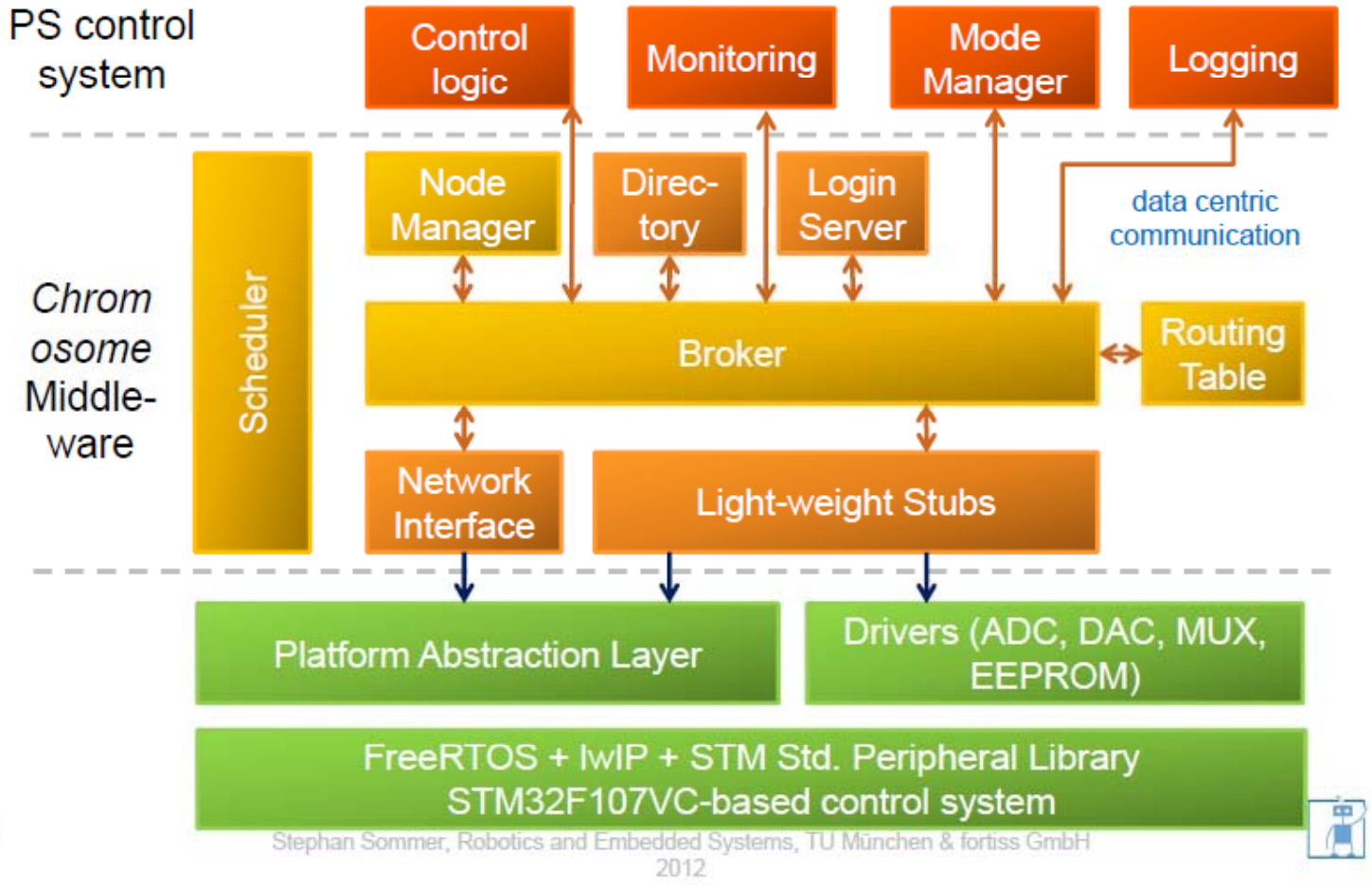
(Some) milestones in the PXD construction

finish evaluation of PXD6 (test production):	Oct. 2011
start prototype (PXD9) production	Feb. 2012
power / cooling / DAQ ready (test)	Jan. 2013
Finish prototype production	Feb. 2013
Start final DEPFET production	July 2013
„Telescope Test“ at DESY („full“ DAQ + slow cont.)	Fall 2013
all ASICs produced	Feb. 2014
BEAST II near beampipe ready	Oct. 2014
finish final DEPFET production Batch 1	Feb. 2015
finish final DEPFET production Batch 2	May 2015
power / cooling / DAQ ready (installed)	July 2015

1/10 SVD
+
partial PXD

PXD HV Control – S.Sommer

PXD Power Supply Nodes: Software Architecture



Chromosome middle-ware was proposed as a direct I/F with the PXD HV system. Structure of layers (NSM, PVSS, Chromosome *etc*) would be better to discuss well.

Radiation Study Errata – T.Higuchi

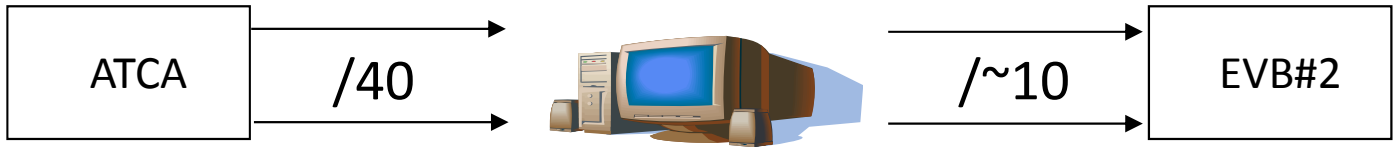
- **Permanent damages (lifetimes)**

Device	Neutron	γ-ray
Virtex5 FPGA	> 20-year-equivalent	> 88-year-equivalent
Optical transceivers	> 12-year-equivalent	**3-year-equivalent ☹**
Voltage regulators	N/A	> 25-year-equivalent

- **Data-error rates (entire Belle II CDC)**
  - One SEU (recoverable w/o penalty) per ~ 4 minutes.
  - One unrecoverable error per ~11.5 hours.

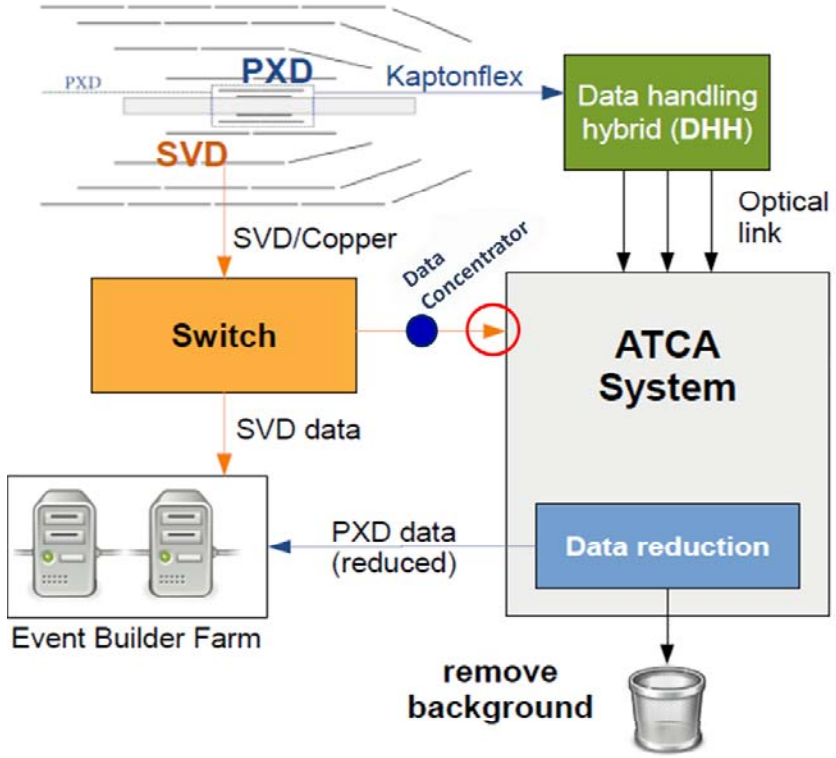
PXD DAQ News – S.Lange

- **Send PXD data by GbE to CDAQ**
  - Plan A
    - GbE by PowerPC (Linux) UDP or TCP/IP software
      - 18 MB/s required, ~26 MB/s achieved
  - Plan B (only if plan A does not work)
    - GbE by optical link UDP hardware
      - Achieved rate at <60 MB/s
    - GbE by siTCP TCP/IP hardware
      - >100 MB/s achieved from CN3 to PC



A UDP→TCP packet-converting PC is proposed.
>200 byte UDP packet is preferable if load of the PC is concerned.

DATCON – S.Lange



- Data Concentrator (DatCon) for data reduction with an FPGA-based track finding algorithm
- Input: 42 optical links with 1.5 Gbps line rate
- Output: One Ethernet and two 6.25 Gbps high speed links

- Hardware: 12 AMC cards in an ATCA shelf with 3 carrier boards

TTD – M.Nakao

Requirements

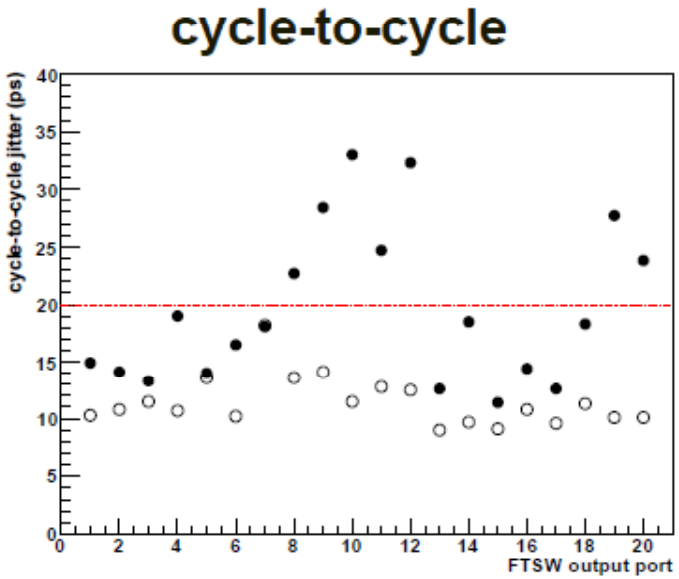
1. **~1100 destinations**
   — 600 (CDC, BPID, EPID) are inside the detector
   — large multiplication factor, compact cable
2. **5 μs total latency for SVD, ~0.5μs for TTD**
   — encoding / decoding (for compact cable) takes time
   — homemade encoder/decoder to bypass intermediate steps
3. **BPID needs <20 ps jitter, Belle2link needs <30 ps jitter**
   — degradation by long metal cable
   — degradation by clock recovery
   — jitter cleaner and careful design

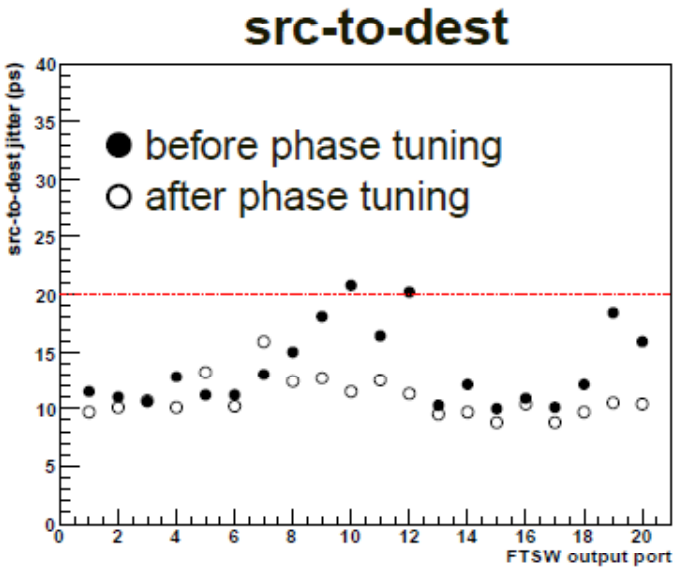
The key-requirement parameters are shown.

TTD – M.Nakao

Jitter result

The jitter cleaner satisfies the BPID requirement.





- **FTSW port dependence, due to phase between CLK & TRG**
- **Close circle before phase tuning, open circle after tuning**
- **Delay tuning brings the jitter below 15ps in most of cases**
- **Two distributors with the same delay setting, with 0.3ns diff**

(similar results with other modules, need systematic measurements)

Rate Reduction – R.Itoh

Proposal: Use of Prompt Reco as a final software trigger

- On HLT : Loosen selection criteria
  * Hadron A selection instead of Hadron BJ.
    - Hadron A has looser selection criteria.

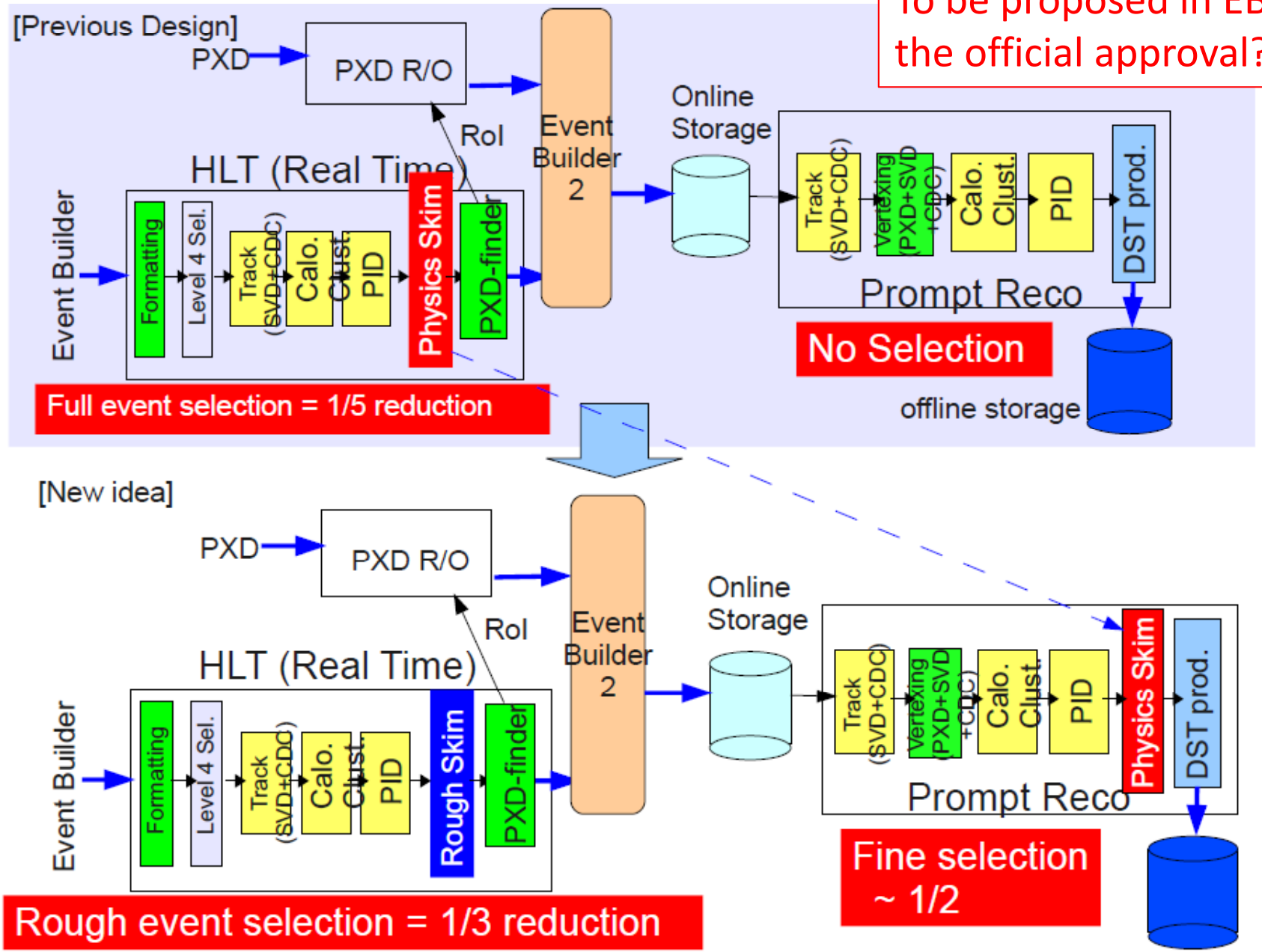
```
        # of hadronic events : 3528666    <- Hadron A
      #hadronic w/ high mult : 2102071
       #hadronic w/ low mult : 1426595
   #hadronic from tight cuts : 1346292
  #hadronic events w/ R2<0.2 : 445736
      #hadronA w/ Jpsi cand. : 385864     <- Hadron "J"
                   #hadronB : 2009592    <- Hadron B
         #hadronB w/ R2<0.2 : 642469
```

  * Loosen tautau selection + inclusion of some of two photon sel.
    => ~50 % increase in the HLT rate is expected.

- On Prompt Reco : Final tight selection
  * "HadronBJ" after the full event processing with
    - almost-final run-by-run calibration constants
    - tracking/vertexing with PXD
  * Physics oriented skims for intensive rare decay events
    (B->lν, B->hγ, τ->μγ, low multiplicty tau decays.....)
  * "Full recon" selection using Hadron A

Rate Reduction – R.Itoh

To be proposed in EB for the official approval?



Size Reduction – R.Itoh

Reduction of COPPER data

- The data from detector front-end are assumed to be well compacted already by FPGA processing.

- Additional raw data processing is possible using COPPER CPU (Linux operated + basf2 environment), but mostly for data formatting and monitoring because of limited CPU power (ATOM 1.6GHz).

- Reduction is also possible at Readout PC under the same software environment (basf2 on linux).

Any processing required for data reduction on COPPER and R/O PC?

* In the data formatting, it is possible to remove redundant headers in the raw data sent through Belle2link (as we did in Belle's AMT readout) -> >20% reduction expected.
* The processing heavily depends on detector's own data format.

Belle2Link – Z.Liu and M.Nakao

Task of KEK test

IHEP people visited KEK to study the B2Link.

- By Dehui,Jinzhou,Nakao,Zhen-An with help from Uno, Taniguchi ,Higuchi,itoh,...
  - Reading firmware for 48ch version CDC FEE OK?
  - Slow control functions OK with 48ch CDC FEE ?
  - Real trigger through TTD OK?
  - Reading 2-4 48ch CDC FEE board with FSLB/COPPER
  - Joint test with CDC detector prototype
  - Test with ECL FEE board

Belle2Link – Z.Liu and M.Nakao

Summary of 48ch CDC FEE boards test

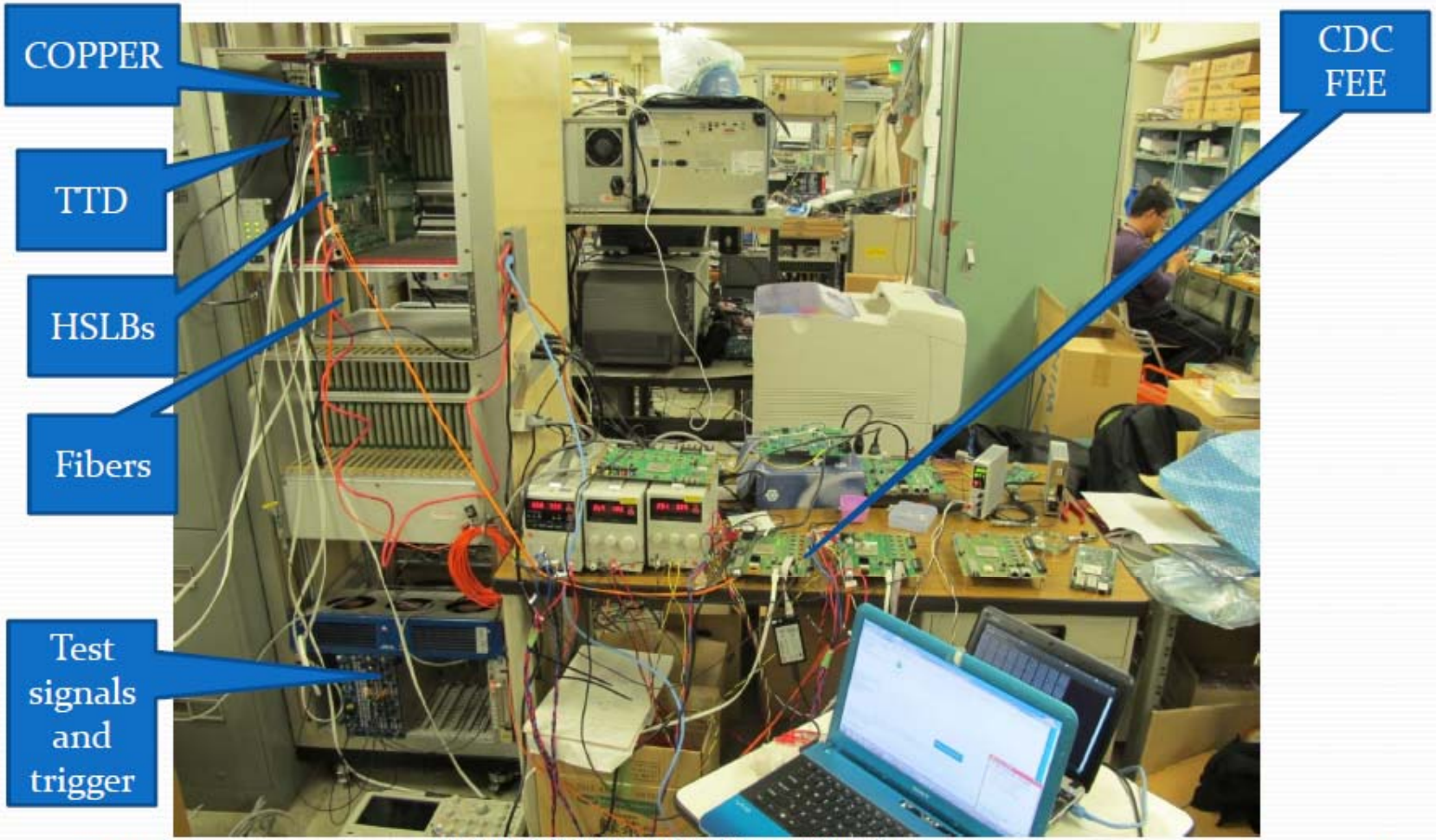
- CDC FEE #2(ver.3) unstable, returned to electronics
- The CDC #1(ver.3) is sensitive for the 1.0v PS
  - High quality PS for 1.0v
  - Be careful with the difference between PS reading and the Pin voltage
  - The core volt. must be near 1.0
  - The high quality PS helps, but need further checking
- The CDC #3(ver.1) is better. Further test is expected.

Bad BER

- Reason: Second hand FPGA might be the reason.

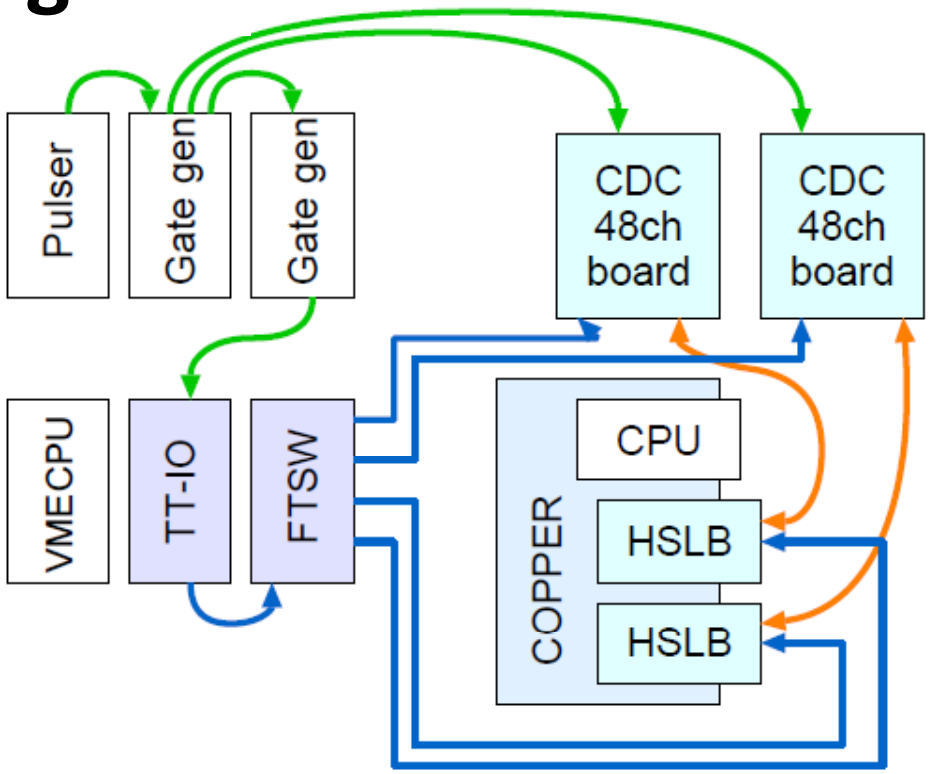
Belle2Link – Z.Liu and M.Nakao

Further test on CDC detector



Belle2Link – Z.Liu and M.Nakao

Block diagram



Study summary

- 1-4 FEEs/HSLBs reading OK
- Disk data saving OK
- CDC window, delay, threshold, pedestal setting OK

- Pulser + gate generator for a test pulse and a delayed trigger
- TT-IO as NIM to LVDS/RJ-45 converter and trigger gate
- FTSW to distribute clock and trigger
- Two boards read out together

Belle2Link – Z.Liu and M.Nakao

Need more address space!

- **CDC firmware handles A32D8 address/data for control**
  - A7D8 of Belle2link is not enough, despite we though CDC board does not have many parameters to fill it
  - Current CDC firmware cannot set the data output phase of the ADC chips, and cannot fully readout data
- **Suggestion: general A32D8 register I/O on top of A7D8**
  - 4 A7D8 registers for address: **A31_24, A23_16, A16_8, A7_0**
  - 1 A7D8 registers to write: **DATAo**
  - 1 A7D8 registers to read: **DATAi**
  - 1 A7D8 registers to stream write: **DATAso**
  - 1 A7D8 registers to stream read: **DATAsi**
  - 2(or 4?) A7D8 registers to stream length: **DATAlen**
- **Could be implemented for CDC, and helpful for others**
  - better to interface LOC_REG instead of Para_decode setting registers

Redefinition of A7D8 was proposed.

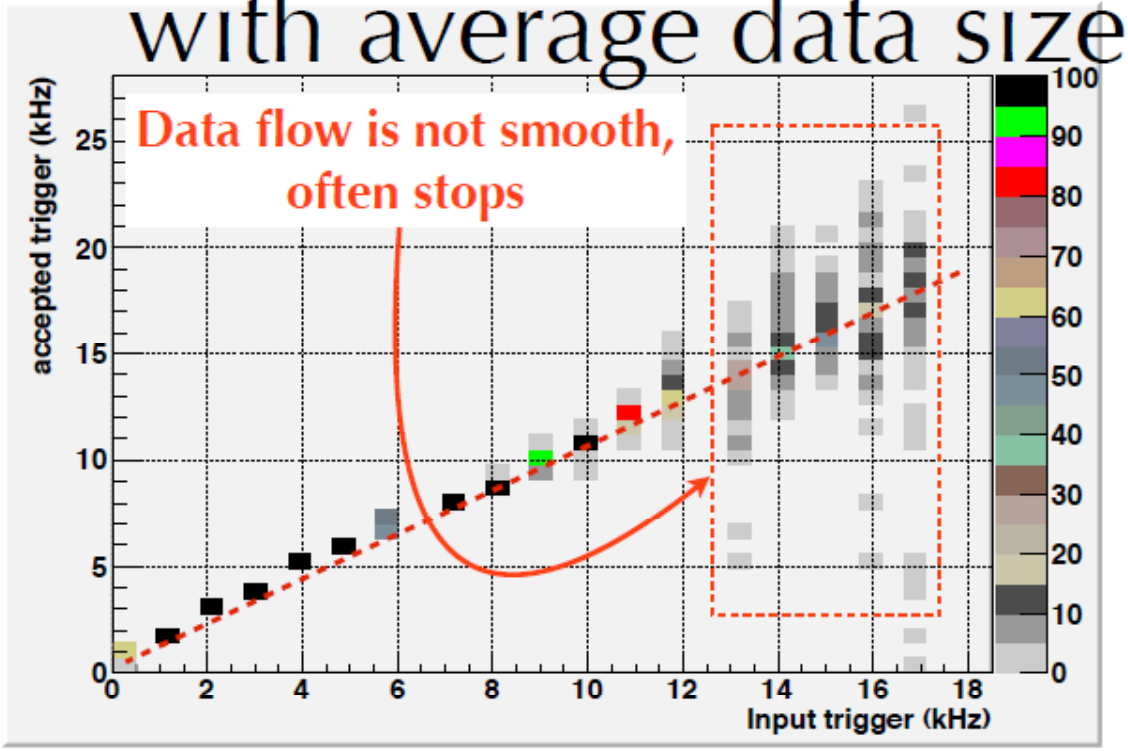
Belle2Link – Z.Liu and M.Nakao

- **VHDL vs Verilog**
  - (I think) **VHDL is more popular than Verilog in Belle II community, but CDC firmware is written in Verilog**
  - **Therefore(?), current CDC firmware is written in mixed VHDL & Verilog, with the top level written in Verilog**
  - (I think) **it's better to provide the top level example in both**
- **ISE version**
  - **Initially, Beelle2link was developed with ISE11.3** (outdated)
  - **Moving around versions is not always trivial**
  - (I think) **Belle2link should be supported on stable (12.4) and latest (13.3 for now) versions**

Question/suggestion about choices of HDL language and ISE version were raised.
Need people's agreement.

Event Builder – S.Y.Suzuki

Maximum trigger rate with average data size



- fully event data size is 50kB (1280byte per sender)
- 6 threads for receiver + 1 thread for event building
- Maximum throughput is about 50kB * 14kHz => 800MB/s
- **over 12 - 13kHz is danger zone**

Critical L1 rate
(L1>12kHz)
for EB layer #1.

HLT→PXD – T.Higuchi

- PXD data size will be reduced with HTL's help.
- Outbound packet format for HLT→ATCA communication is proposed.

Even 200 tracks / ev

- The performance study with prototype implementation (even with a UD socket) shows much better performance than the requirement.
- CPU resource (quad core Intel Xeon 3.16GHz) is not exhausted up.
- DATCON system is also under investigation.

Data Flow – R.Itoh

Requirements

- 30 kHz L1 rate for $L=8\times10^{35}cm^{-2}sec^{-1}$ (Max. ave. rate),
- Event size : ~1MB from PXD, ~100kB from other detectors.
  -> Real-time reduction of this data stream is a challenging task of Belle II DAQ data flow.

Design concept

1. No "software" boundary between DAQ and offline
   - HLT uses the same reconstruction software used in o
     and the "physics event selection" is used as software
   - The software for data reduction and monitoring are su
     to be developed in offline environment and is ported in DAQ
     w/o any modifications.

2. Multi-level data reduction
   - Having CPUs at every step of DAQ to perform the data reduction step by step.

How to ensure library coherence btw offline and online?

* A common data processing framework shared with offline
* Unified data flow based on the framework
* ROOT based data management

Data Flow – R.Itoh

Performance

Data size : 32 words

1. Raw Data Generator only on COPPER : 30.2 kHz
2. Full data flow. Rate measured on R/O PC : 5.1 kHz
   -> Veeerrrrry SIIIIlowwwww even though full CPU consumption
   <- Previous measurement by Higuchi-san using simple algorithm on EPC6315
   > 30kHz transfer rate with ~160 bytes event size.

Possible reasons of slowness:

a) ROOT streaming performance	<- as is expected.....
b) DataStore access	<- Object management on basf2 may cost some
c) basf2 itself	<- basf2 is still not optimized
d) Data transfer over socket	<- Extra CPU cost?

3. Remove socket data transfer : 7.8kHz
4. Replace DataStore access with direct passing : 12.4kHz
5. + Remove ROOT streaming : 25.5 kHz

I'm happy that my old result is somewhat reconfirmed...

=> Re-design of RawCOPPER class

HLT – S.Lee and R.Itoh

Current Status

- Previous (partial) working version
  - Management System
    - ☑ XML parsing works well
    - ☑ Node information reconstruction @ manager node works well
    - ☑ Node information distribution over network works well
    - ☑ Node information reconstruction @ process node works well
    - ☐ Node information serialization using EvtMessage is required
  - Data Flow over Network
    - ☑ Data serialization using EvtMessage works well
    - ☑ Data transfer over network looks working
    - ☑ Separated data handling looks working (but need further improvement)
    - ☐ Data reconstruction is not clearly confirmed
    - ☐ Multiprocess handling is problematic
    - ☐ Process termination is incomplete
    - ☐ EM node implementation is not done
    - ☐ Persistent connection of B2Socket is required

No crash after 1,000 events.

Schedule: The system will be ready by the end of 2012 (R.Itoh).

DQM – R.Itoh

- **Express Reco for PXD DQM**

  - Express Reco reads the recorded data in the storage and a full tracking using PXD + CDC + SVD is supposed to be performed utllizing the HLT processing results to generate PXD-DQM.

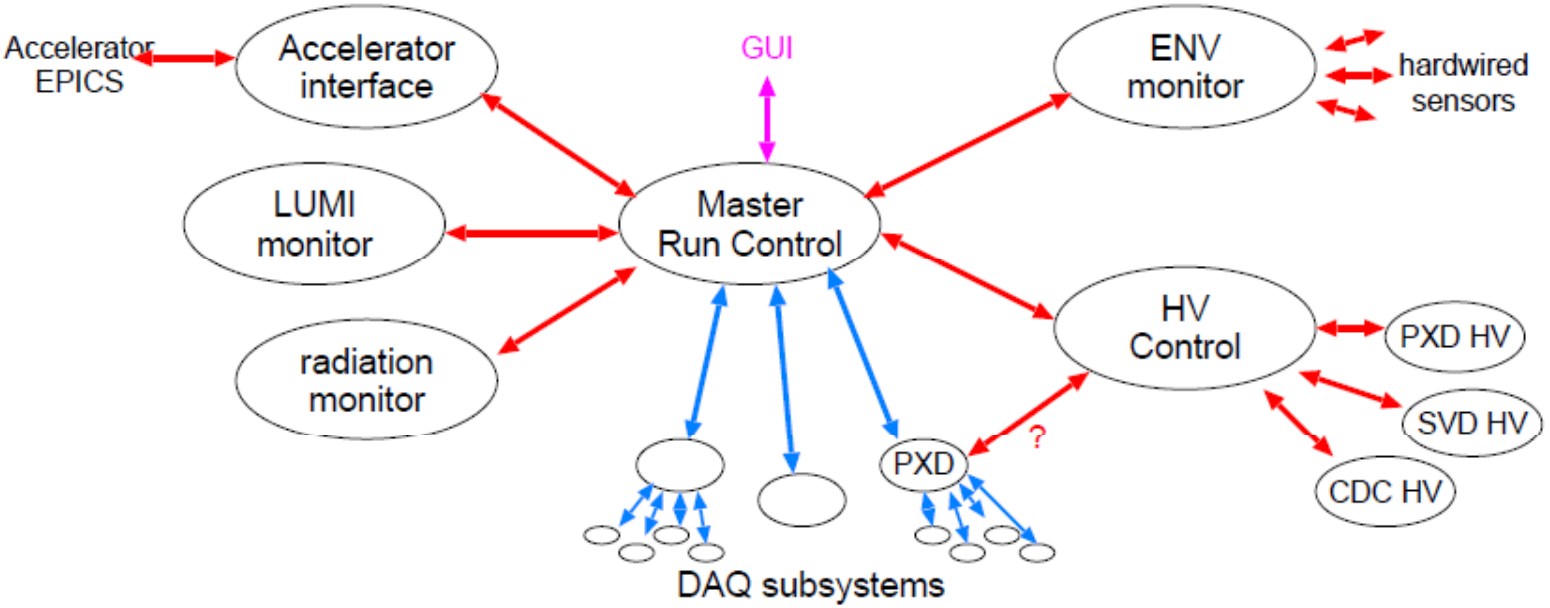
- **Automated data-quality monitoring?**

  - Any automated method to compare live histograms with references and to find the problem?
    * LHC experiments should have some experience, but I don't know the detail (there were some presentations in CHEP2010, I remember).
    * I need help especially on this!
      -> "DQM Task Force Issue!!!!"

Histograms of the last-few-minute data will be necessary.

Slow Control – M.Nakao

Control tree



State model

States will be simplified from the Belle case.
No OFFLINE/ONLINE/PAUSE anymore.

PVSS – S.Sommer

Slow Control for the Pixel Vertex Detector

- Application of the design rules to the PXD Slow Control:
  - Creation of a homogeneous and scalable infrastructure for slow and probably run control
  - Integrated status monitoring and fault detection
  - Plug&Play support to integrate new or evolving software and hardware components
  - Security layer to support save off-site access to experiments and data
  - Tailoring and deployment of the whole system within a tight time schedule

➔ A new solution satisfying all requirements can not be developed within reasonable time and budget

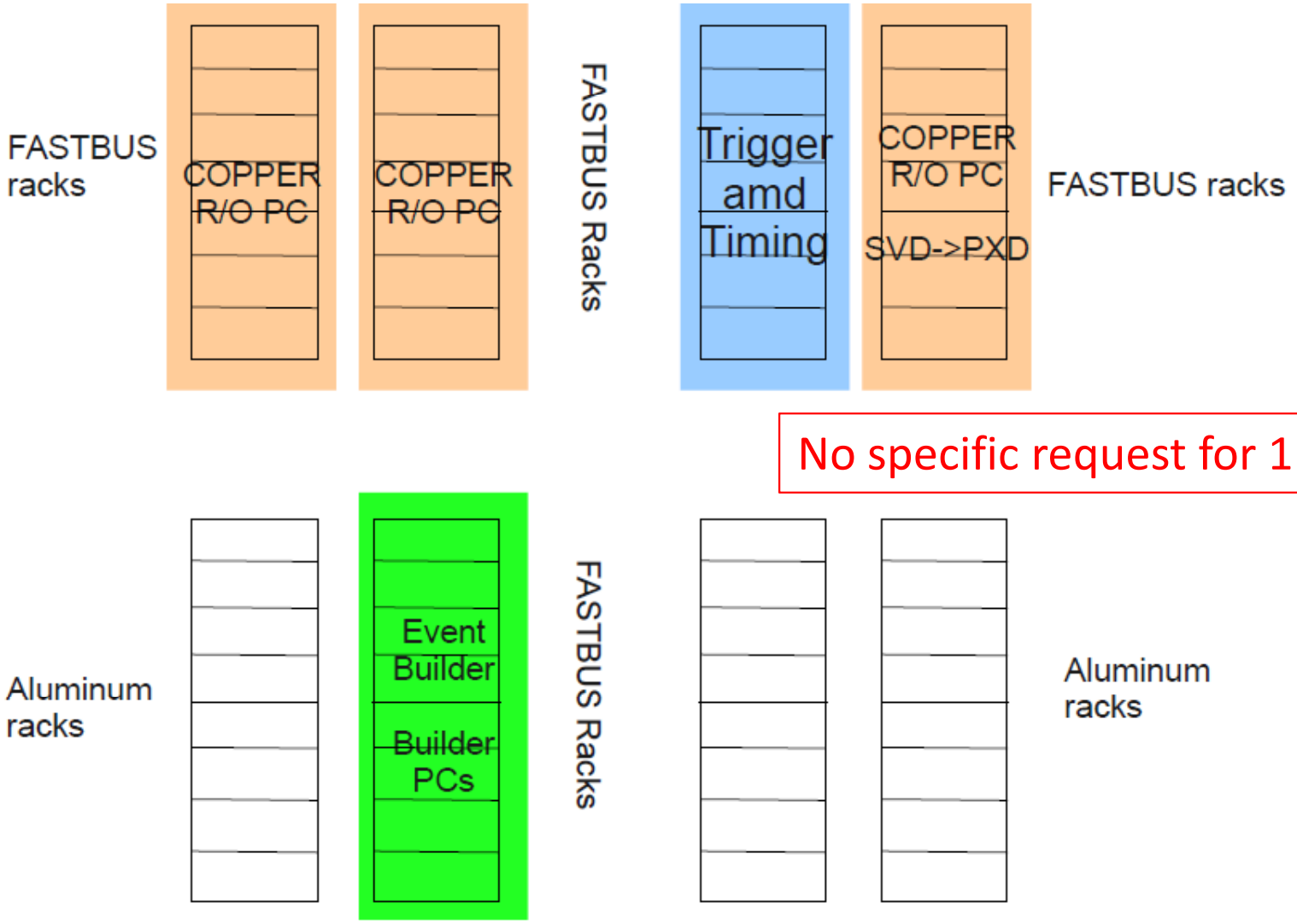
➔ An of the shelf product needs to be found which can be used as basis and provides sufficient options for extension

- Result of market analysis:
  - PVSS II (now WinCC Open Architecture) provides the necessary basic infrastructure and programming interfaces
  - PVSS II needs to be integrated anyway because it is used for the cooling

Internal slow control of the PXD will be based on the PVSS.

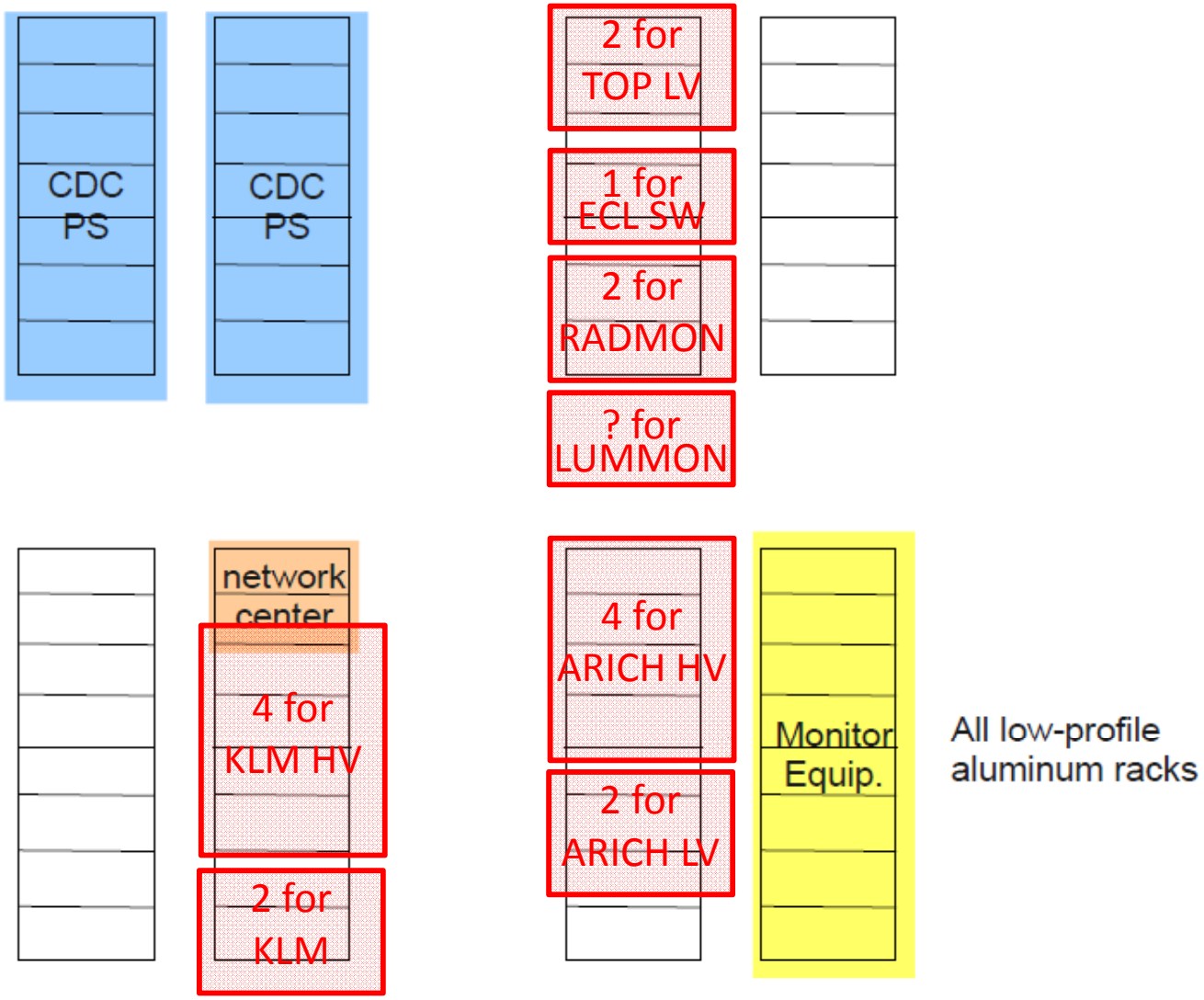
Layout in EH and Around – R.Itoh + All

1F: 0th version layout + requests raised during the workshop (Jan.18,2012)



Layout in EH and Around – R.Itoh + All

2F: 0th version layout + requests raised during the workshop (Jan.18,2012)



Layout in EH and Around – R.Itoh + All