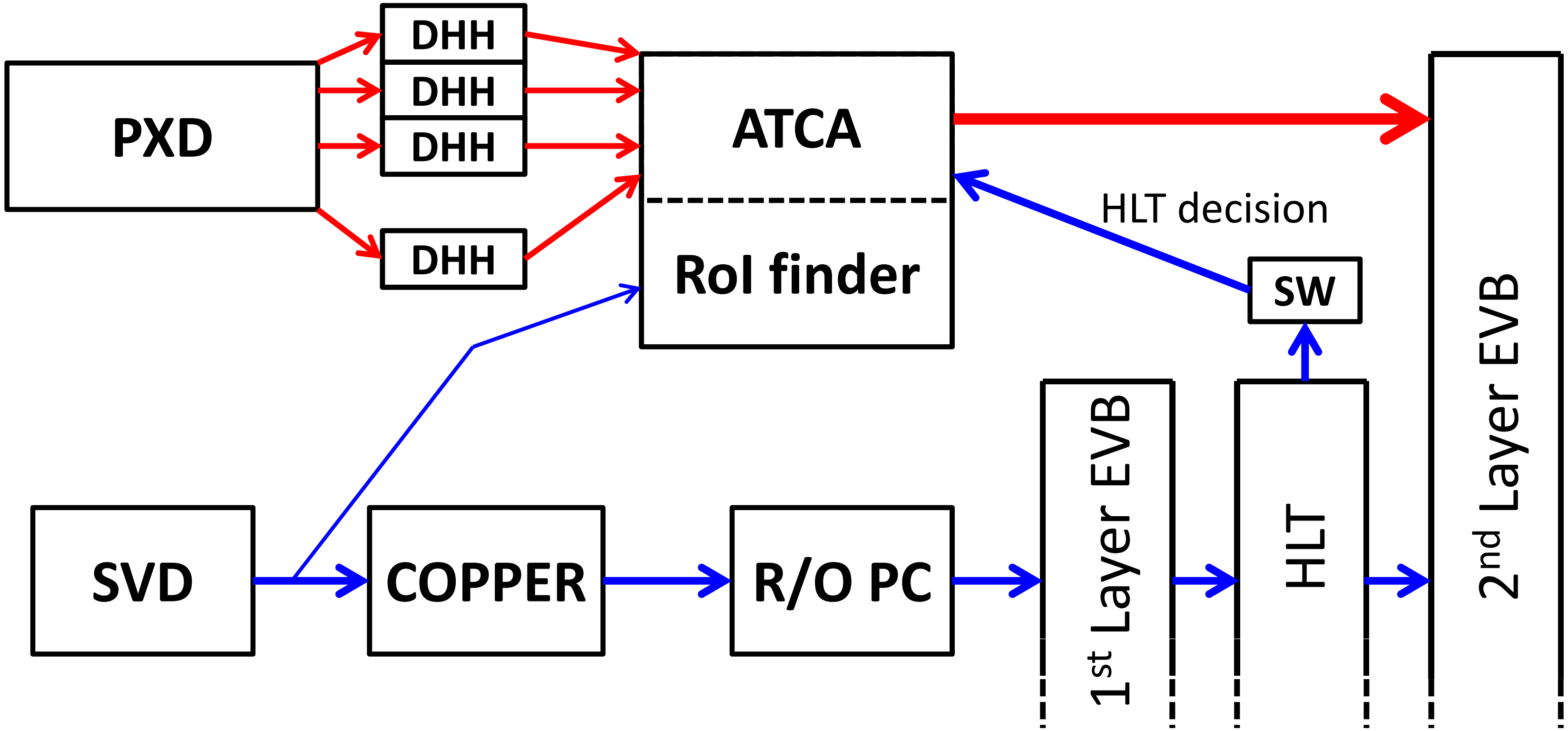
PXD DAQ Integration

Takeo Higuchi (KEK)

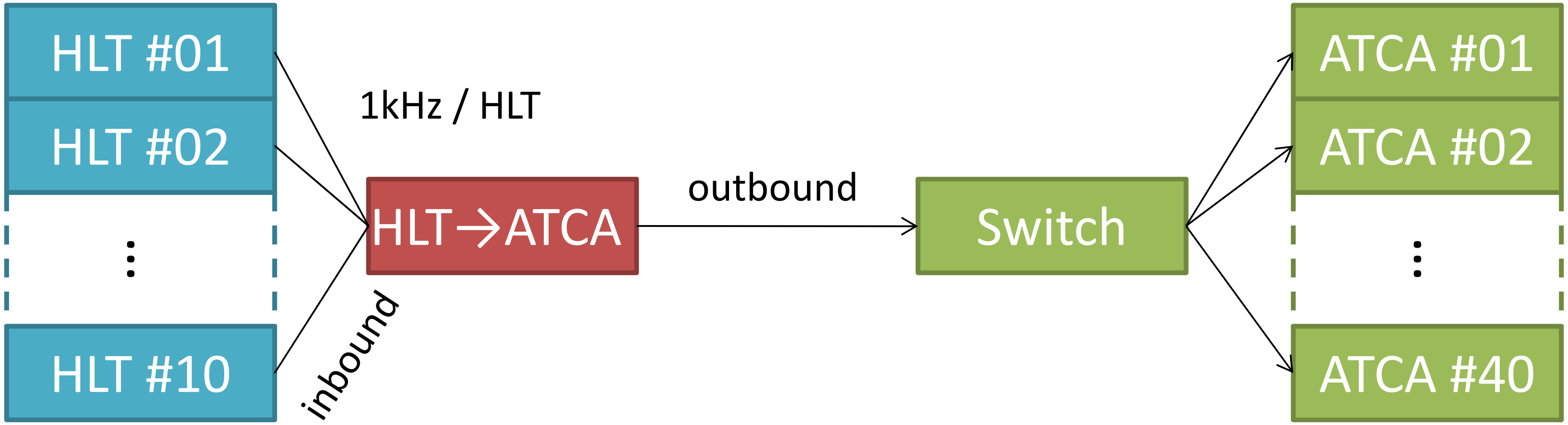
PXD Data Size Reduction



PXD Data Size Reduction

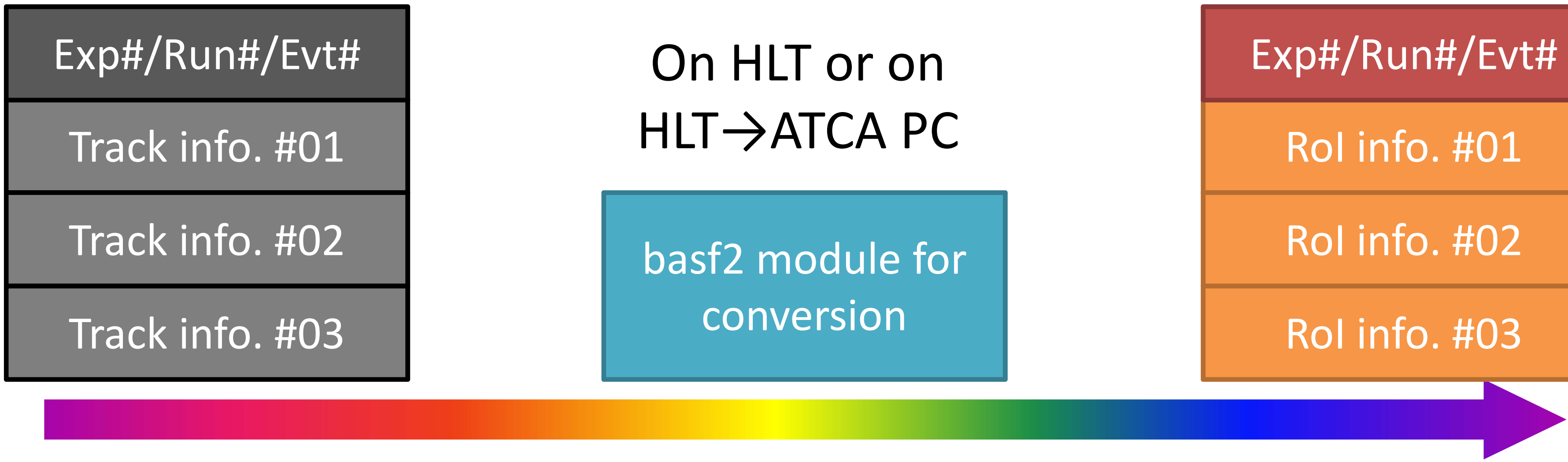
- **PXD data size will be reduced using HLT information and HLT-detected track information.**
  - HLT-silent case → All PXD data are discarded and just "event frame" is sent from the ATCA to the event builder.
  - HLT-fired case → PXD hit signals only associated to tracks found in the HLT (using SVD and PXD) are picked up by the ATCA firmware and after event-record formatting, they are sent to the event builder.

0^{th} Version Sketch (Hardware Link)



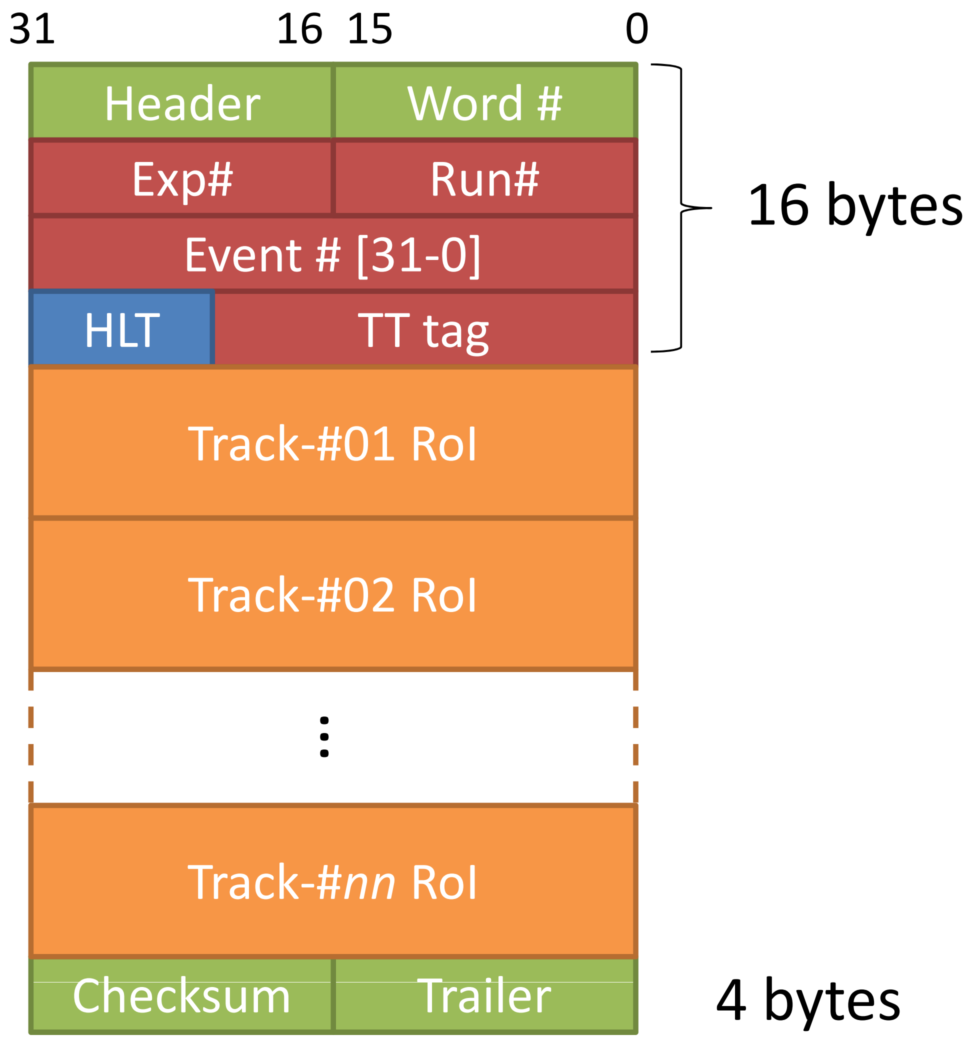
- **Boundary conditions**
  - PXD: (40 half-ladders) x (768 rows) x (250 cols)
  - HLT reduction factor ~ 30kHz → 10kHz (latest assumption). *As of Nov.21,2011*
  - Track multiplicity ~200 (worst case, according to Heck-san).
  - Links of ATCA to half ladder is assumed static at least for the beginning (according to Lange-san).

0th Version Sketch (Software Link)



- **Conversion software**
  - The conversion software runs on HLT PC or HLT→ATCA PC.
  - Would be implemented as a basf2 module.

0^{th} Version of RoI-Info Structure



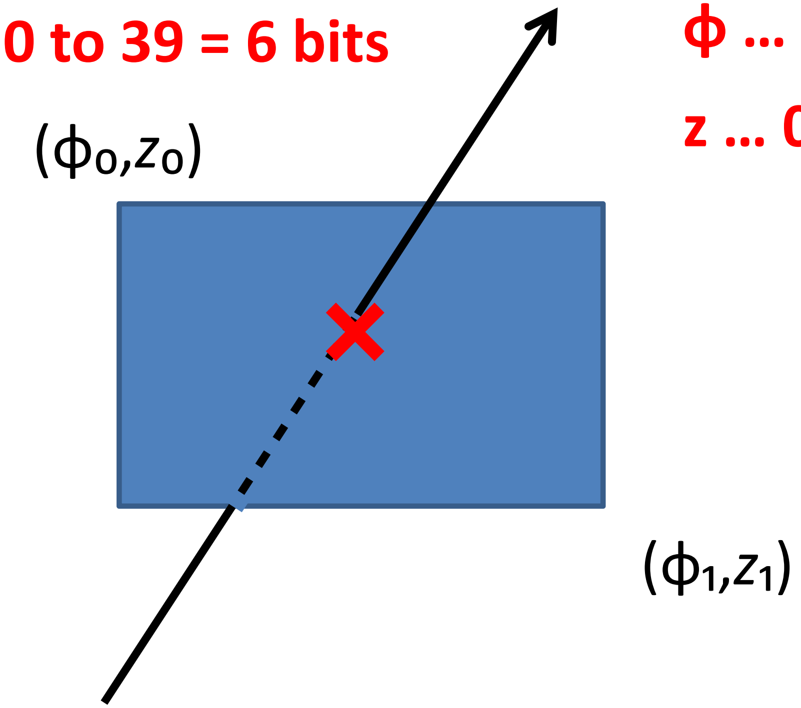
RoI

- **RoI is a rectangular shape.**
  - Size of each RoI would depend on the helix error matrix.

Half ladder ID … 0 to 39 = 6 bits

ϕ … 0 to 249 = 8 bits

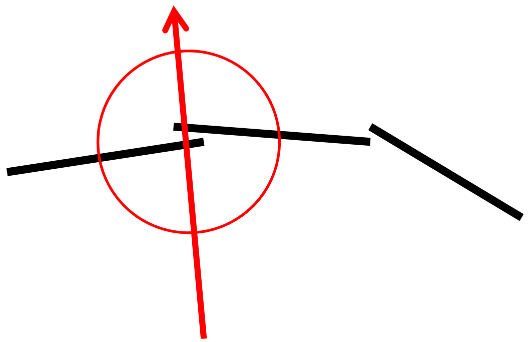
z … 0 to 767 = 10 bits



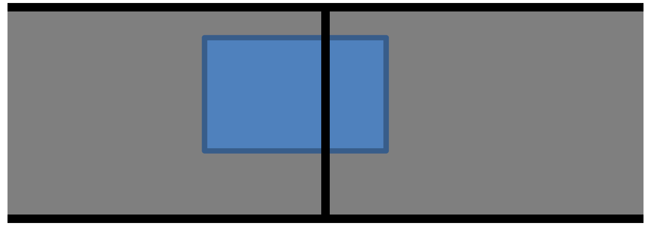
6 + 2x(8+10) = 42 bits → 64 bit (48 bit possible?)

RoI Across Ladders

- **Case (A)**



- **Case (B)**

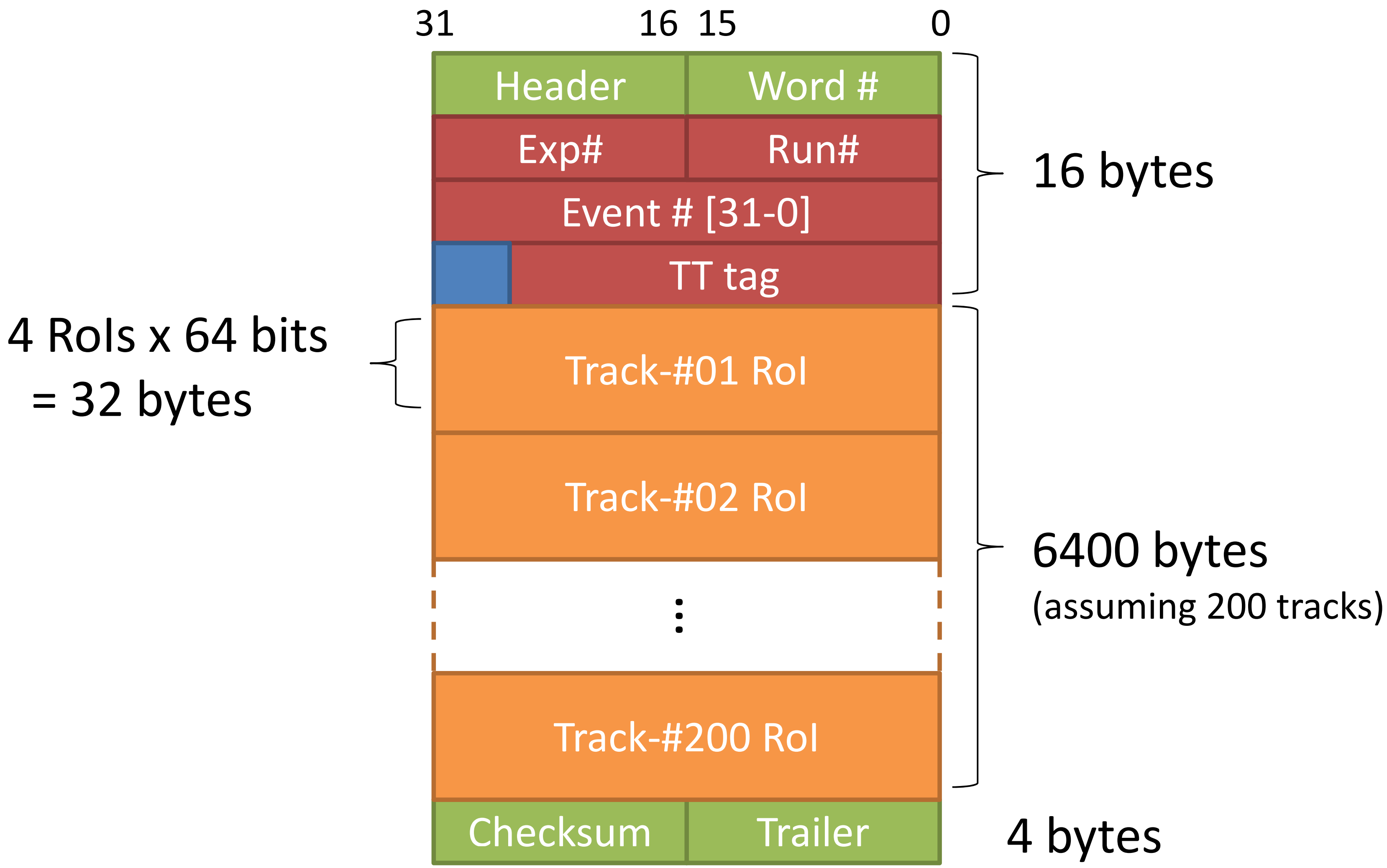


- **Case (C)**
  - Combination of (A) + (B).

Need to survey for the fraction of the across-ladder RoI. But let's say, conservatively, all tracks have 4 associated RoIs.

NOTE: every track has at least 2 associated PXD RoIs (layer-1 and layer-2).

0^{th} Version of Outbound Packet

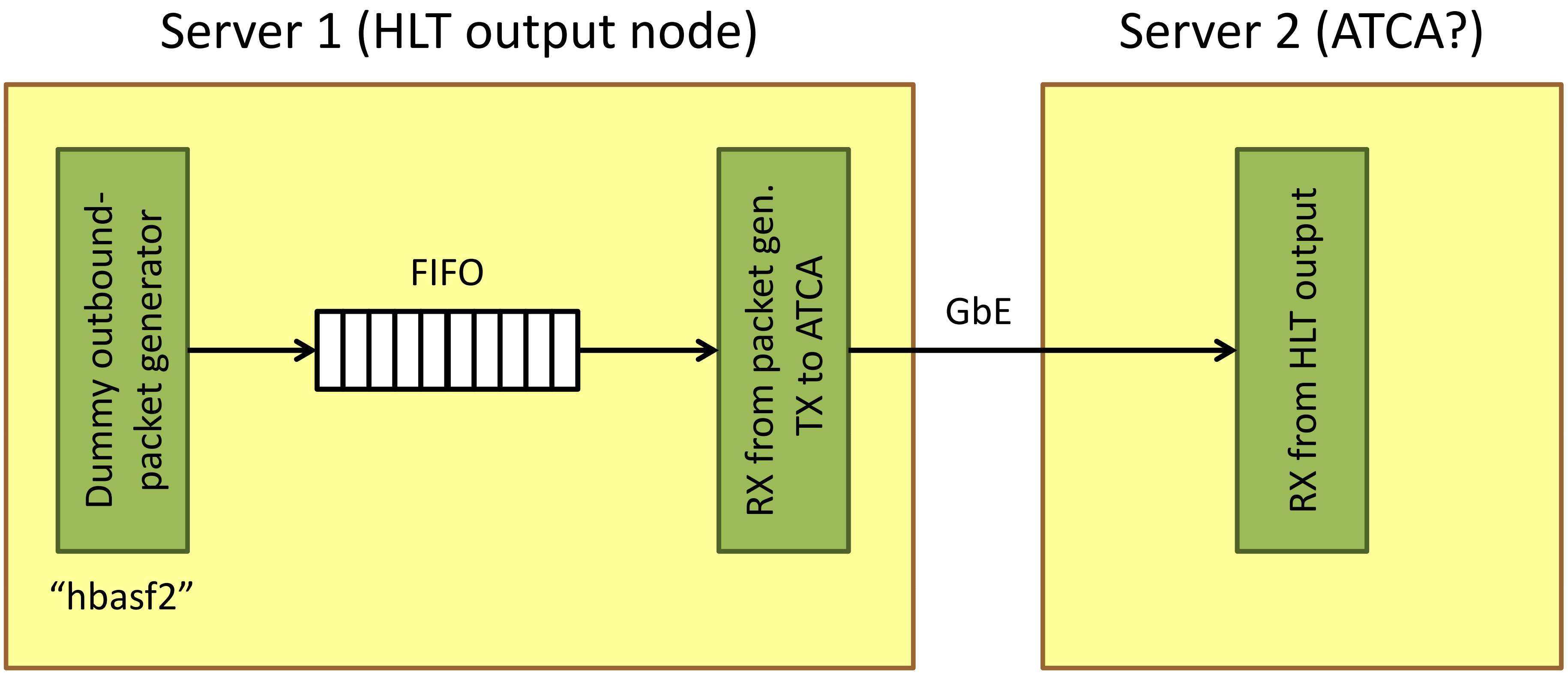


Expected Outbound Throughput

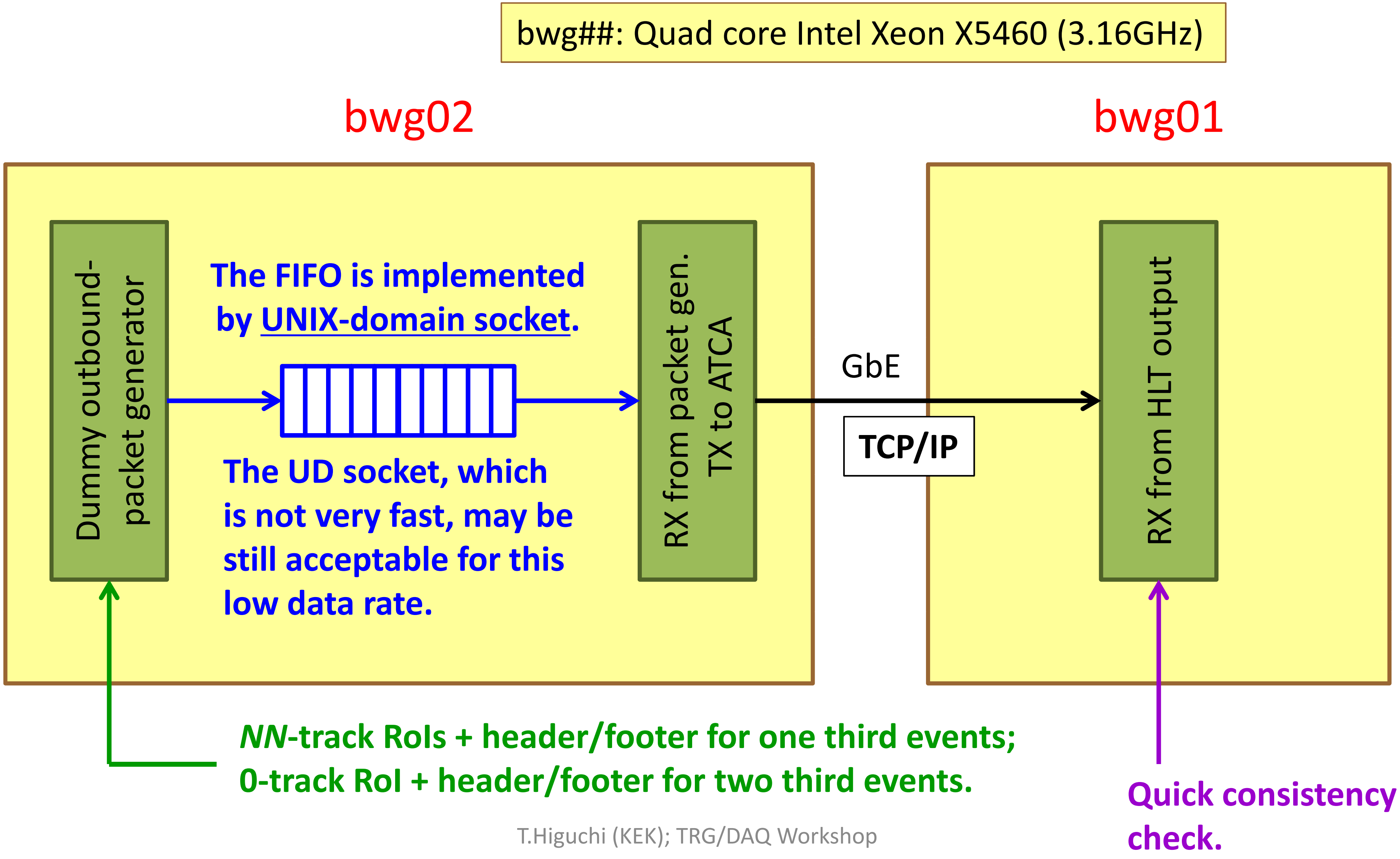
- **Packet size**
  - HLT-fired case
    20 (header+trailer) + 6400 (200xRoIs) bytes → 6420 bytes.
  - HLT-silent case
    20 (header+trailer) bytes.

- **Expected throughput**
  - $\underbrace{\text{10kHz x 6420 bytes}}_{\textit{HLT-fired}}$ + $\underbrace{\text{20kHz x 20 bytes}}_{\textit{HLT-silent}}$ = 61.6MB.

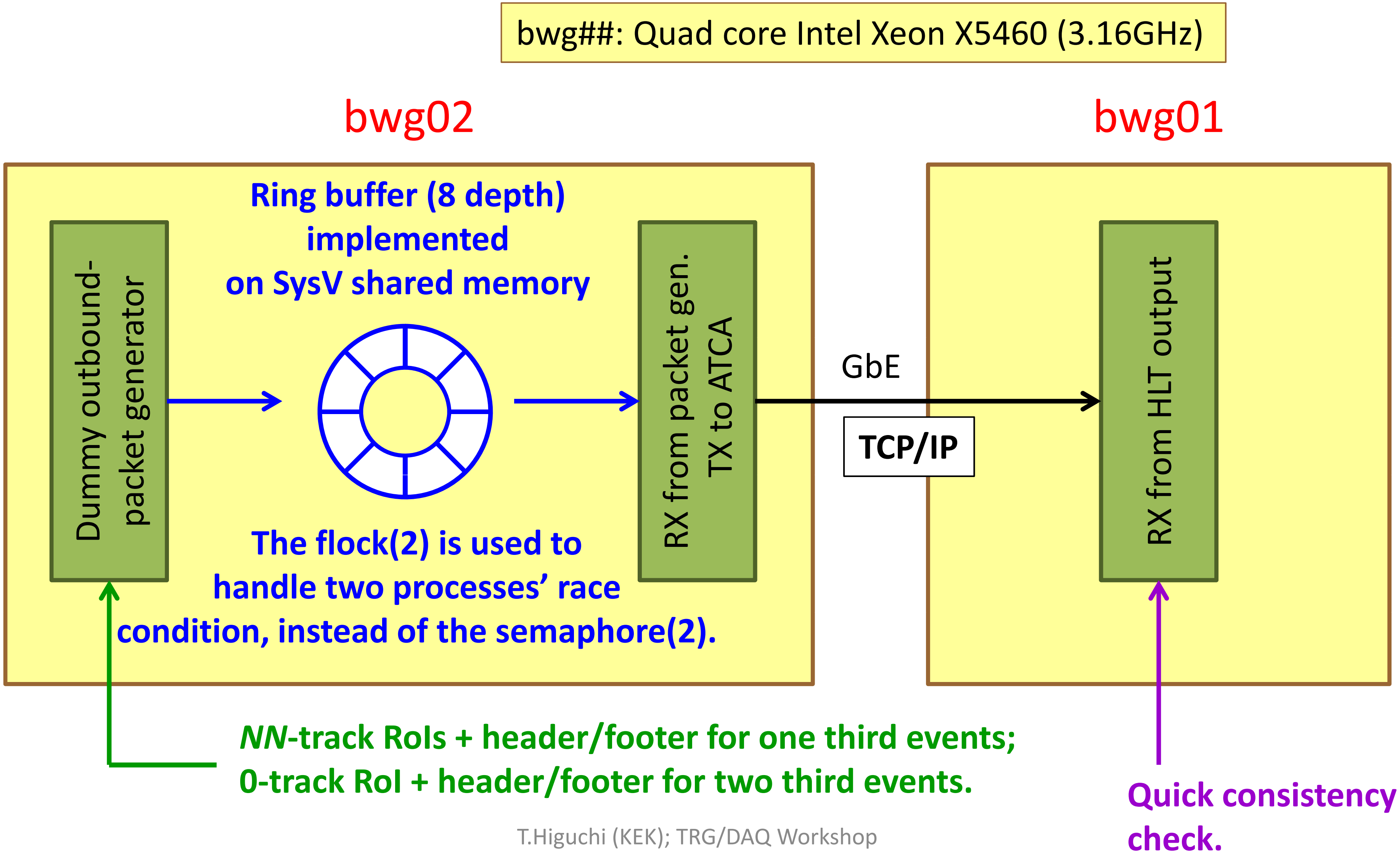
Implementation Proposal



Prototype Implementation [1]

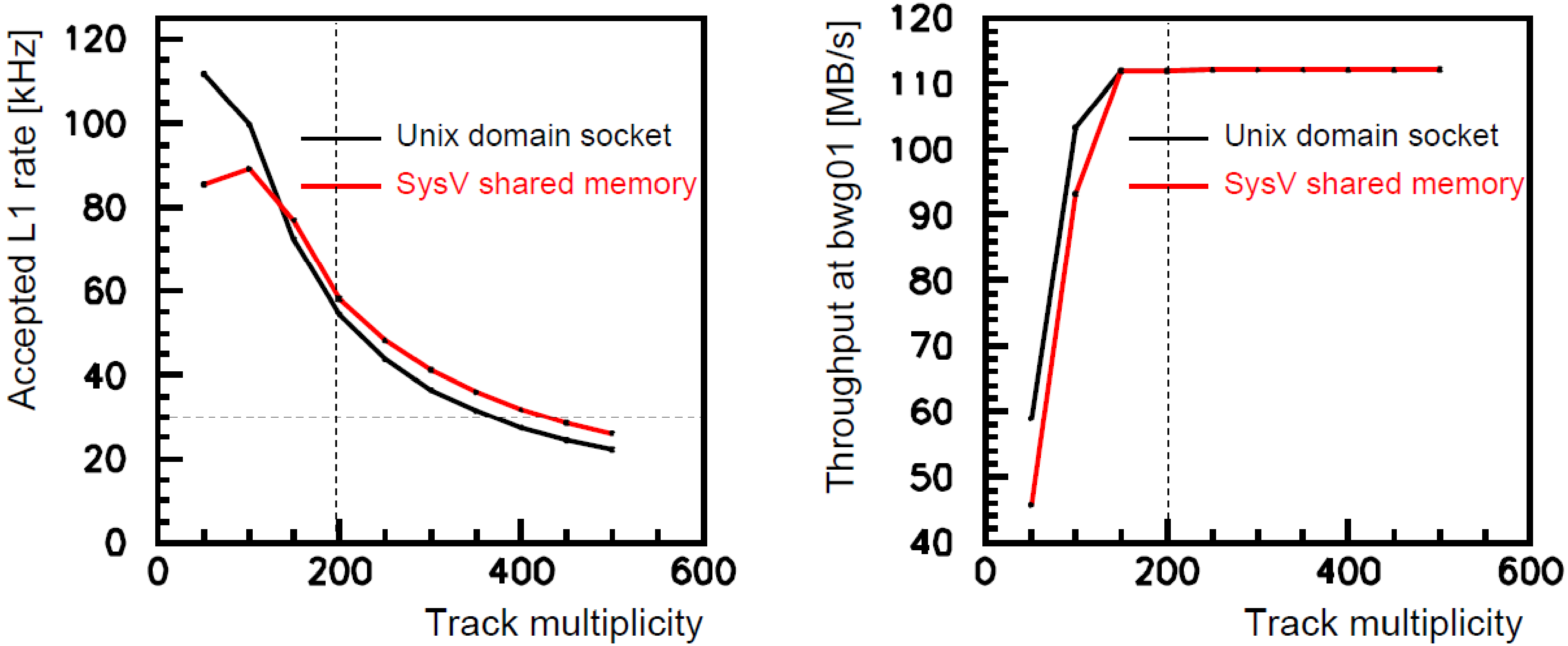


Prototype Implementation [2]



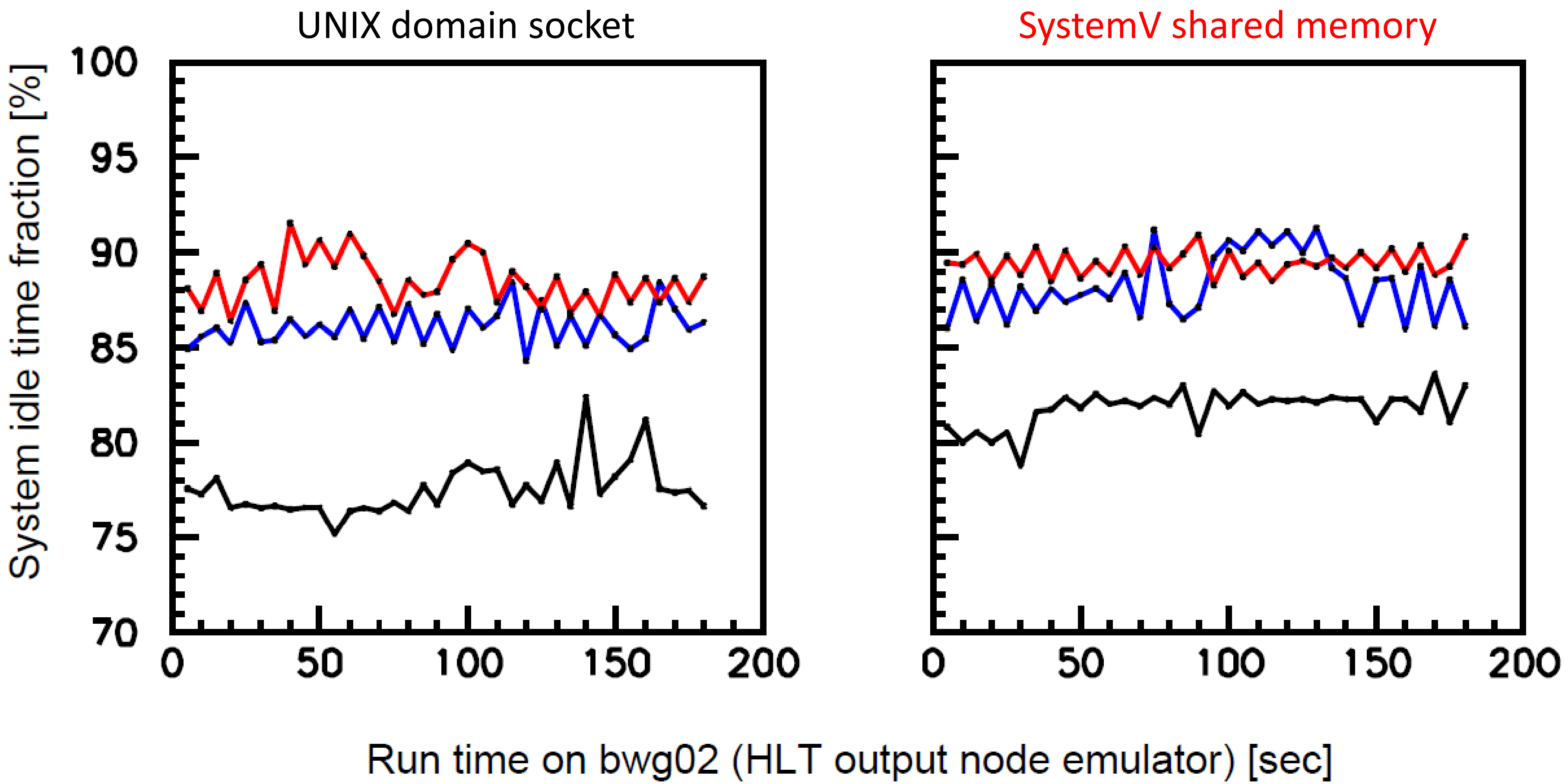
Throughput Measured at RX Node

Performance study at the maximum-speed data output



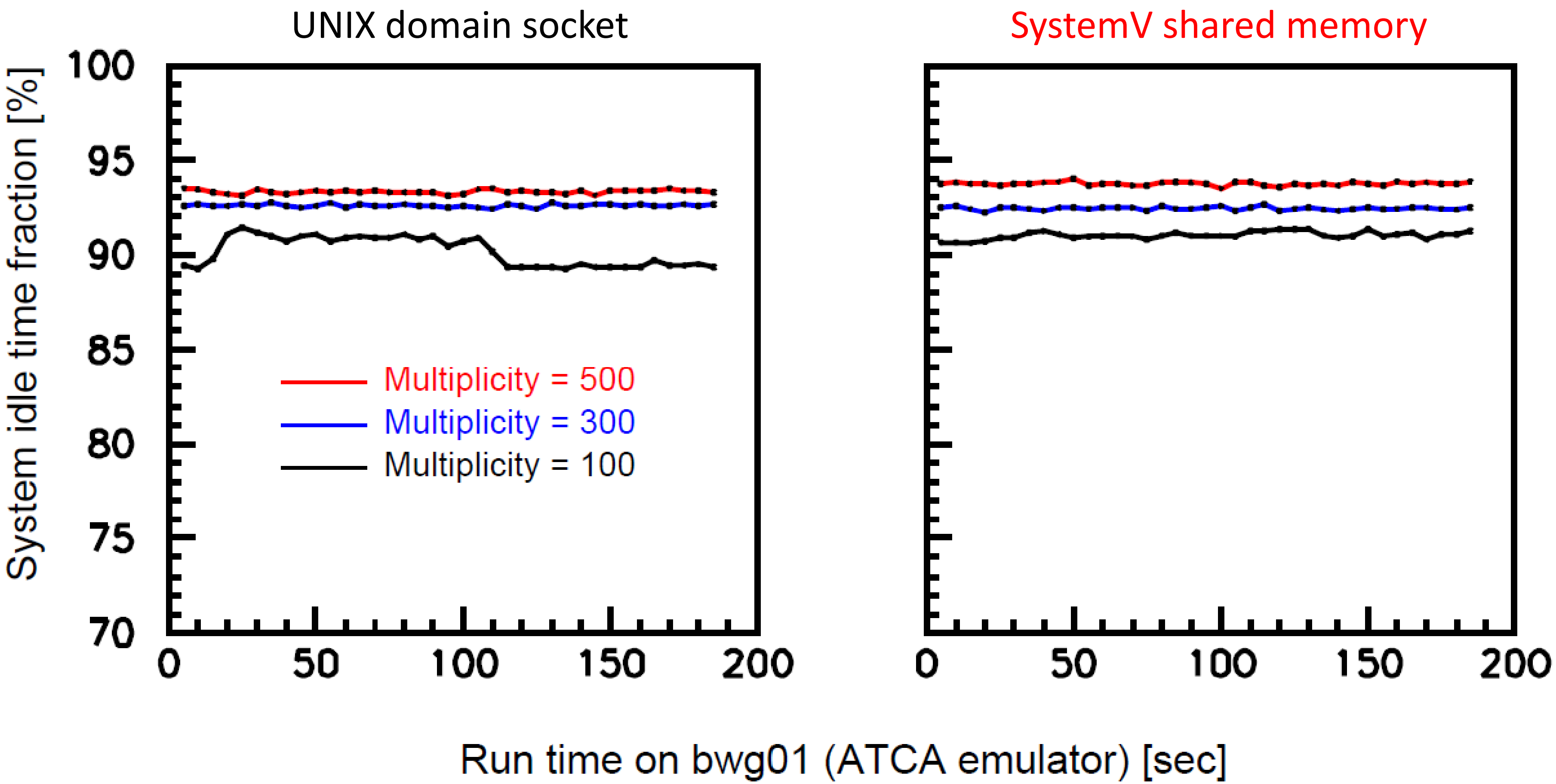
Even with the UNIX domain socket implementation (simpler implementation), the observed performance is well beyond the requirement.

CPU Idle Time Fraction at TX Node



CPU resource of the TX node is not exhausted up.

CPU Idle Time Fraction at RX Node



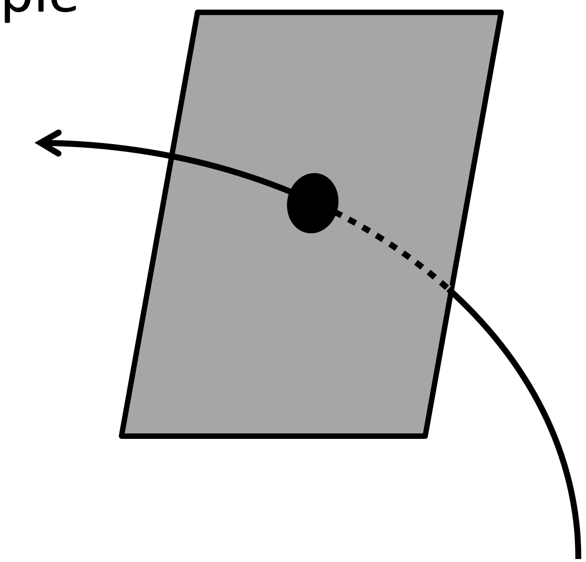
CPU resource of the RX node is not exhausted up, as well.

Memorandum

- **I also studied with a named pipe in stead of the UD socket as the FIFO inside the HLT node. Performance with the named pipe is measured worse than UD socket. No reason to take a named-pipe option at all.**

What's Next

- **Conversion from track position and error to RoI (with a help from PXD group)**
  - Baseline: geometrical calculation
  - Second baseline: optimization of the best size? How do we convert the size from the helix error matrix?
  - Advanced (?): how to take the multiple scattering effect into account?



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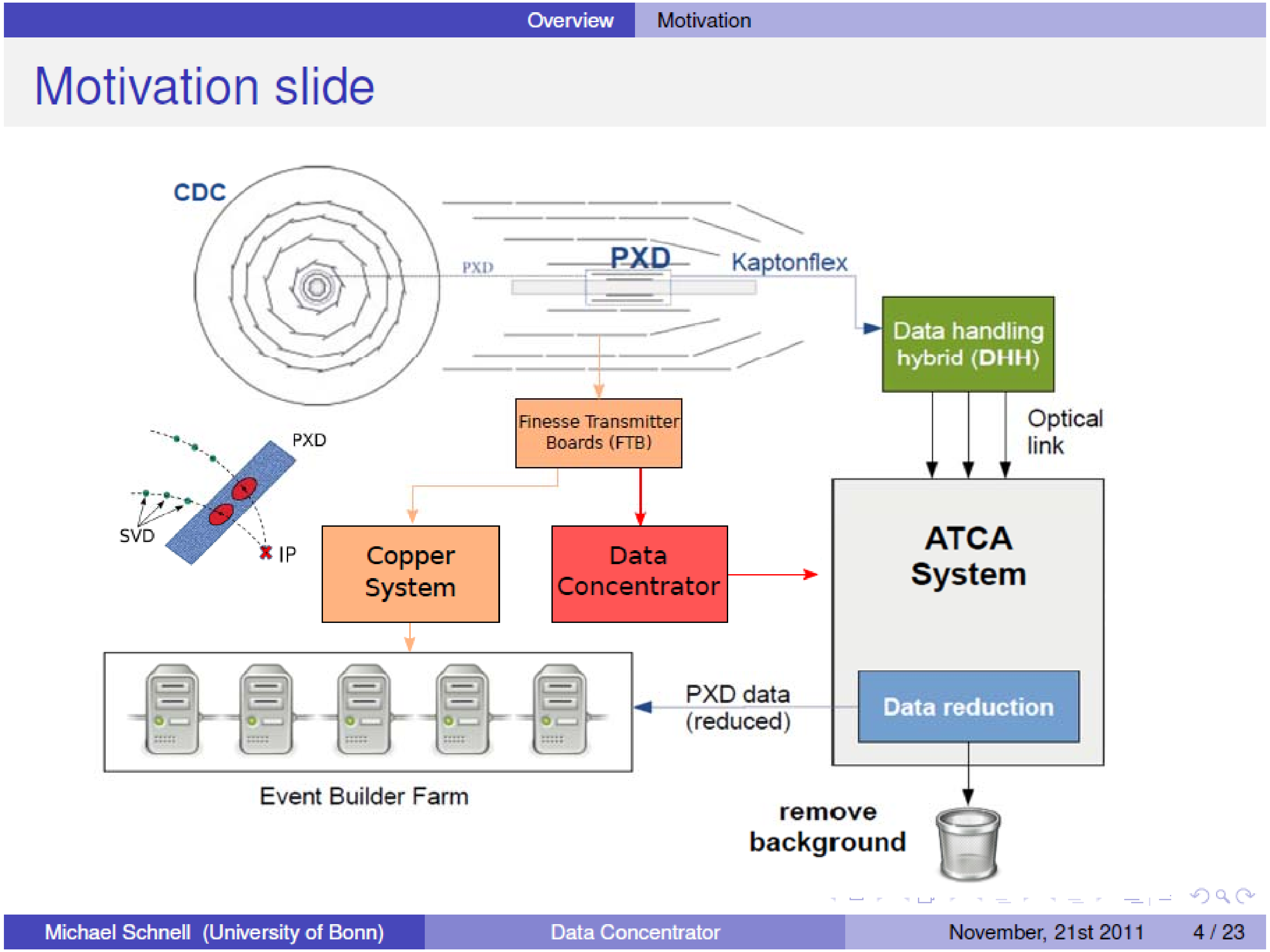
DATCON [0]

- **"DATCON" is another technique to reduce PXD data size under hard investigation by Bonn team.**
- **The DATCON system will be implemented as ATCA module.**
- **The DATCON modules receive digitized SVD signals branched from the main data stream and performs RoI finding on the PXD by SVD-only tracking in its firmware.**

Michael Schell, Jochen Dingfelder, and Carlos Mariñas (Bonn)

DATCON [1]



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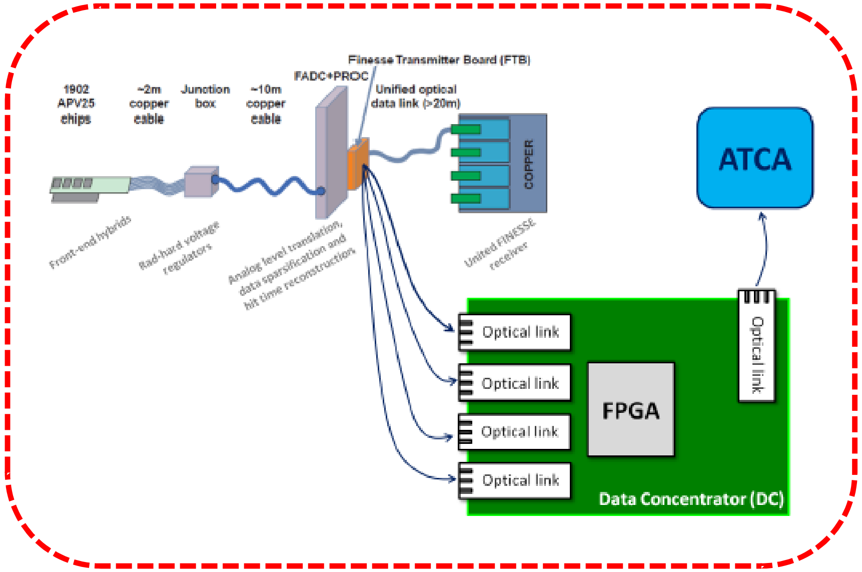
DATCON [2]

Technical specification for the Input cards

- Input:
  - 42 links tops
  - 1.5 Gbps max
  - On average 110 Mbps expected
  - Dynamic bandwidth
- Output:
  - 6.25 Gbps over backplane or SFP+
  - 440 Mbps average data rate

Markup by TH



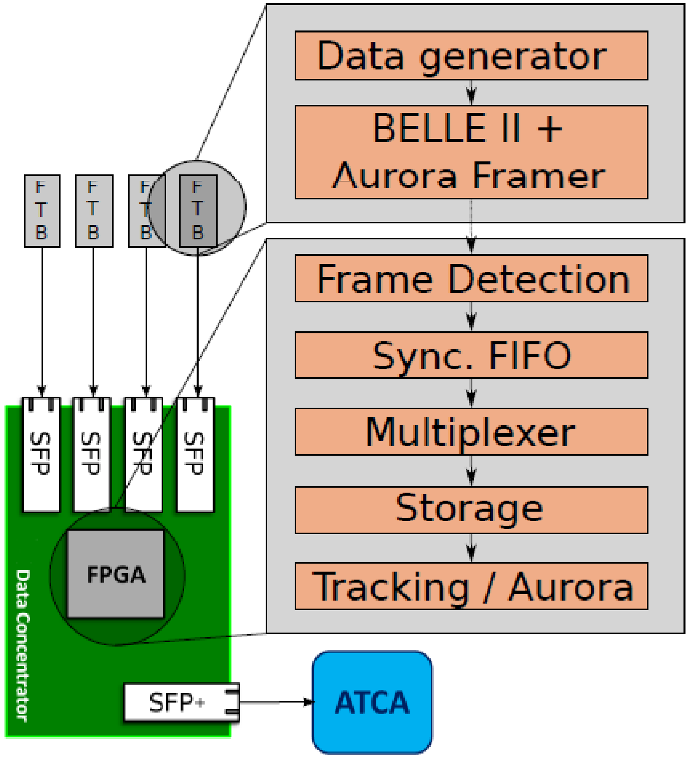
→ Total: 4.6 Gbps ≈ 550 MiB/s

Michael Schell, Jochen Dingfelder, and Carlos Mariñas (Bonn)

DATCON [3]

Overview of the data flow in the prototype

- Physical layer connection over Aurora
- Data link layer over BELLE II Link
- Multiplexer for "concentrating" incoming data streams to one output storage
- Processing of the saved data
- Transmission to ATCA

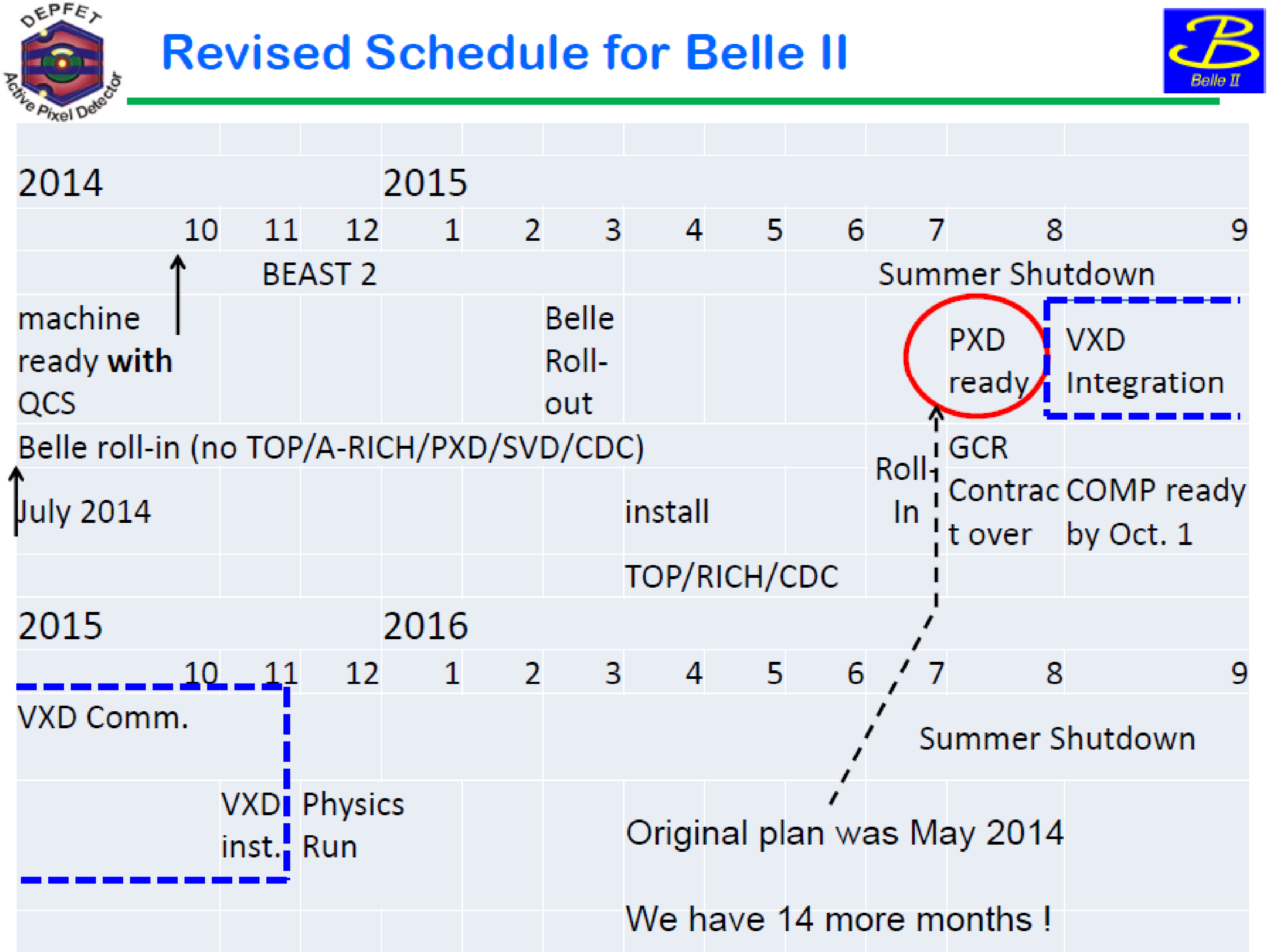


Summary

- PXD data size will be reduced with HTL's help.
- Outbound packet format for HLT→ATCA communication is proposed.
- The performance study with prototype implementation (even with a UD socket) shows much better performance than the requirement.
- CPU resource (quad core Intel Xeon 3.16GHz) is not exhausted up.
- DATCON system is also under investigation.

Christian Kiesling (MPI)

Belle II Grand Schedule



Items Related to Global DAQ

- **PXD+SVD**
  - Readout device installation.
  - Network cabling.
  - Cabling for DATACON.
  - Cabling for HLT→ATCA connection.
  - Cabling and test for TT system.
  - System test for RoI finding.
    - Efficiency, purity, and throughput.
  - Run control and slow control
    - Partial system.
  - DQM

3-6 months?

Items Related to Global DAQ

- **PXD+SVD+…+<u>CDAQ</u>**
  - 2nd level event builder.
  - Network cabling.
  - Run control and slow control
    - Full system.

2-3 months
with a few overlap
with previous page?

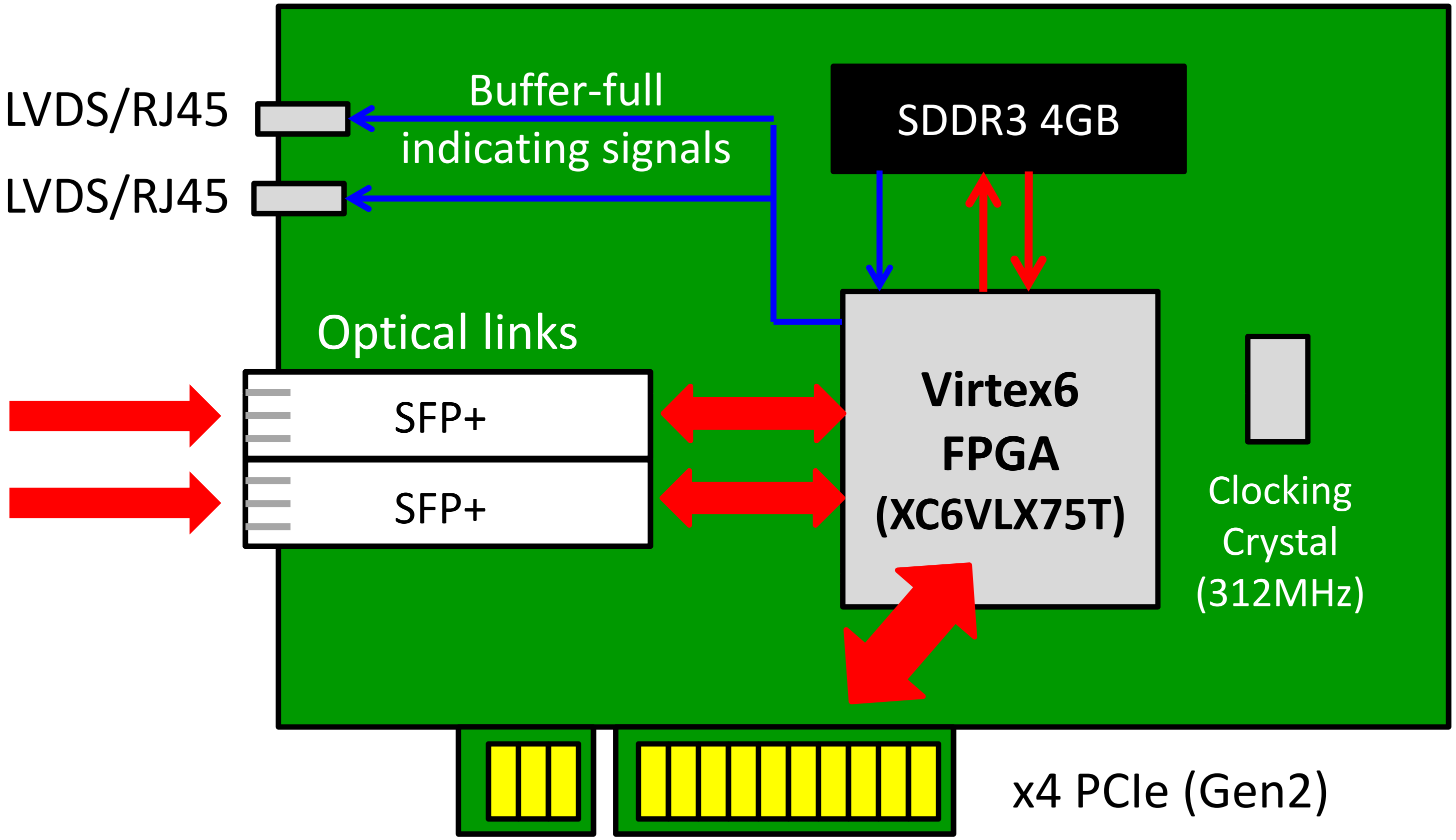
As the schedule is not very relaxed, we should be so careful in placing milestones that we can surely be ready at *t*=0 in 2015.

PCI-Express Option (Backup Solution)

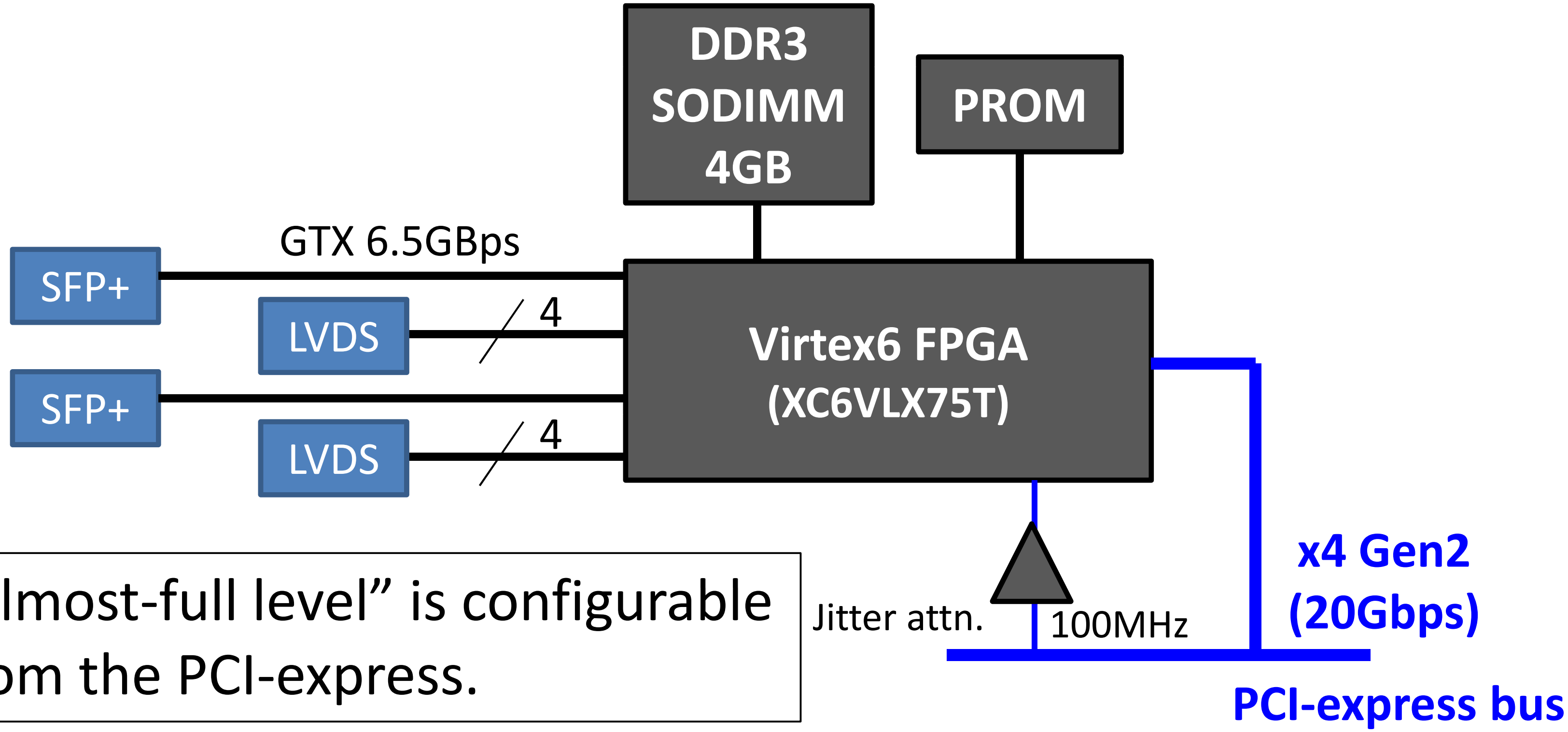
Takeo Higuchi (KEK)

RocketIO→PCI-Express Card

- **Schematic chart**

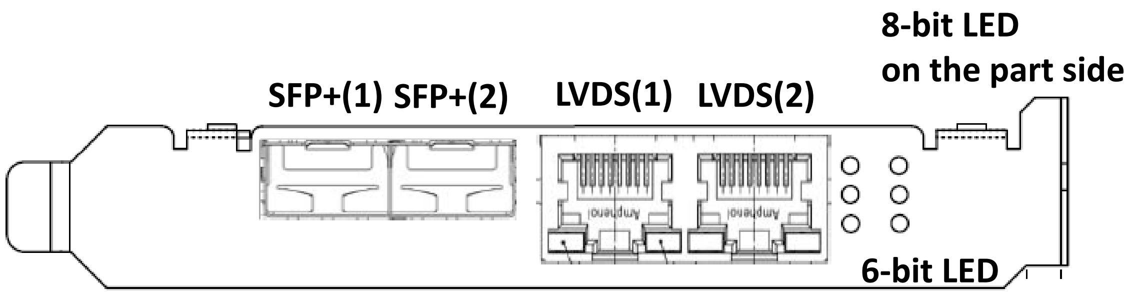


Block Diagram



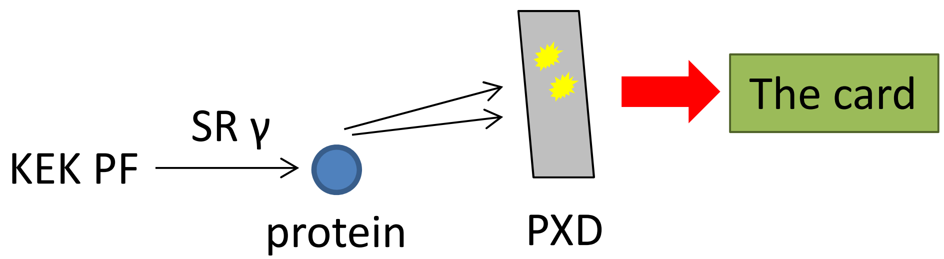
"Almost-full level" is configurable from the PCI-express.

Front panel design



Expected Usages

- Backup solution for the Belle II PXD readout
- Test-data generator to the ATCA system
- Readout of PXD for diffracted SR γ by protein – structural biology (funded study)



Schedule

- **Delivery**
  - We have the two prototype cards in February 2012.
- **Test and usage**
  - We make a dry run test and performance study of the card in March 2012.
  - The first real usage is expected to take place in the KEK PF in the early fiscal year of 2012.