## Missing hits investigation

- Position loss due to corrupt data is still under investigation. This is probably not the main source of the missing hits.
- The special case of hits that span two windows had a problem causing loss of position. This has been fixed in v3.3 candidate.
- Another bug was the check for data corruption related to windowspan cases. Will be fixed in 3.4.
- Fixing both issues, restores the missing hits.

276	+
277	+ for (samp = startSample; samp < startSample+16 && samp < 64; samp += 2) {
278	<pre>+ int16_t loAdc = swapEndian(ch_det_buf_in[pos]) &amp; 0xFFF;</pre>
279	<pre>+ int16_t hiAdc = (swapEndian(ch_det_buf_in[pos]) &gt;&gt; 16) &amp; 0xFFF;</pre>
280	+ if (debug) {sprintf(errmsg, "%d, %d ", loAdc,hiAdc); printfMessage(errmsg);}
281	+ if (pedestal_subtraction_flag != 0) { //Will put back after enabling pedestal subtraction
282	<pre>+ loAdc -= pedestal_val[bs_index+baseIndex+samp];</pre>
283	<pre>+ hiAdc -= pedestal_val[bs_index+baseIndex+samp+1];</pre>
284	+ if(pedestal_val[bs_index+baseIndex+samp]<600    pedestal_val[bs_index+baseIndex+samp+1]<600
	pedestal_val[bs_index+baseIndex+samp]>1500    pedestal_val[bs_index+baseIndex+samp+1]>1500){ //using the same condition as firmware
285	+ hitInfo.integral = 1;
286	+ }
287	+ }
288	<pre>+ // int16_t *samplePtr = (int16_t *) &amp;(ch_det_buf_in[pos]);</pre>
289	+ // samplePtr[0] = loAdc;
290	+ // samplePtr[1] = hiAdc;
291	+ sampleData[samp-startSample] = loAdc;
292	+ sampleData[samp+1-startSample] = hiAdc;
293	<pre>+ if(writeRawHit){FullWaveformsToCopy[CounterFullWaveformsToCopy][2+(samp-startSample)/2] = swapEndian((loAdc &lt;&lt; 16)   hiAdc);}</pre>
294	+ pos++;
295	+ }
296	+

2	if (nSamples != 32 && nSamples != 16) {
3	<pre>nSamplesWrongCounter++;</pre>
k i	if (debug)
5	{
5	<pre>sprintf(errmsg,"ASIC %ld hit %ld incorrec</pre>
7	<pre>sprintf(errmsg,"\thad totHits = %ld, char</pre>
3	
)	
)	totHits -= nHits - iHit;
L	
2	<pre>while (swapEndian(ch_det_buf_in[pos]) != 0&gt;</pre>
3	pos++;
k –	
5	<pre>if (debug) {sprintf(errmsg,"stopped at word</pre>
5	<pre>ProcessPacketProblemCounter++;</pre>
7	//pos++;
3	break; You, 5 months ago • Initial
)	//continue;
)	}

## PCIe40 FE Dead time

- The dead time observed by Harsh is under investigation. Dead time is not distributed near uniformly between TOP boardstacks. We have three candidates main for explanation in terms of likelihood:
  - One or more TOP boardstacks due to bad analogue threshold or some other reason generate too much noise and saturate the connection.
  - Individual channel problems on the PCIe40 board or computer.
  - The shared memory space for the TOP data on PCIe40 is filled and through an unknown mechanism an asymmetric backpressure creates dead time on individual TOP boardstacks.

