# TOP Feature Extraction

## Progress Updates and Plans

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TOP Feature Extraction Group Meeting
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# Project status

- **Recently finished testing 2nd version of TOP Feature Extraction at UH.**
- Successfully tested version 1 at KEK (with 1 TOP FEE, s09a).
- Yet to test version 1 with all TOP FEEs to check if there is any significant impact on performance.
  - Powered up all the TOP FEEs connected to rtop1 this morning.

- Almost finished the script for reading pedestals in parallel from all TOP FEEs.

- **Next steps:**
  - Test version 1 at KEK with full TOP setup
  - Help Shahab test out version 2 at UH
  - Test version 3 at KEK

# TOP Feat Ext – Tests at KEK

Version 1

- No pedestal subtraction
- Single TOP FEE

# Preparations for testing TOP FE at KEK

## (version 1 – no pedestal subtraction)

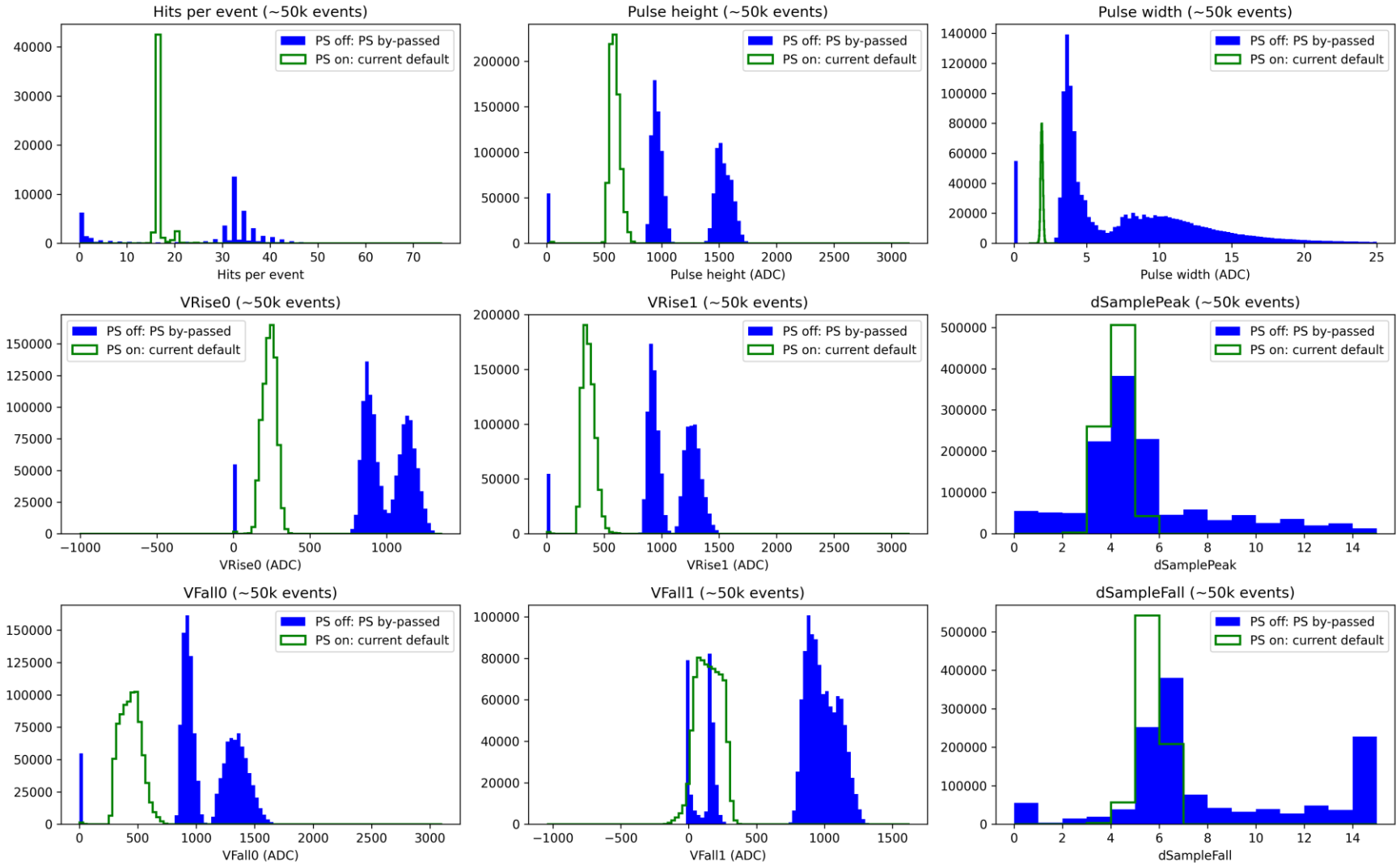
- To not disturb the existing TOP/DAQ setup, for testing TOP FE I made the following changes…
- Minor modifications made in the `pcie40_software` + TOP FE code (v1):
  - Branch: **`top-feature-extraction-kek-v1`**
  - Why?
    - Slightly different RL-9 OS/kernel versions
    - No need to fake the SCROD ID at KEK
    - Have a different IPC socket for testing purposes
- Compiled **`basf2`** on *rtop1* and *rtop2* with minor modification:
  - **`daq/rawdata/modules/src/DeSerializerPC.cc`** – Turn on **`NO_DATA_CHECK`** flag
- Compiled daq_eb (sw event builder) on *rtop1* and *rtop2* with minor modifications:
  - Using IPC socket: **`/tmp/pcie40_roproc_test`** for my tests
  - Similarly, using separate files for eb status/stats
  - Listening port was also modified to 5109

# Testing procedure

1. Power-cycle & Configure TOP BS (one or more at a time) with firmware: **8C-93/84-23**
2. Prepare TTD with:
   ```
   ttaddr -65 –c; ttaddr -65 –a; ttaddr -65 –m
   ttaddr -65 –u pcie40b,s09a
   ```
3. Enable PS-bypass mode: **pcie40_regconfig --ch 0 --fee32 -w 0x4EF 0x1**
4. Start calibration pulser with:
   ```
   ssh topslc01
   ssh pulser bash set5kHz.sh
   ```
5. Start eb0_for_pcie40 with:
   ```
   eb0_for_pcie40 –l 5109 –i 1 –u /dev/shm/eb0_up_test –d /dev/shm/eb0_down_test
   ```
6. Start basf2 for dumping data to file with:
   ```
   basf2 ~/RecvStream1.py –o ~/test.sroot 0 5109 temp
   ```
7. Start DAQ software with: **pcie40_ulreset; sweb_receiver 0x03000002**
8. Start issuing triggers with: **resetft -65; trigft -65 aux 50000**

# Comparison with expected results

## Version 1 – No pedestal subtraction



# More tests planned for later today

Version 1

- All TOP FEEs connected to rtop1/rtop2
- Performance impact with the full setup

# TOP Pedestal data RO

Using sweb_receiver

# Reading pedestal data from TOP FEE

- Power-cycle TOP BS with firmware: *8C-93/82-23*
- Configure it. This reads in new pedestals and saves it to the SCROD memory
- Enable sending pedestal data from SCROD memory to PCIe40 via b2link:

```
pcie40_regconfig --ch ___ --fee32 –w 0x182D 0x4
```

- Prepare PCIe40 to read data with *ID for TOP 0x03000001*

```
sweb_receiver 0x03000001
```

- Start software event builder with,

```
eb0+1tx_for_pcie40 -l 5101 -i 1
```

- Start basf2 to incoming read data from the IPC port (5101)

```
basf2 RecvPeds2Root.py -o testPed.sroot 0 5101 temp
```

- Send FTSW triggers (local): *num trig out > 8192*

```
trigft -13 pulse 2000 8400
```

Combined all these steps into a single bash script

Plan to integrate this in TOP Power-cycle and Config GUI

# New unpacker for pedestal data

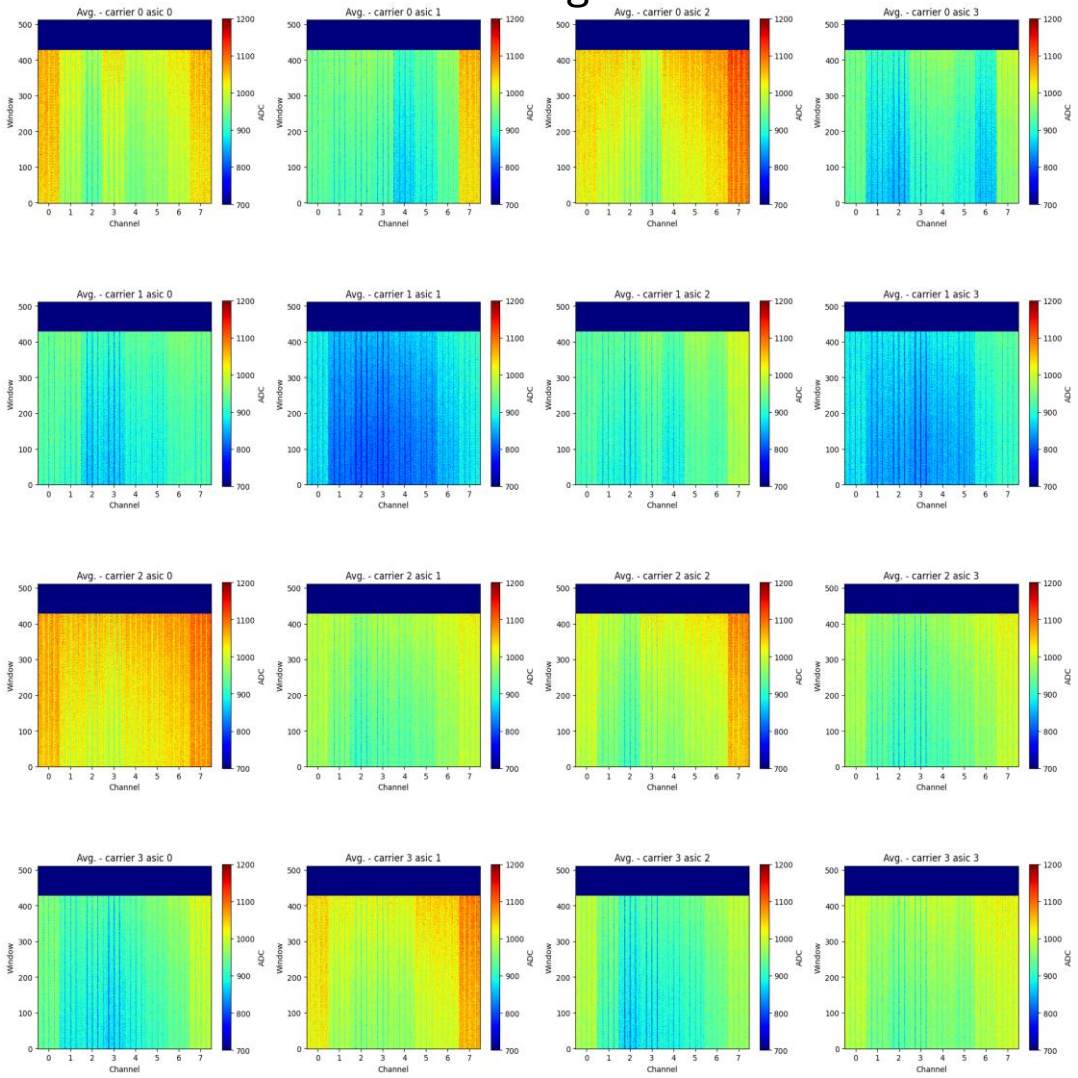
- Previously the pedestal data used to be unpacked with the peddump.c code
- This expects the file has only the B2Link header, footer and pedestal data.
- Don’t know how to remove PCIe40 header/footer from within basf2, so instead **I wrote a small unpacker for pedestal data in python**, works fine.
- Steps (1-3 included in the bash script):
  1. Read pedestals from TOP FEEs and dump them in a root file.
  2. Then convert root to binary file/format.
  3. Run python unpacker to unpack and dump these into a txt & binary file.
  4. Use one of the 2 files to read pedestals and do feature extraction.

- Running with multiple BS have some inconsistent behavior, will try to debug and fix this.
- Also, need to slightly modify the python unpacker to correctly unpack pedestal data from multiple FEEs.

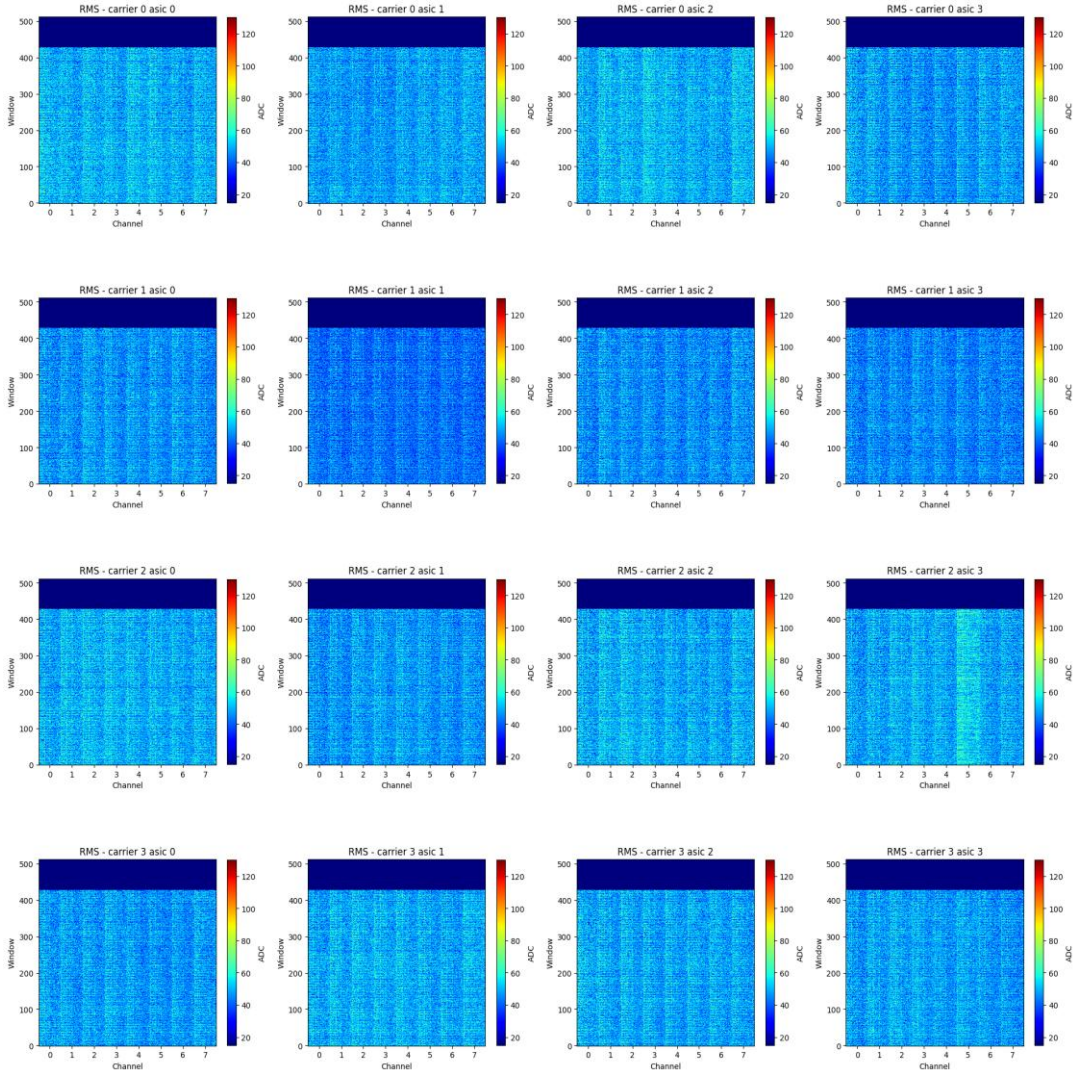
# Pedestal values for BS-3 (UH)

BS-3 → ch 7 → SCORD ID: 7

Average




RMS

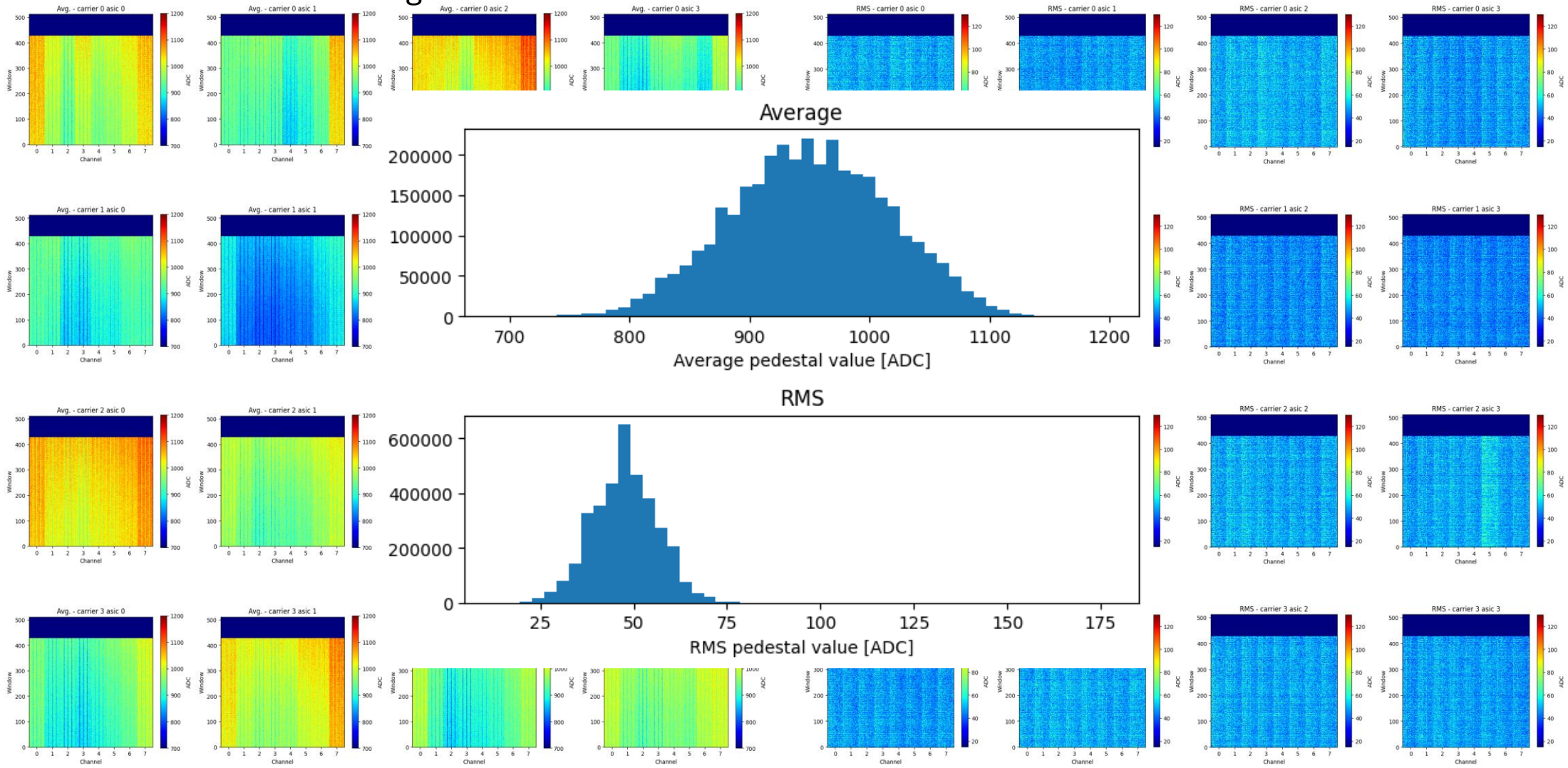


# Pedestal values for BS-3 (UH)

BS-3 → ch 7 → SCORD ID: 7

Average

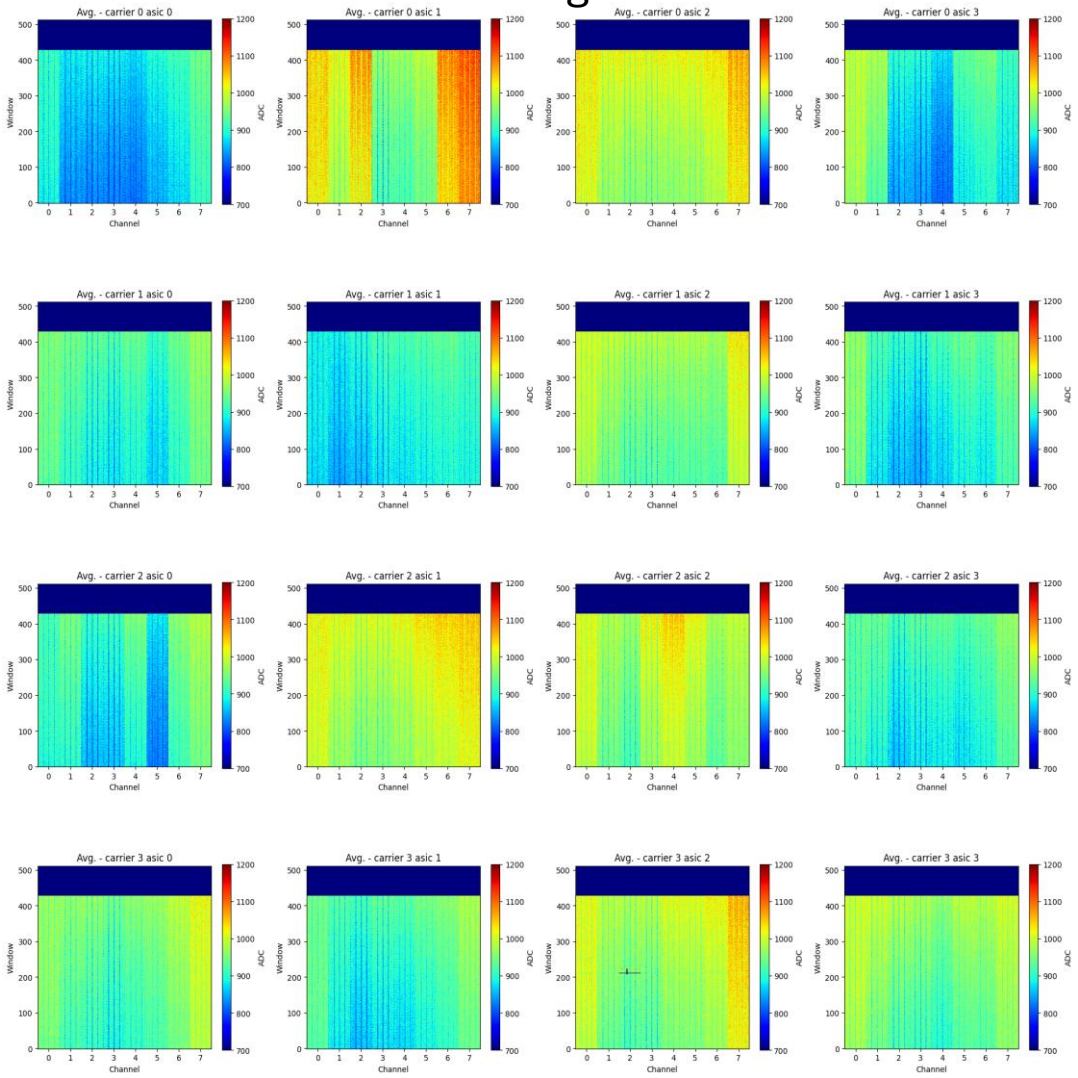
RMS



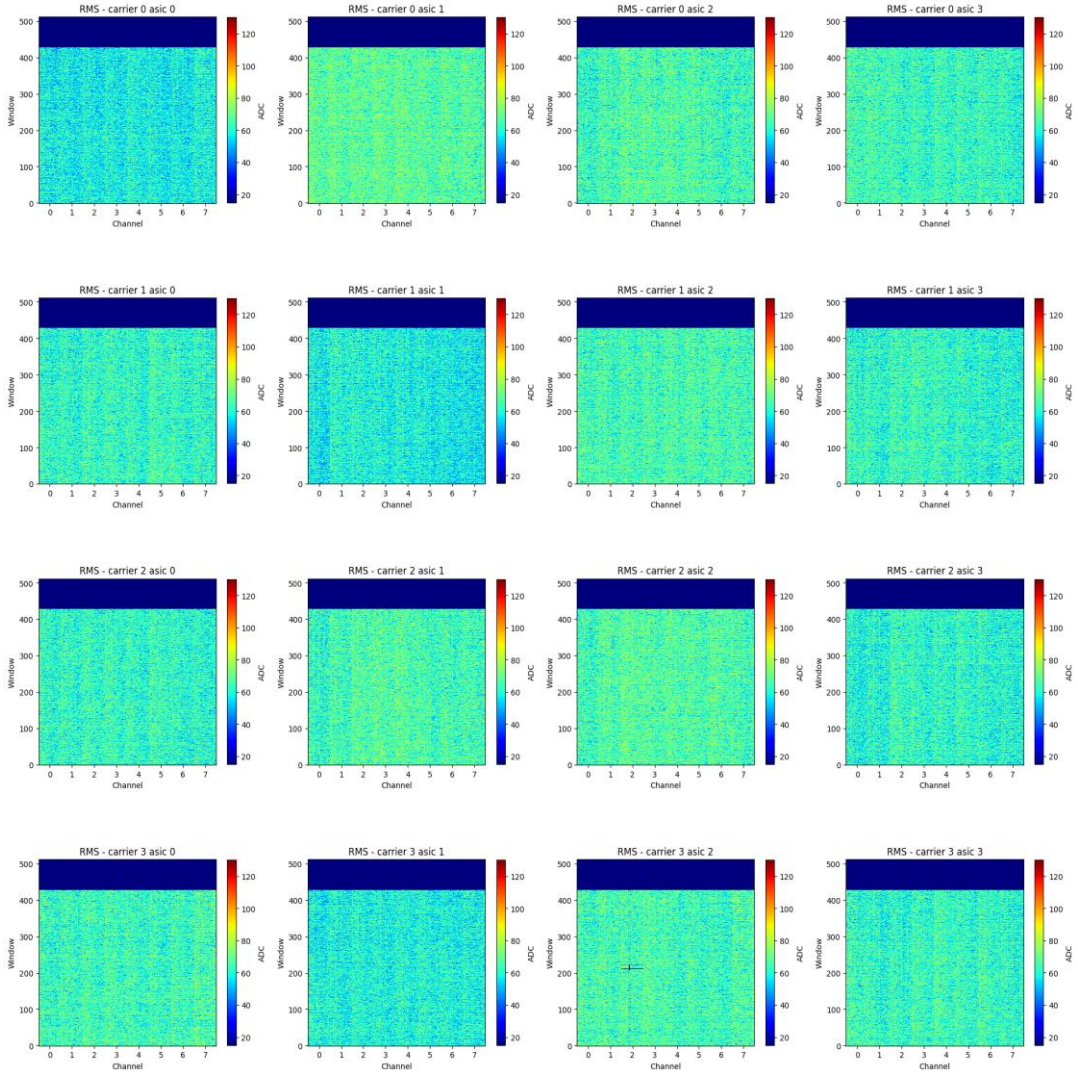
# Pedestal values for BS-5 (UH)

BS-5 → ch 11 → SCORD ID: 100

Average



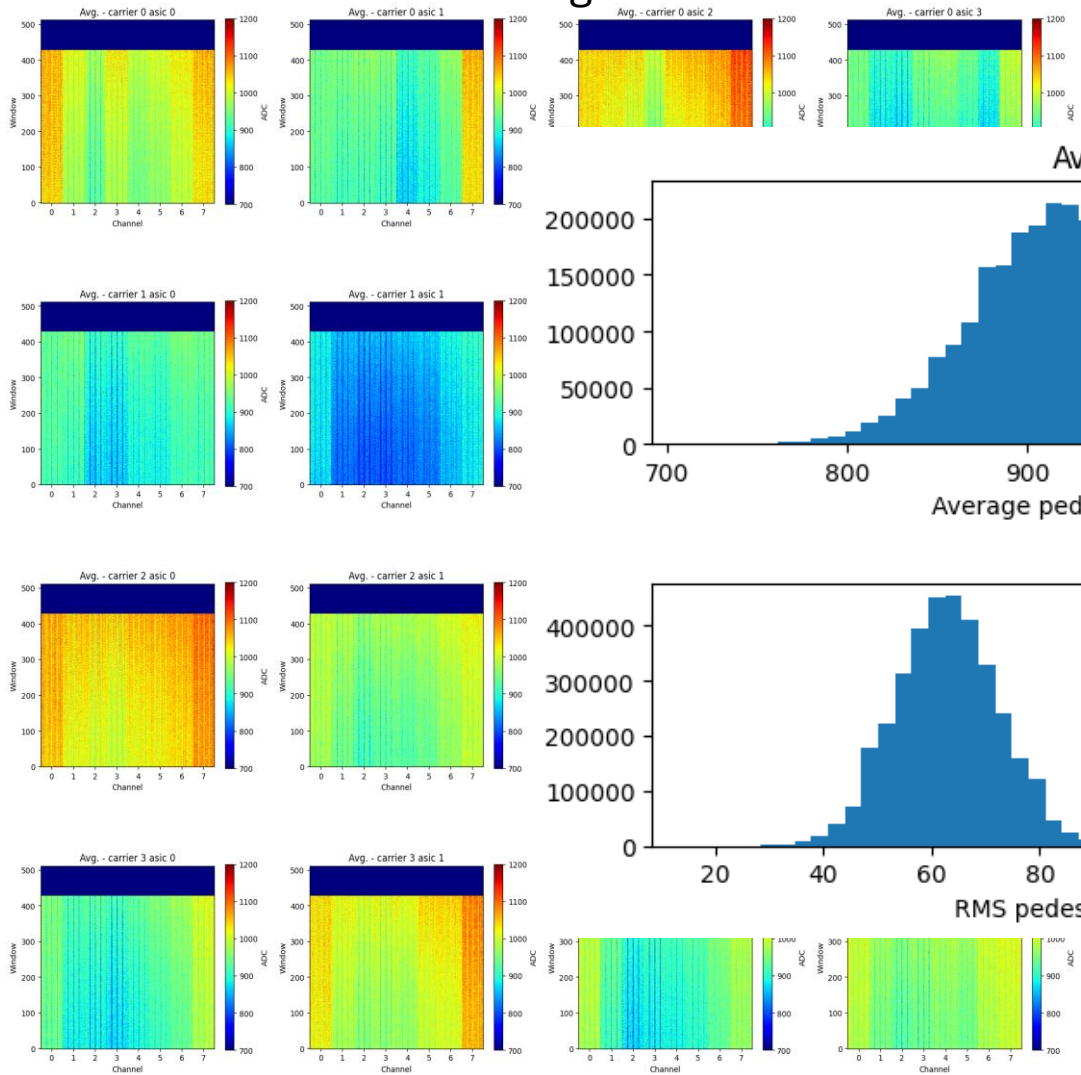

RMS



# Pedestal values for BS-5 (UH)

BS-5 → ch 11 → SCORD ID: 100

Average

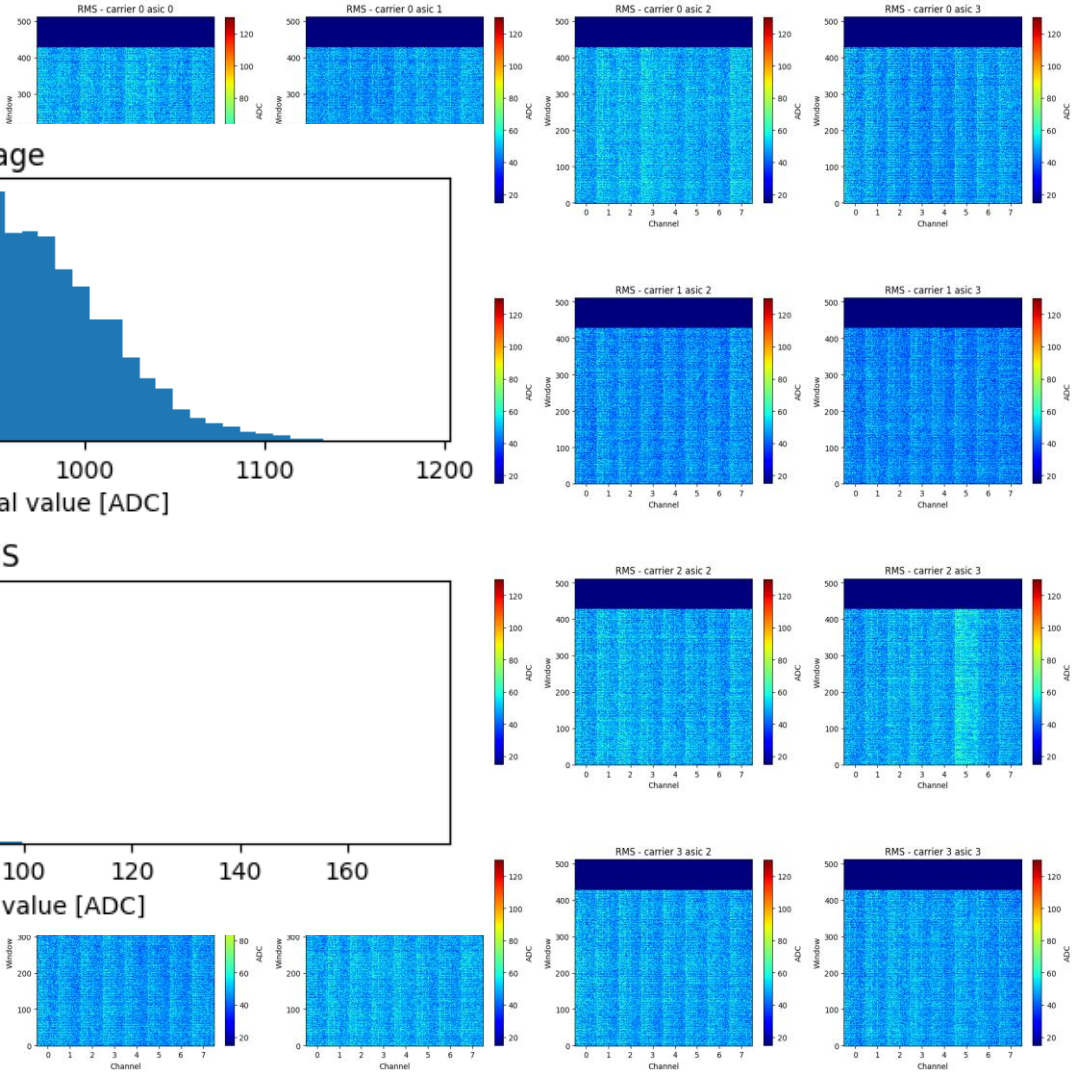









RMS



# Thank you for your attention.

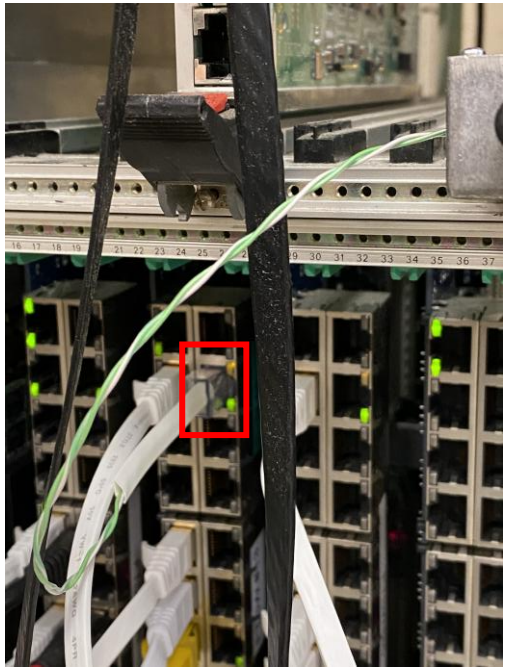
Any questions/comments?

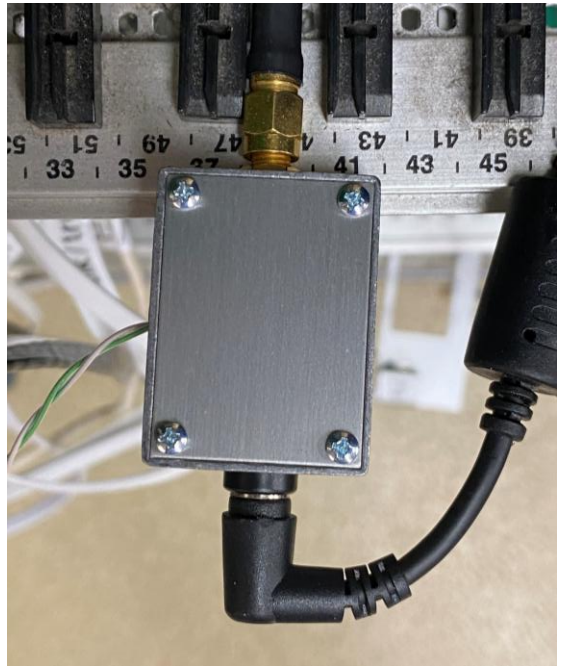
# Backup slides

# Upgrade of TOP Test Bench at Varner Lab

- Until now, the fast pulser was not synchronized with the FTSW (or triggers)
- This injected pulses randomly – provided a more realistic scenario

- After the upgrade, we can now sync pulser and FTSW triggers, and this ensures hits in every event
- We could still inject pulses randomly
- Current default is ~25% occupancy (hits in 2 out of 8 channels)
- Possible to run at full occupancy as well.





# B2L, HSLB, COPPER/PCIe40 data formats

## New data format for RawCOPPER hdr. and trl. (ver. alpha-200809)

- Remove COPPER header/trailer (which is currently removed on a readout PC. )
- Position in header will be removed to reduce header size.
- Error information in trailer (which link, what kind of error )
- XOR checksum ( less CPU power to re-calculate on host servers or HLT )

1 Number of total words
2 0x7f7f | Format ver.(8bit) | Number of words in this block ( 8bit )
3 exp no. (10bit=1024), run no.(22bit=4194304 including subrun )
4 event number(32bit)
5 From B2link FEE header 2 (TT-ctime | Trig-type)
6 From B2link FEE header 2 (TT-utime )
7 Node ID
8 b2link CRC error bit (4) | |truncation mask (truncated or not) / type of data (compressed,calibration, …)
9 Position of ch0 data
10 Posiont of ch1 data
…
56 Position of ch48 data

1word=32bits

RawCopper Header (56words)

Detector buffer(slot 0)

Detector buffer(slot 1)

B2link (FEE/HSLB) header and trailer

Detector buffer(slot 47)

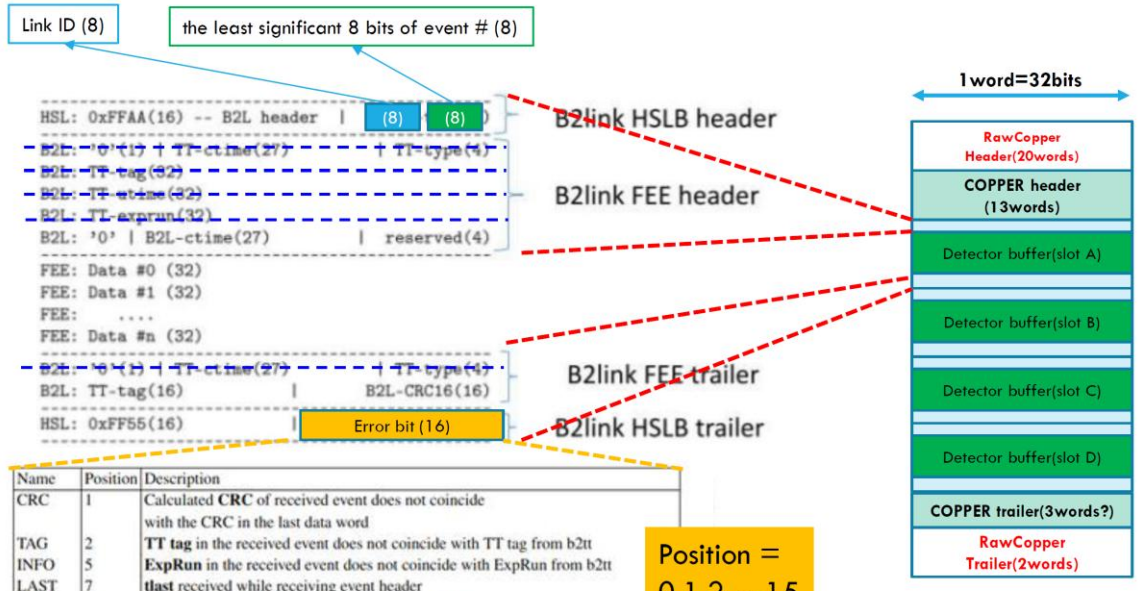
RawCopper Trailer(4words)

1 Error bit
2 Error slots
3 XOR checksum
4 termination word of this block = 0x7fff0006

12/6/2024 VER.1.2 OF NEW PCIE40 DATA FORMAT 2

## New data format for B2L/HSLB hdr. and trl. (ver. alpha-200809)

- Basically unchanged
- Added some info in ffaa header and ff55 trailer




| Name | Position | Description |
|---|---|---|
| CRC | 1 | Calculated **CRC** of received event does not coincide with the CRC in the last data word |
| TAG | 2 | **TT tag** in the received event does not coincide with TT tag from b2tt |
| INFO | 5 | **ExpRun** in the received event does not coincide with ExpRun from b2tt |
| LAST | 7 | **tlast** received while receiving event header |
| THR1 | 8 | Throttling in Belle2Link to prevent FIFO overflow |
| ANY | 9 | OR of all other error bits |
| TOUT | 10 | Timeout, no data received from the FEE for this trigger |
| AHEAD | 11 | **TT tag** from b2tt greater than **TT tag** in data |
| BEHIND | 12 | **TT tag** from b2tt smaller than **TT tag** in data |
| THR2 | 13 | Throttling of the long event (> 81920 B in a single channel) in the event processor |

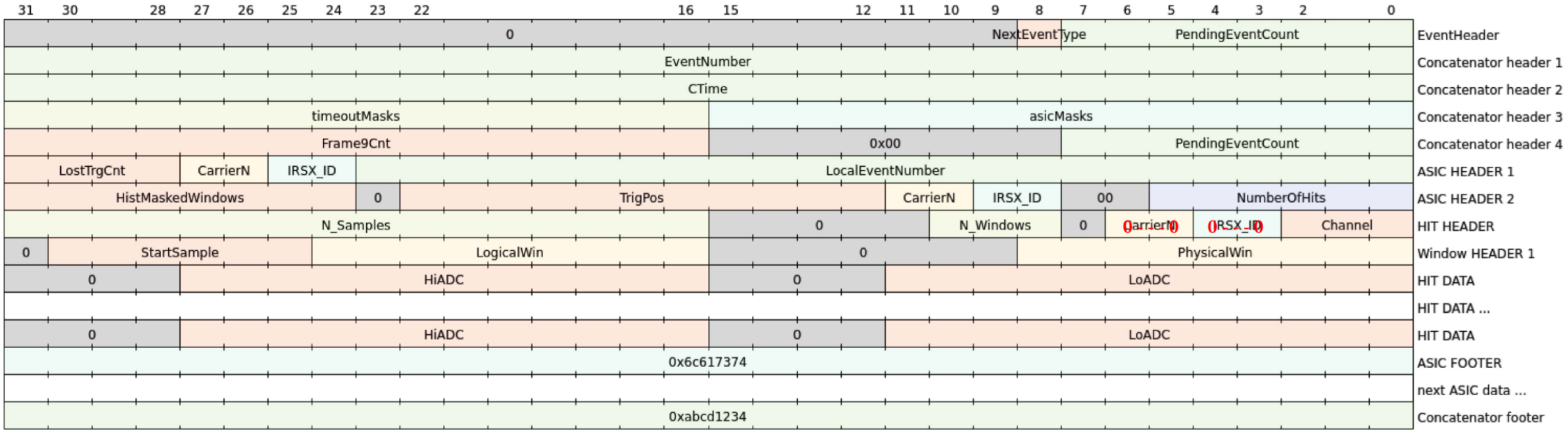
Position = 0,1,2 …15

Table VII: Error word in the DMA header and the last word of the event

VER.1.2 OF NEW PCIE40 DATA FORMAT 3

# Raw data format

**Note:** Hit header bits 3, 4, 5 and 6 are always 0.



# TOP Production Data Format

## Production Debugging 4.1

**2.2 Belle 2 TOP Data Format (Production Data)**

*Note that the data listed below does NOT include protocol headers; trigger type, ctime, utime, and trgtag are included in Belle2Link headers.*

| Word | Bits 31 30 29 28 27 26 25 24 | 23 22 21 20 19 18 17 16 | 15 14 13 12 | 11 10 09 08 07 06 05 04 03 02 01 00 | Hit |
|---|---|---|---|---|---|
| 0 | Type (=0x04) | Version (=0x01) | 0xA | SCROD _ID | N/A |
| 1 | EXTRA | NumWordsBonus | Phase(0-8) | NumWordsCore | |
| 2 | SKI RSVD(0000) | ctime (11 LSBs) | Revo9 Counter | | |
| 3 | ASIC Masks (TimeoutMasks \| Register Masks) | | eventQueueDepth | eventNumberByte | |
| 4 | Carr IRSX Channel | Window | 0xB | tFine WF H/S **Heap Window** | 1 |
| 5 | | vPeak | Integral | | 1 |
| 6 | | vRise0 | | vRise1 | 1 |
| 7 | | vFall0 | | vFall1 | 1 |
| 8 | SampleRise | dSampPeak dSampFall | **HeaderChecksum** | | 1 |
| | ... | | | | |
| N*(5+EXTRA)+4 | SD_type | Slow data | 1 0 1 | Nhits | N |
| | RAW HITS APPENDED HERE. | | | | |

Waveform Flag Heap/Stack Flag

"1 0 1 x" = 0xC or 0xD

= status bits

= reserved (0 for now)

= unsigned

= signed

*Sum of all 16-bit values in "hit header" = 0x0000*

Event size = (N*5+2) * 4 bytes e.g., for an event with 20 hits --> 408 bytes

at 30 kHz trigger rate, this gives 11.67 Mb/s

8000 is max words

NumWordsCore from hits alone, max is (13*MAX_HITS) = 3328

Max remainder then is 4672, so we should hae 13 bits reserved for it? Per raw hit, we have 18 words, so we can do a max of... 259 words

*Check with Luca on maximum number of hits per channel.

**Waveforms at the very end. Start with some kind. https://www.phys.hawaii.edu/repos/belle2/itop

***Waveform header, waveforms, waveform footer.

**Slow data types**

| | |
|---|---|
| 5 | FPGA temperatures |
| 9 | board temperatures |
| 1 | Humidity sensor |
| 24 | FPGA power values |
| 10 | FW/SW versions |
| 128 | Trigger scalers |
| 1 | pedestal measurement (10-bin average) |
| 178 | subtotal |