TOP Feature Extraction

Progress Updates & Plans

Shahab Kohani Harsh Purwar

TOP Feature Extraction Weekly Meeting
April 14th, 2025

PCIe40 Testing at UH

- Multiple issues with reading the data and modifying the PS bypass register during the week.
  - Currently working fully on Harsh's account.
  - PS bypass register can't be modified on my daqupsvr account.
- Wrong Endian data inside the PCIe40. Harsh wrote the function "swapEndian()" which must be used for both unpacking and packing of each individual word.
- Multiple issues found in the packer logic.
  - Missing output write lines
  - Attempting to overwrite the input data in case of pedestal bypass waveform writing to output.
  - Made modifications to fix which should be tested later today.

Data format

- Some clarification/confirmation needed:
  - Production Debugging 4.1 is used for waveforms.
  - Type 0 version 16 data used at KEK. Version 16 is the same as Production Debugging 4.1/ TOPunpacker code seems to confirm.
  - Integral is not calculated in TOP firmware. Is this needed?
  - Phase is set to zero. Looks like it reaches zero when reprogramming the BS. Expected behavior?
  - Raw Hits will include window header(s) and waveforms (17 or 18 words)

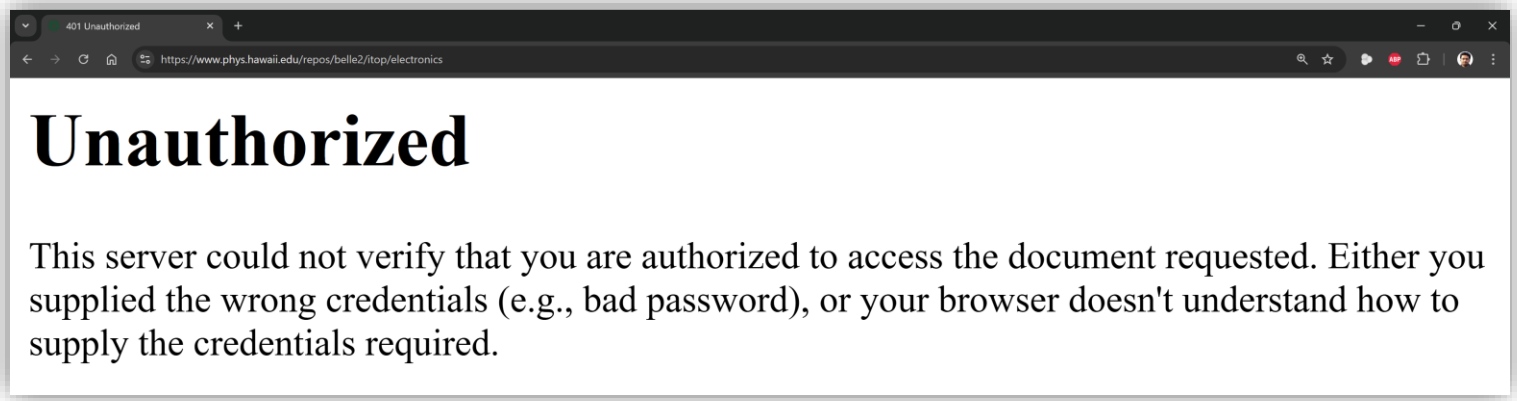
	Bits																													
Word	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**	**Hit**
0	Type (=0x04)								Version (=0x01)								0xA				SCROD _ID												N/A
1	EXTRA				NumWordsBonus												Phase(0-8)				NumWordsCore												
2	SKI	RSVD(0000)			ctime (11 LSBs)												Revo9 Counter																
3	ASIC Masks (TimeoutMasks | Register Masks)																eventQueueDepth								eventNumberByte								
4	Carr		IRSX		Channel				Window								0xB				tFine				WF	H/S	Heap Window						1
5				vPeak													Integral																1
6				vRise0																vRise1													1
7				vFall0																vFall1													1
8	SampleRise								dSampPeak				dSampFall				HeaderChecksum																1
	...																																
N*(5+EXTRA)+4	SD_type								Slow data												1 0 1				Nhits								N
	RAW HITS APPENDED HERE.																																

Updating SVN repo fails on TOP pocketdaq

- Vasily updated the SVN with the new FW version (SCROD PL 0x8C) with new TOP header.
- Issue:

```
[harsh@pocketdaq uh-svn-repo]$ svn up
svn: OPTIONS of 'https://www.phys.hawaii.edu/repos/belle2/itop/electronics': SSL
handshake failed: SSL alert received: Handshake failed (https://www.phys.hawaii.edu)
```

- Temporarily, I hope I can download the files over the web (need access!), required for TOP feature extraction tests or if someone with access (Matt, Vasily) could send it to me, that would work as well.



Using fast pulser to trigger FTSWs

Higher occupancy

- The current setup at UH has a fast pulser that generates pulses that mimic a hit.
- However, this pulser is not in sync with the FTSWs. Thus, we randomly feed in the pulses from this pulser to the TOP BS, so some events have hit, some don't – *more realistic scenario, I guess*.
- If we could use the pulser to trigger FTSWs we expect to have all events with hits – *higher occupancy*.
- Matt mentioned after the last meeting that he may have a board that could allow us do this using the AUX port of the primary/TOP FTSW (0x81/0x13).

Register access issue

Resolved!

- It has been observed in the past that at times TOP PS bypass register (0x4EF) fails:
  - to enable PS bypass mode (likely a register write access issue)
  - to readback the correct value (PS bypass is enabled but the register reads back the old value)

- I carried out a few careful tests using the two boardstacks (bs3, bs5).
- I power-cycled these, reloaded the TOP firmware (8A-93/82-23), configured the BS – all this worked as expected.
- I then read/write the register 0x4EF a few times and it seems to work perfectly fine.

- Shahab's account on TOP pocketDAQ was missing some crucial files and this was fixed few minutes back.

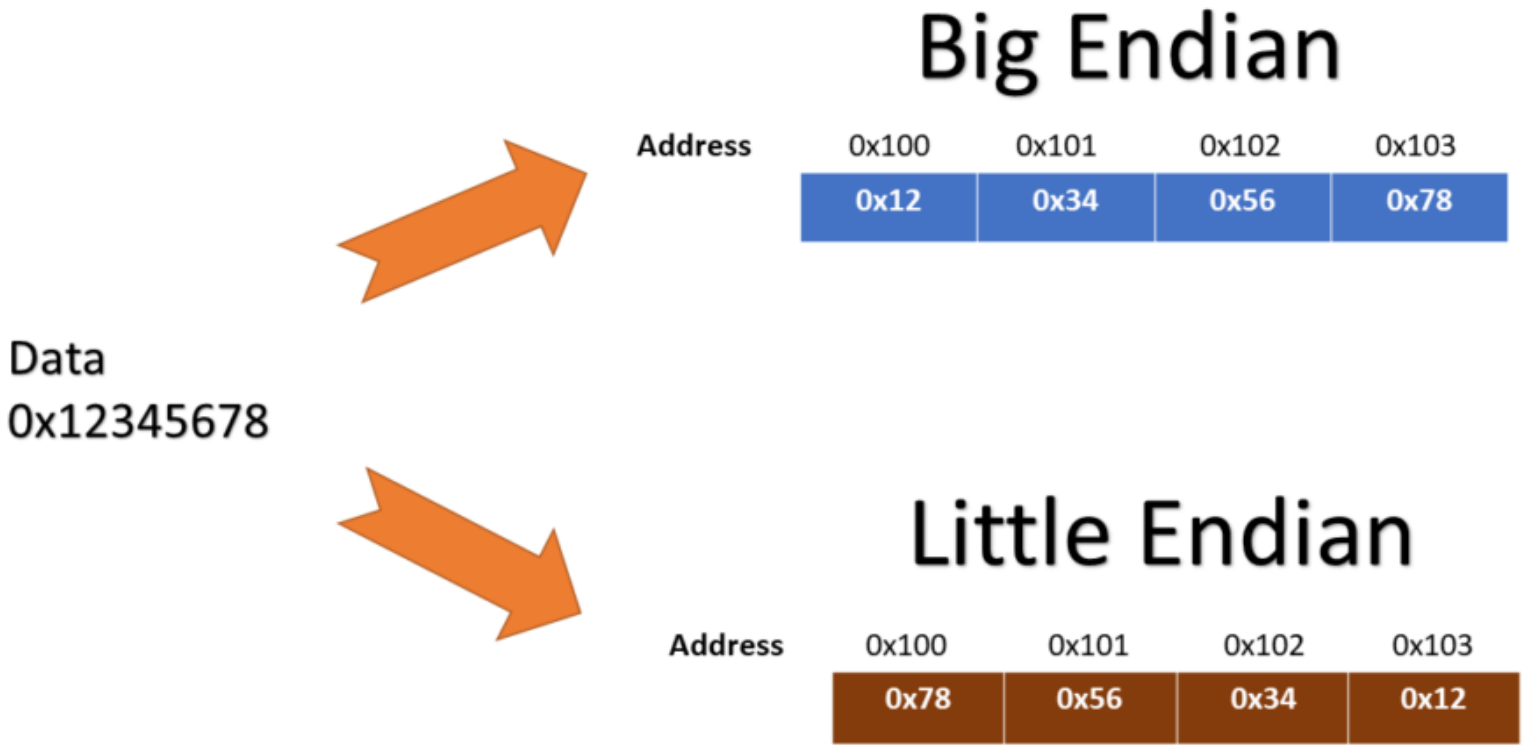
Plan for this week

- Wrap up the implementation of TOP Feature Extraction, version 1 enters testing phase, hopefully today.
- Yet to do for version 1:
  - Formatted output data words (header + data + raw waveforms) should be according to the actual TOP data format (Production debugging 4.1?) – to be confirmed with Kurtis/Vasily
  - Some debugging and final checks before testing.

- Testing phase plan:
  - Compare the output data format/words for a few events, manually.
  - Save several events (1M/10M) to file, run basf2 unpacker to check for errors.

Thank you for your time & valuable inputs!

Little and Big Endian



TOP Production Data Format

Production Debugging 4.2

2.2 **Belle 2 TOP Data Format (Production Data)**

Note that the data listed below does NOT include protocol headers; trigger type, ctime, utime, and trgtag are included in Belle2Link headers.

Word	Bits 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 09 08	07 06 05 04 03 02 01 00	Hit
0	Type (=0x04)	Version (=0x02)	0xA	SCROD _ID	N/A
1	EXTRA	NumWordsBonus	Phase(0-8)	NumWordsCore	
2	SKI RSVD(0000)	ctime (11 LSBs)	Revo9 Counter		
3	ASIC Masks (TimeoutMasks | Register Masks)		eventQueueDepth	eventNumberByte	
4	Carr IRSX Channel Window	0xB	tFine	WF SB **Integral**	1
5	vPeak	**H/S Heap Window 1**		**H/S Heap Window 0**	1
6	vRise0	vRise1			1
7	vFall0	vFall1			1
8	SampleRise dSampPeak dSampFall	**HeaderChecksum**			1
...					
N*(5+EXTRA)+4	SD_type Slow data	1 0 1	Nhits		N
	RAW HITS APPENDED HERE.				

= status bits

= reserved (0 for now)

= unsigned

= signed

SB: Straddle Bit

WF: Waveform Flag

Heap/Stack Flags, per Window

Sum of all 16-bit values in "hit header" = 0x0000

"1 0 1 x" = 0xC or 0xD

Event size = (N*5+2) * 4 bytes e.g., for an event with 20 hits --> 408 bytes

at 30 kHz trigger rate, this gives 11.67 Mb/s

8000 is max words

NumWordsCore from hits alone, max is (13*MAX_HITS) = 3328

Max remainder then is 4672, so we should hae 13 bits reserved for it? Per raw hit, we have 18 words, so we can do a max of... 259 words

*Check with Luca on maximum number of hits per channel.

**Waveforms at the very end. Start with some kind. https://www.phys.hawaii.edu/repos/belle2/itop

***Waveform header, waveforms, waveform footer.

Slow data types

5	FPGA temperatures
9	board temperatures
1	Humidity sensor
24	FPGA power values
10	FW/SW versions
128	Trigger scalers
1	pedestal measurement (10-bin average)
178	subtotal

TOP Production Data Format

Production Debugging 4.1

2.2 **Belle 2 TOP Data Format (Production Data)**

Note that the data listed below does NOT include protocol headers; trigger type, ctime, utime, and trgtag are included in Belle2Link headers.

Word	Bits 31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12	11 10 09 08 07 06 05 04	03 02 01 00	Hit
0	Type (=0x04)	Version (=0x01)	0xA	SCROD _ID		N/A
1	EXTRA	NumWordsBonus	Phase(0-8)	NumWordsCore		
2	SKI RSVD(0000)	ctime (11 LSBs)	Revo9 Counter			
3	ASIC Masks (TimeoutMasks | Register Masks)		eventQueueDepth	eventNumberByte		
4	Carr IRSX Channel	Window	0xB	tFine	WF H/S **Heap Window**	1
5		vPeak	Integral			1
6		vRise0		vRise1		1
7		vFall0		vFall1		1
8	SampleRise	dSampPeak dSampFall	**HeaderChecksum**			1
	. . .					
N*(5+EXTRA)+4	SD_type	Slow data	1 0 1	Nhits		N
	RAW HITS APPENDED HERE.					

Waveform Flag Heap/Stack Flag

"1 0 1 x" = 0xC or 0xD

= status bits

= reserved (0 for now)

= unsigned

= signed

Sum of all 16-bit values in "hit header" = 0x0000

Event size = (N*5+2) * 4 bytes e.g., for an event with 20 hits --> 408 bytes

at 30 kHz trigger rate, this gives 11.67 Mb/s

8000 is max words

NumWordsCore from hits alone, max is (13*MAX_HITS) = 3328

Max remainder then is 4672, so we should hae 13 bits reserved for it? Per raw hit, we have 18 words, so we can do a max of... 259 words

*Check with Luca on maximum number of hits per channel.

**Waveforms at the very end. Start with some kind. https://www.phys.hawaii.edu/repos/belle2/itop

***Waveform header, waveforms, waveform footer.

Slow data types

5	FPGA temperatures
9	board temperatures
1	Humidity sensor
24	FPGA power values
10	FW/SW versions
128	Trigger scalers
1	pedestal measurement (10-bin average)
178	subtotal