High Energy Physics Integrated Circuits design

What is HEPIC?

- HEPIC is a consortium of IC design engineers and physicists working in High Energy Physics (HEP) instrumentation

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… but also …

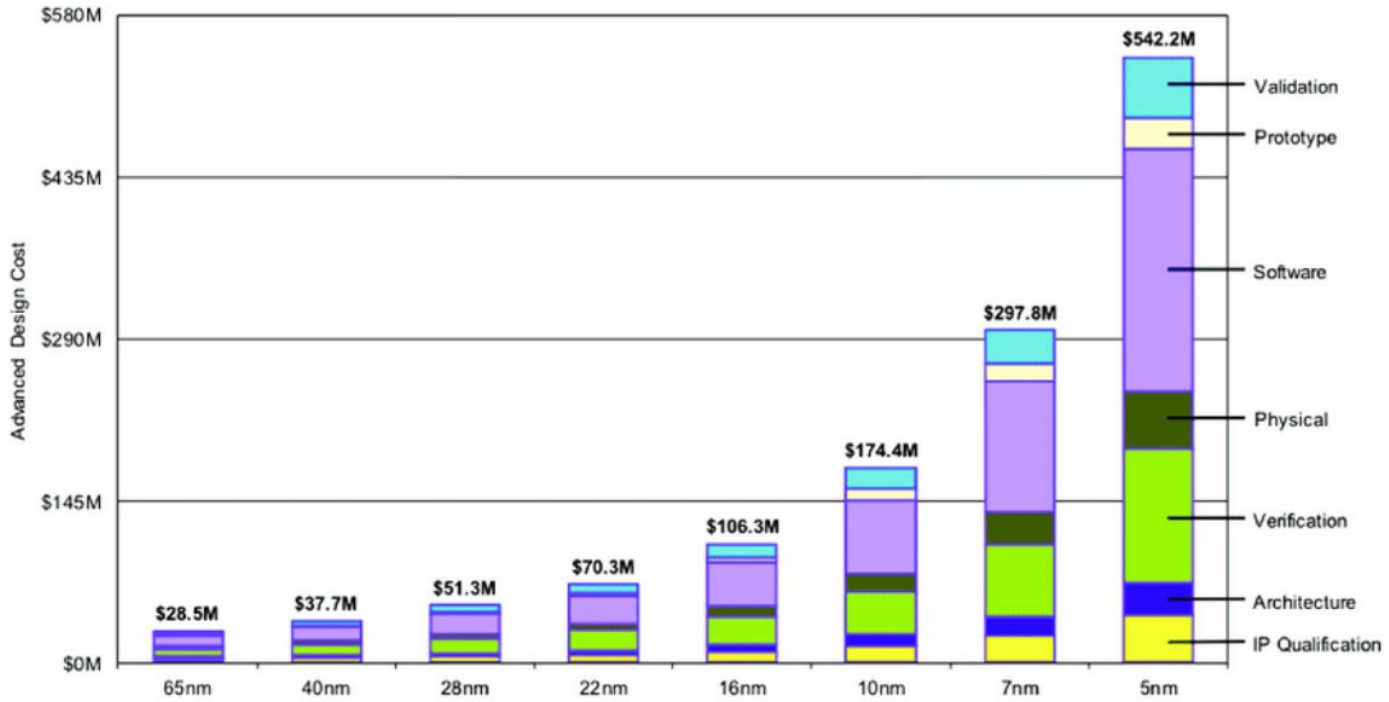
- An IC Design Traineeship Program With Applications In High Energy Physics (HEPIC)

HEPIC consortium

- HEPIC is a consortium of IC design engineers and physicists working in High Energy Physics (HEP) instrumentation
- Webpage: https://www.hepic.org
- Members: 10 Universities, 5 National Labs
- Goals:
  - Coordinate activities across U.S. Universities and National Labs
  - Forum for ASIC designers to interact and synchronize on technical matters (*e.g.*, foundry processes to standardize on, EDA tools, open-source)
  - Advocate for common needs
- Workshops are held periodically: last HEPIC 2024 workshop was held at Brookhaven National Laboratory
- HEPIC is affiliated with / provides inputs to CPAD on ASIC topics

HEPIC

Why HEPIC?


$580M
$435M
$290M
$145M
$0M
Advanced Design Cost
$28.5M
$37.7M
$51.3M
$70.3M
$106.3M
$174.4M
$297.8M
$542.2M
65nm
40nm
28nm
22nm
16nm
10nm
7nm
5nm
Validation
Prototype
Software
Physical
Verification
Architecture
IP Qualification

Summary of HEPIC 2024 workshop

- ASIC design topics:
  - Cryo-CMOS technologies and designs
  - ASICs for future trackers: timing detectors, monolithic, beyond Si
  - EdgeAI/Unconventional computing (overview talks from institutions and selected speakers)
- Open-source tools and IPs
- Inter-institutional projects: recent experiences, issues and what’s next
- Collaboration between universities and National Laboratories
- Collaboration with industry and other research agencies
- Training opportunities and workforce development

Some initiatives from HEPIC

- Three-way NDA IMEC/TSMC/HEPIC for TSMC technologies ≥ 28nm:
  - Signed by 4 National Labs, few Universities
  - Provides legal framework to collaborate on selected technologies
  - Without it, it would not be possible to share IPs and circuits
- Common access to EDA tools:
  - Negotiate common access to EDA tools with price agreed across DOE
- Open-source tools and IPs:
  - Software/RTL code is easier to share (*see SLAC surf, FNAL Spacely, etc…)*
  - Shared experience on open-source tools: some mature and in use (cocoTB), some are not (analog tools not quite there yet)

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Traineeship Program With Applications In HEP

Website: https://ee.stanford.edu/academics/hepic

- **Goal:** training at a DoE, introduce students to the HEP design community, the scientific ASIC design challenges they face, and other students across the country who are part of the same program.
- **Participating institutions (as of 2025):**
  - **Universities:** Stanford, UC Davis, UC Santa Cruz, University of Texas Arlington.
  - **National Laboratories:** Argonne, Brookhaven, Fermilab, Lawrence Berkeley, SLAC
- The program is running well,
- Would be better to have a larger pool of students
- Please reach out if you are interested in joining!

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Traineeship Program With Applications In HEP

- **The program provides:**
  - Tuition supplement and $35k yearly stipend for 2 academic years of PhD / Master
  - Summer training at a DoE National Laboratory
- **Program Organization**
  - Fall Quarter
    - Students find out about program
    - They apply to the program, and start taking IC design classes
    - PIs review applications and select apprentice
  - Winter Quarter
    - Lab propose projects
    - Meeting where projects are introduced
    - Student – lab project matching process

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HEPIC summer week 2025

Sign up now for the next edition!

https://indico.slac.stanford.edu/event/9769/overview

- In-person only @ SLAC National Laboratory (sorry, no, there's no Zoom!)
- June 23 - 27, 2025
- Maximum 20 participants
- Mornings: lectures on physics and IC design topics:
  front-end design, Cryo-CMOS, timing detectors, A/D converters
- Afternoons: practical design exercises
- Speakers from LBNL, SLAC & industry

HEPIC

Testimonials and impressions

- *'I learned a lot in terms of physics of colliders and accelerators and how that physics is translated to hardware design and circuits. As a non-expert in IC, I learned a lot about circuits and their components.'*
- *'Thank you for this amazing experience, I had a lot of fun and enjoyed meeting the other students.'*
- *'Before participating in this program, I had very limited knowledge about High Energy Physics detectors. After experiencing the lectures, tours, and working on the design challenge, I am definitely intrigued by the prospect of designing readout ASICs for HEP detectors.'*