Implementation of small-scale ML in Belle II Chamber Drift Chamber Front-End Electronics for cross-talk noise reduction

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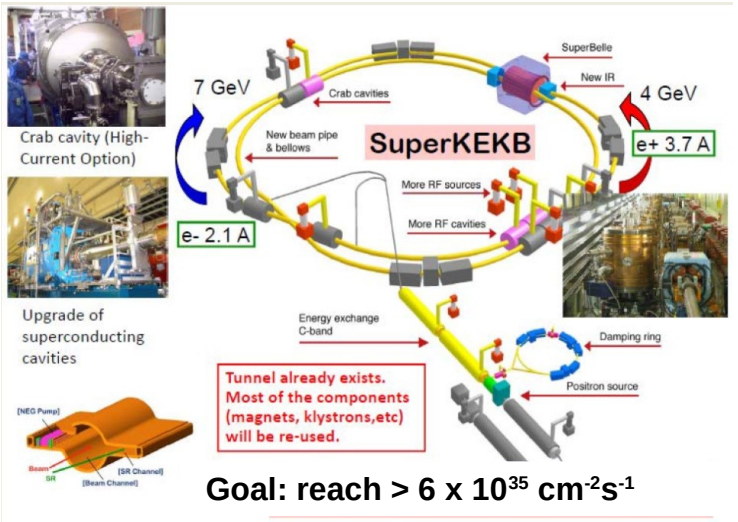
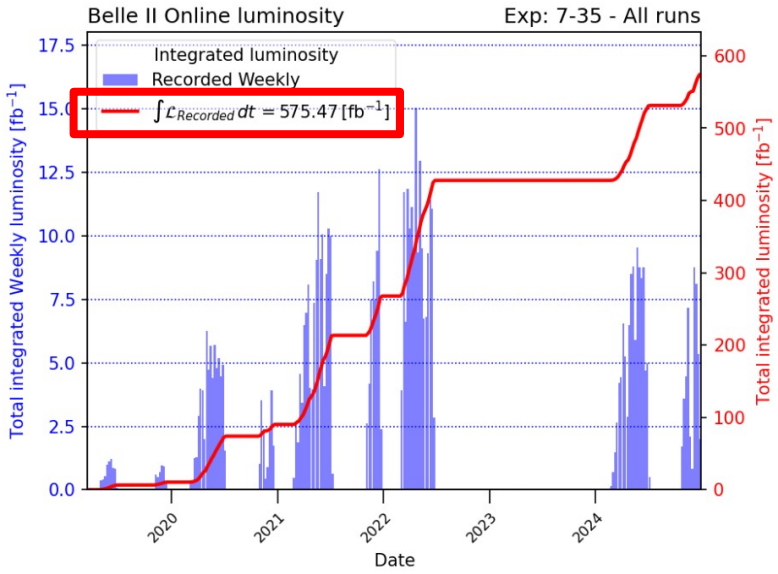
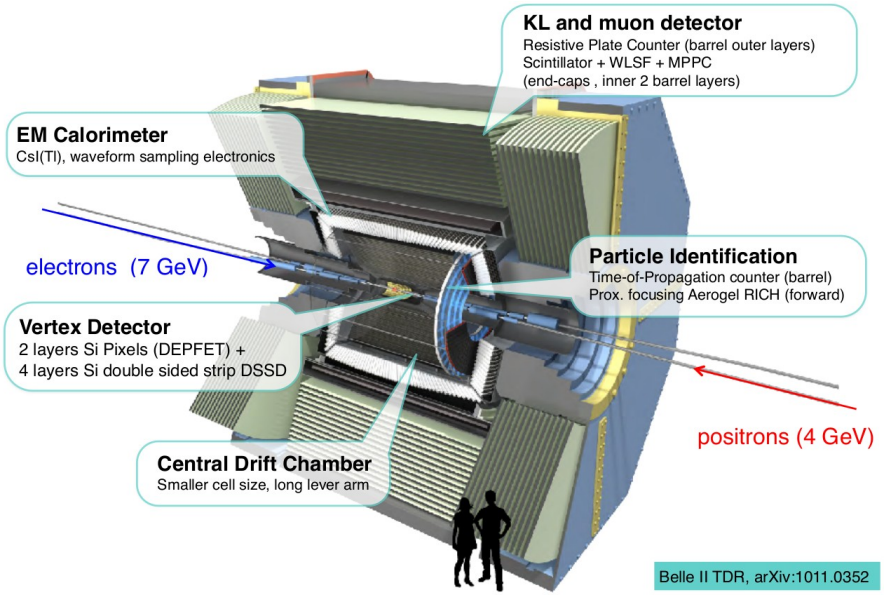
SuperKEKB and Belle II

- SuperKEKB: Upgraded from KEKB.
  - More than 30 times larger luminosity of KEKB with nano beam scheme.
- Asymmetric collision with 7.0 GeV e^- and 4.0 GeV e^+ for Y(4S) $\rightarrow B\overline{B}$.
- Belle II: Newly-designed sub-detectors set to improve detection performance.
  - Physics target: Rare B, τ, charm physics, Dark Matter search, CP Violation.

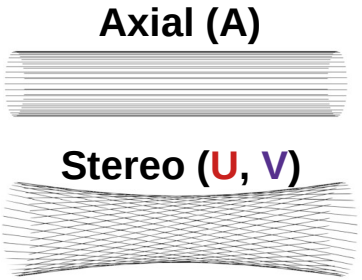


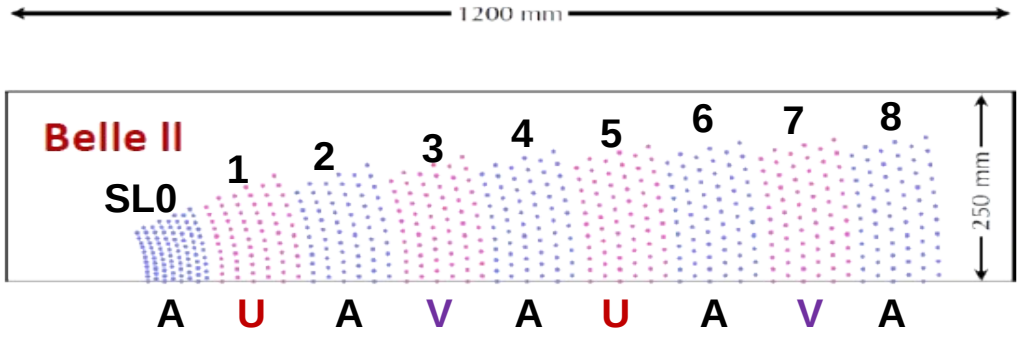


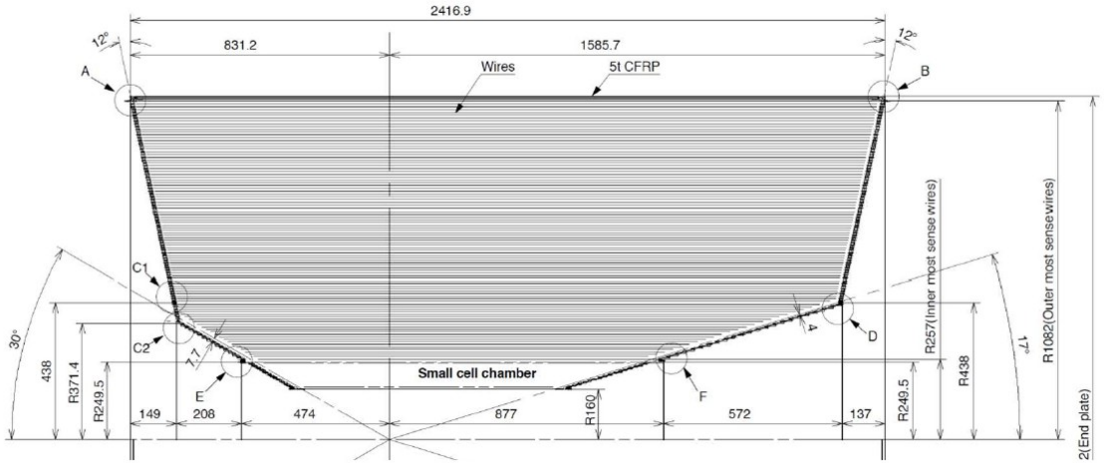


Belle II Central Drift Chamber

- Central Drift Chamber (CDC): One of the major charged tracking device in Belle II.
- About 14 thousand of sense wires and mixture of He and ethane as ionization gas.
- Gas atoms' ionization will accumulate charges on sense wires when charged particles go through.
- An alternative **AUAVAUAVA** wire configuration for 3D information:
  A: Axial super-layer (SL) parallel to z-axis
  U, **V**: Stereo SL with two small stereo angles.

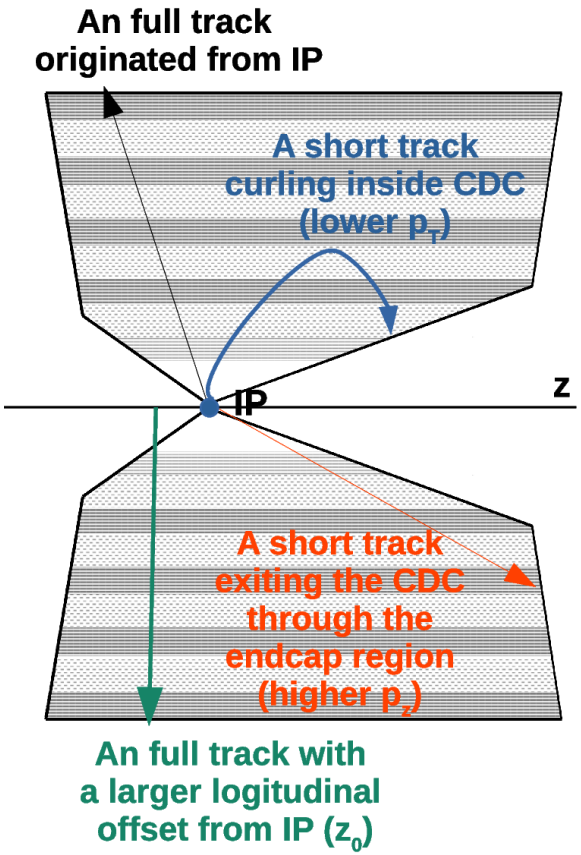


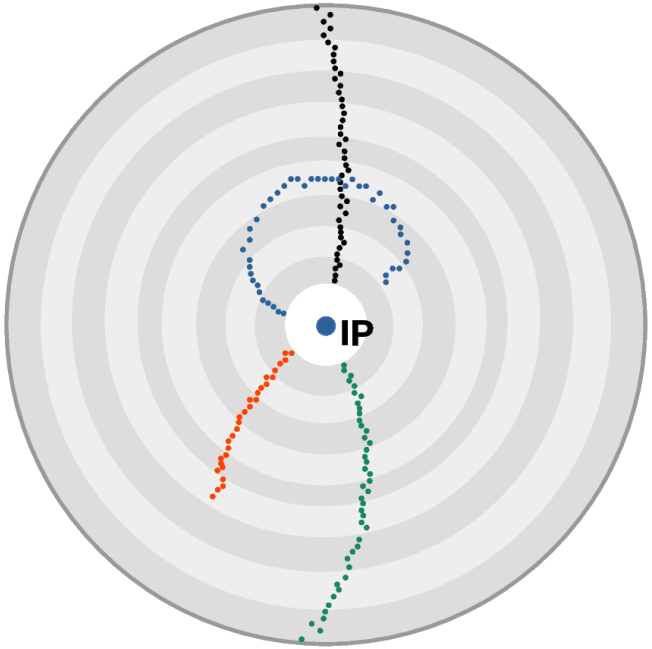




Tracking with CDC

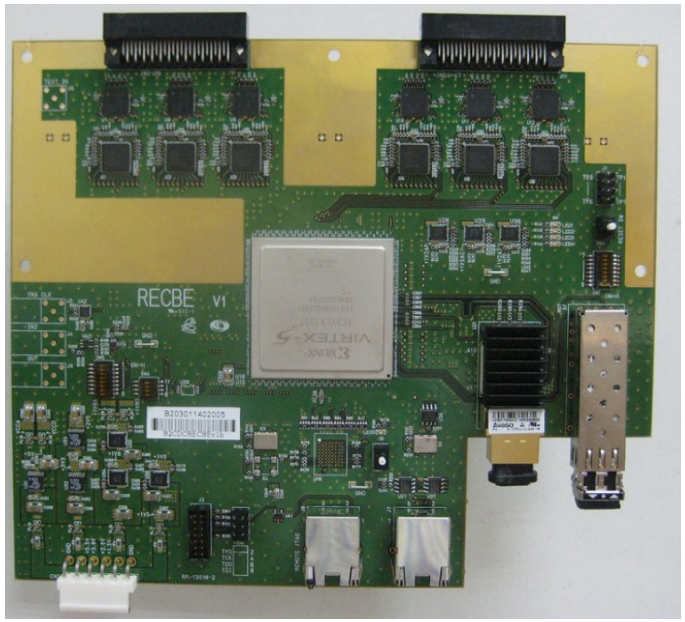
- A simple illustration of tracking with Belle II CDC:
  - Full track is the major one to be searched and used in Level-1 trigger.
    - 2 full tracks with additional condition is essential for high multiplicity physics: Tau, hadronic events.
    - 2D information is enough for finding full track. 3D information (z) can further reduce the background for it.



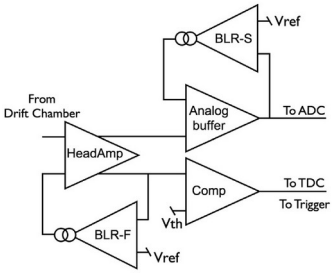


Front-End Electornics

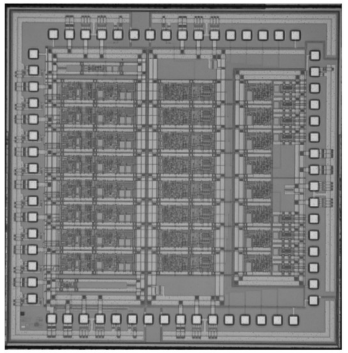
- Featured with Xilinx Virtex-5 FPGA
- In total ~300 FEE for the entire CDC
- ASIC for ADC and shaping
  - 1 ASIC for 8 wires. In total 48 channels (6 ASICs) per FEE.
- Optical modules for data paths to TRG and DAQ.



Single channel



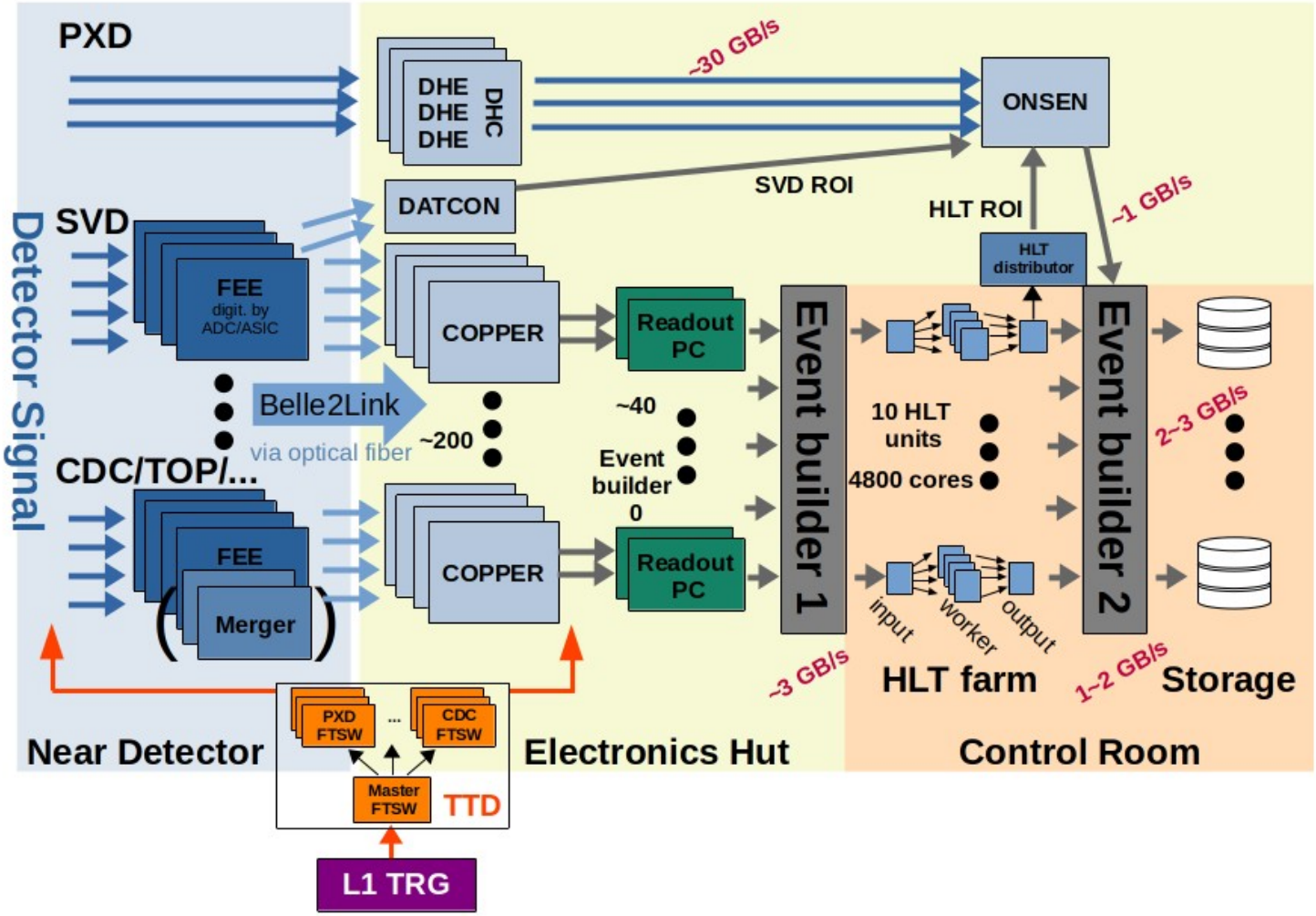
2.5x2.5 mm^2



NIM A 735 (2014) 193-197

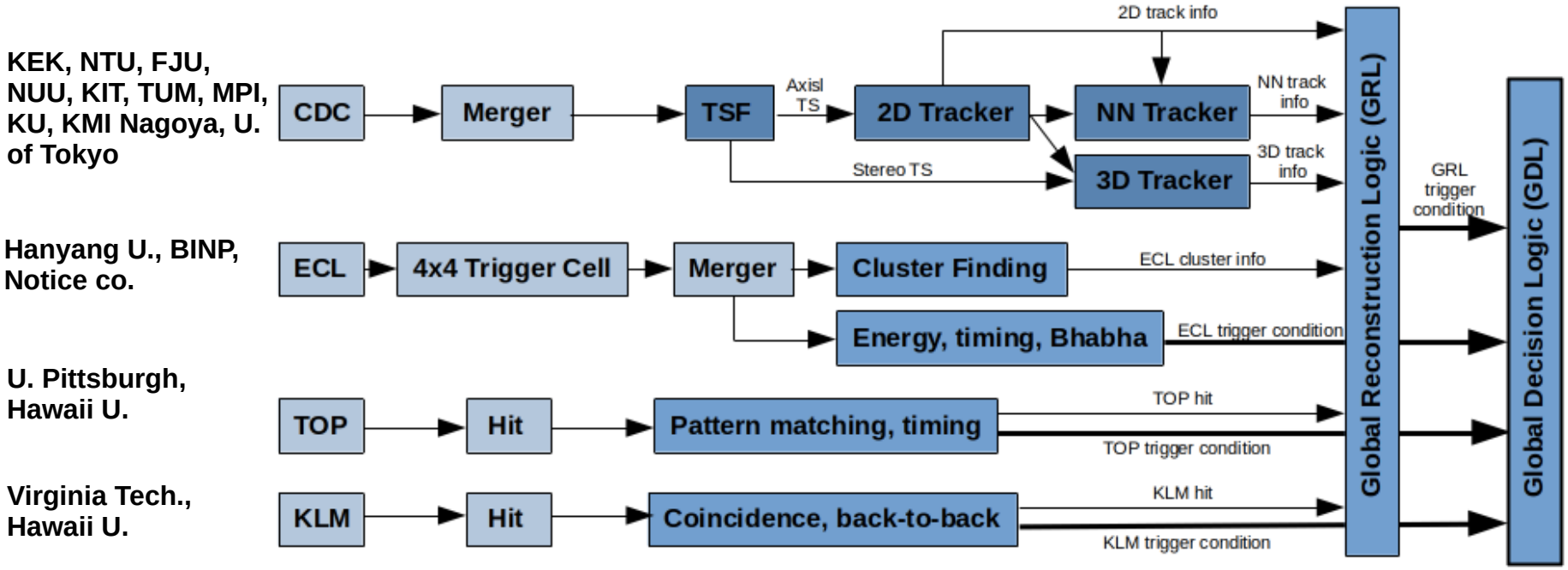
Belle II DAQ

- Standalone Level-1 hardware trigger: max 30 kHz at peak luminosity
- HLT: CPU farm



Belle II Level-1 trigger

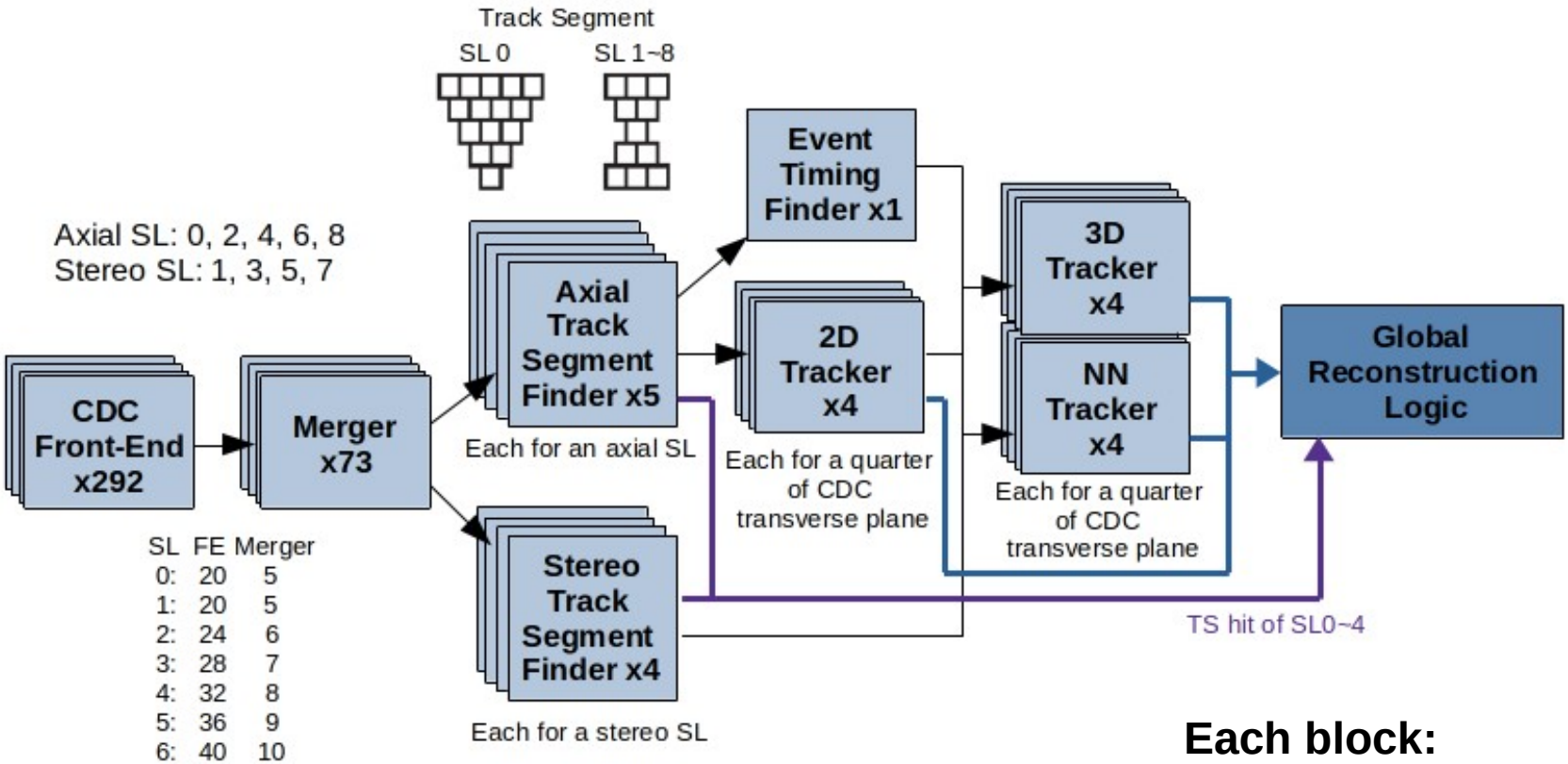
- 4 sub-trigger systems + 2 global trigger systems.
- Every block is FPGA boards with specific algorithm.
- Comprehensive trigger menu to select various kinds of physics events.
- Everything in this chain has to be finished in ~5 μs.



KEK, NTU, NCU

Belle II CDCTRG

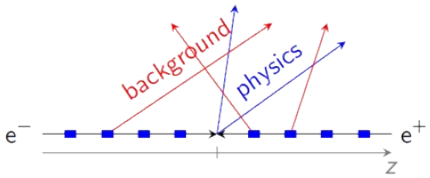
- Real-time tracking in Level-1 trigger.

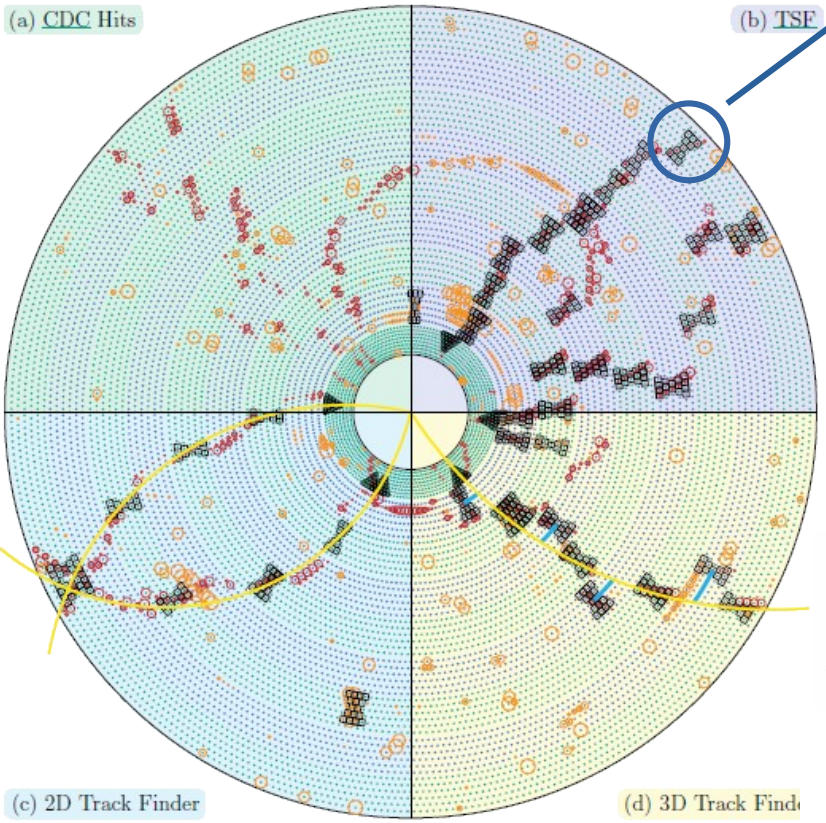


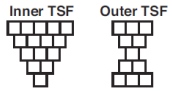
Each line with arrow:
Optical link
(max. 25 Gb/s/link)

Each block:
A FPGA board with complicated algorithm logic design.

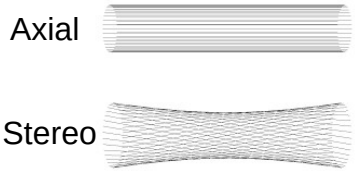
Tracking with CDC for Level-1 trigger



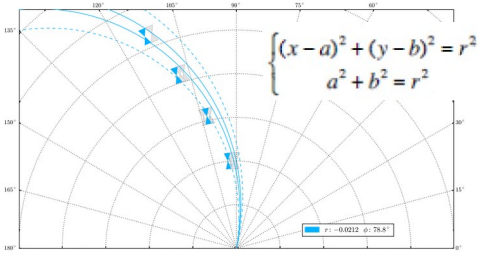




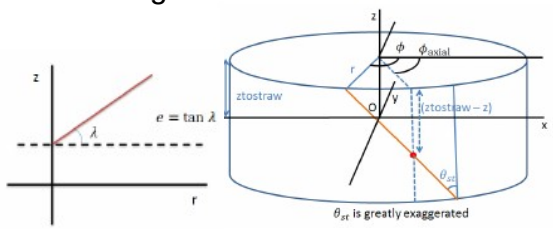
Track Segment:
Simplification on the algorithm

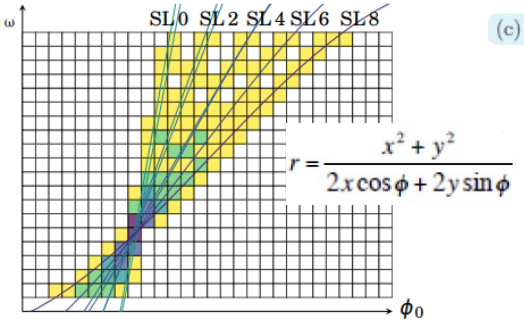


2D Track Finding:
Hough transformation.
Limited track condition.

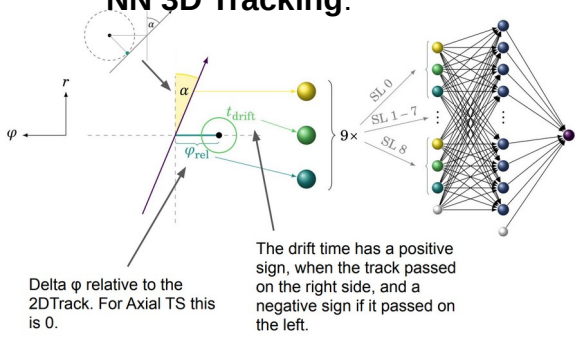


3D Tracking:
Fitting with Stereo wire info





NN 3D Tracking:

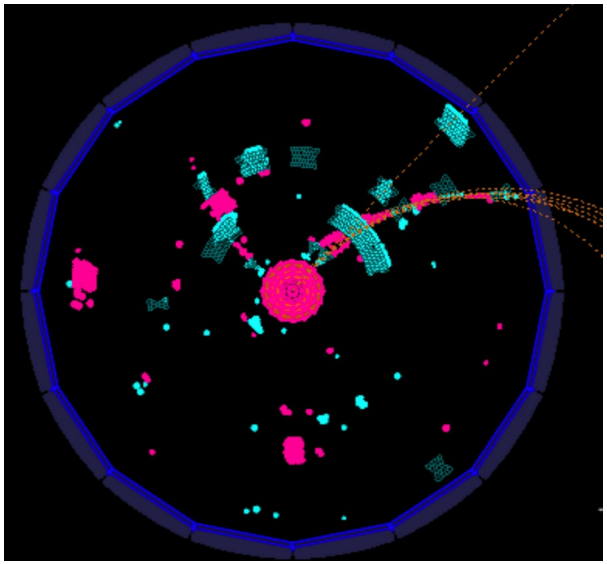


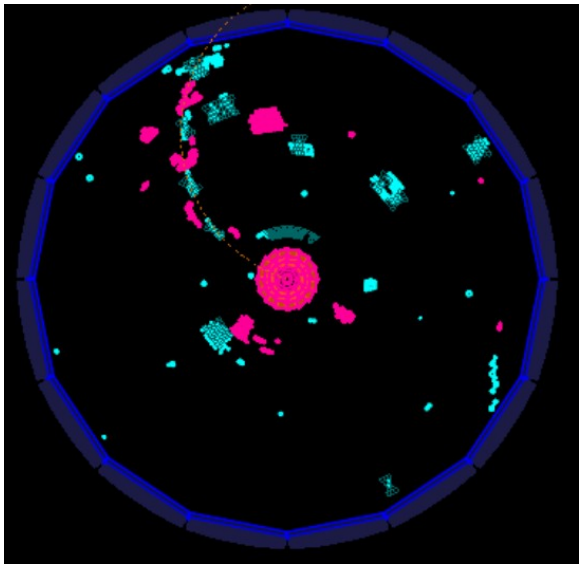
Tracking in Level-1 trigger is based on reduced dimension (Track Segment) for adaptation in FPGA.

CDC cross-talk noise

- In the present Belle II operation so far, bunch of wire hits in neighboring regions occurred frequently without associataion to tracks.
  - The exact reason is still unknown.
  - Not only in beam collision, but also in cosmic run.

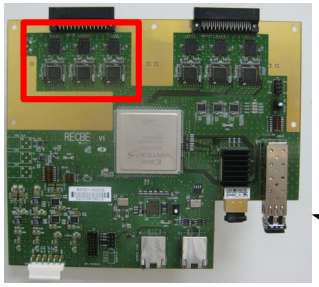
- In term of Level-1 track trigger in FPGA:
  - 2D tracking with Hough transformation and reduced dimention.
    - High fake trigger rate in L1 tracking due to cross-talk noise: a factor of 2 or more.
  - Also increases loading in HLT processing.





Real-time CDC cross-talk noise reduction by AI/ML in FEE

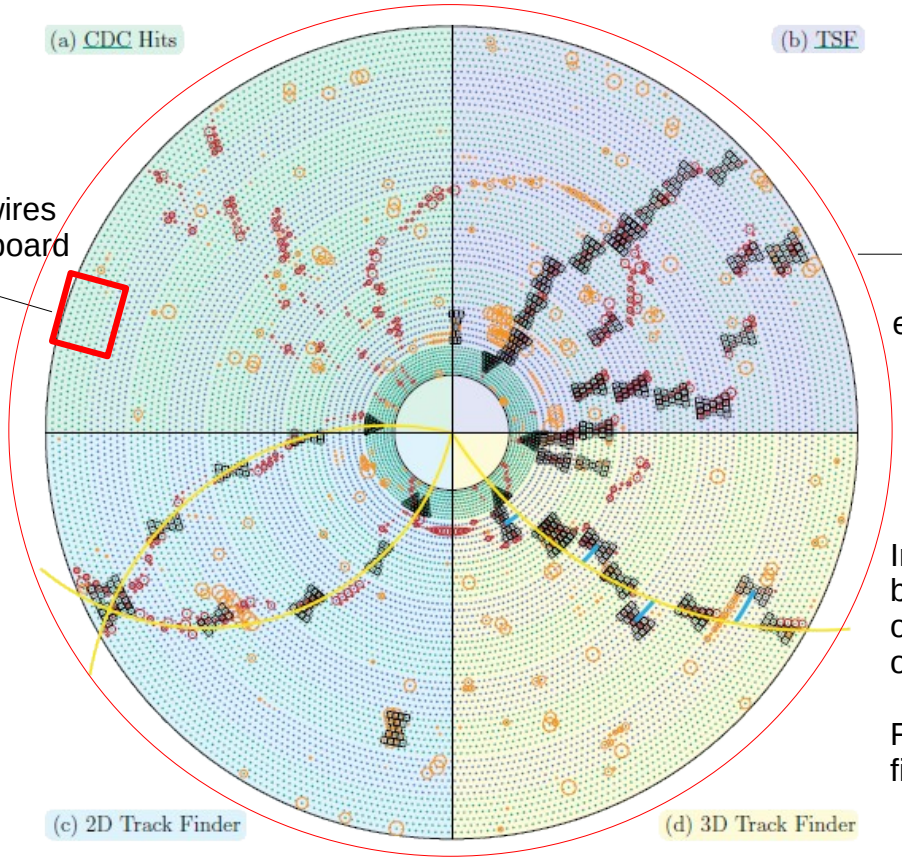
ASIC for
ADC, TDC and shaping purpose



CDC FEE
Xilinx Virtex-5
Collect the 48 channels
(8 * 6 ASICs)
information (ADC, TDC)
to downstream.

FEE has s mall coverage on the detecor, and all it has are the waveform info of each channel.

48 wires
per board



Almost the
entire detector

Belle II UT4
UltraScale

In L1 trigger, we use large-scale backend FPGA device (UltraScale, or even Versal) with a global scope of detector to perform reconstruction.

For instance, a GNN-based noise filtering on CDC.

Our plan: Small-scale AI/ML in FEE on each channel for noise reduction.

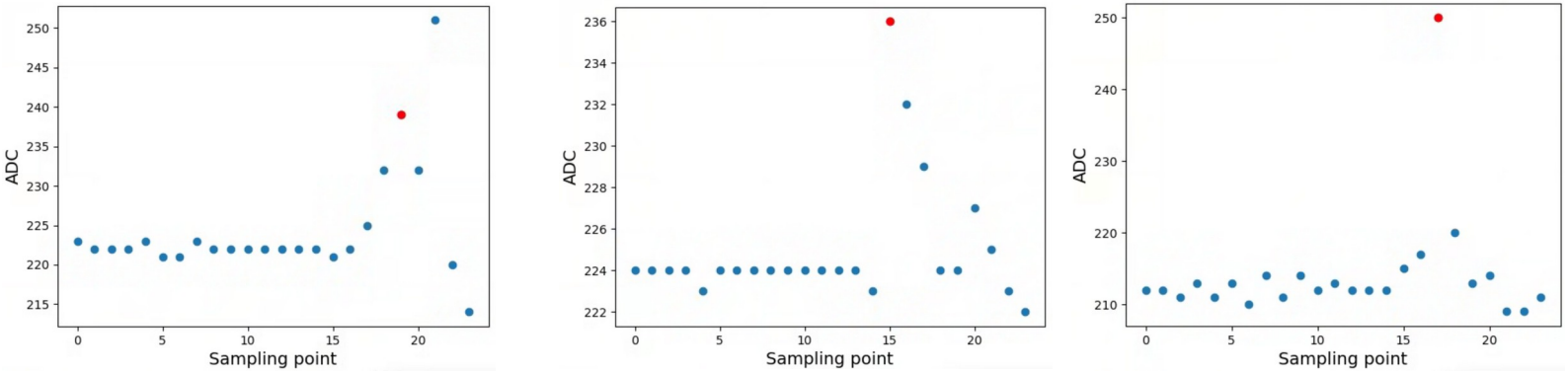
ADC waveform data from CDC FEE

J. Phys.: Conf. Ser. 762 012007, 2016
Comput Softw Big Sci 3 1, 2019

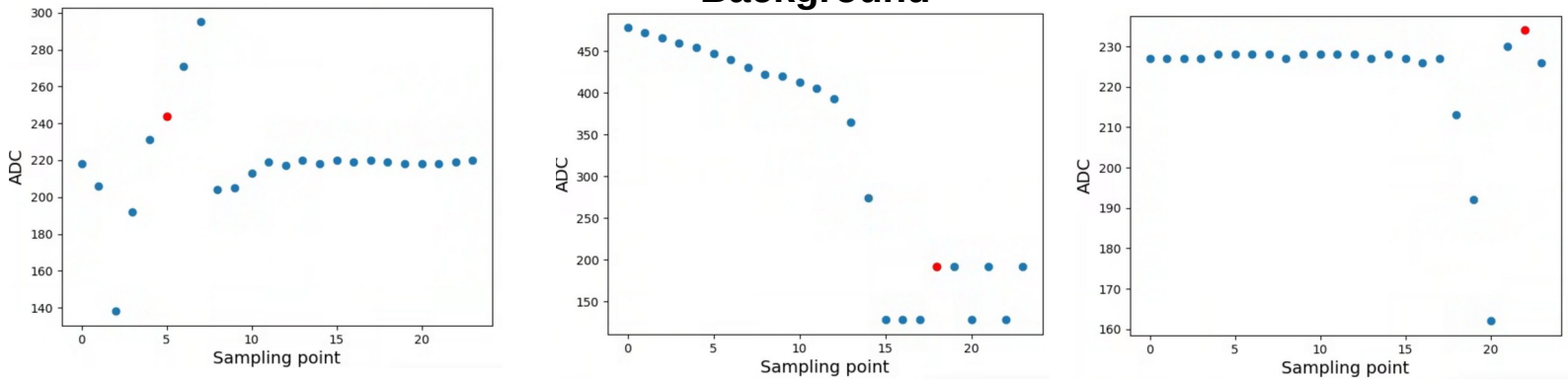
- We use the waveform data taken from FEE in beam collision runs.
- To isolate signal wire hits for training, we rely on the offline tracking software of Belle II.
- For background, we limit the number of hits > 6 over the 8 channels in an ASIC chip.
  - Although both of the selections are not perfect, they can select relatively pure signal/backgrund samples.

Signal

Red point: when TDC is fired.



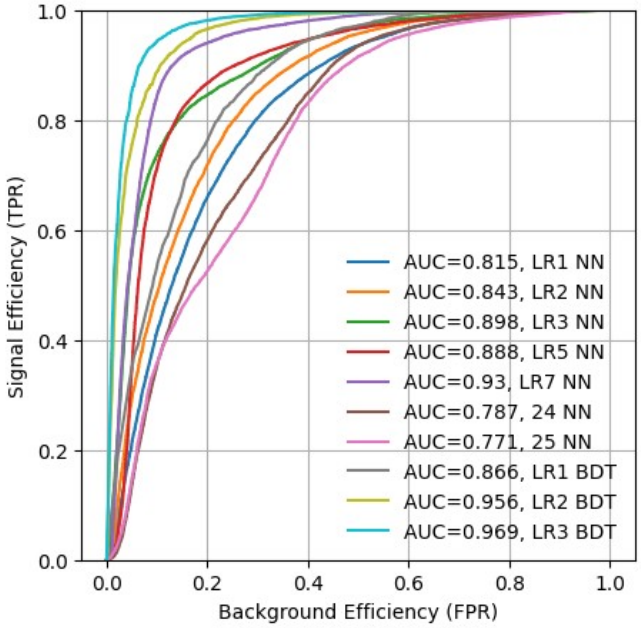
Background

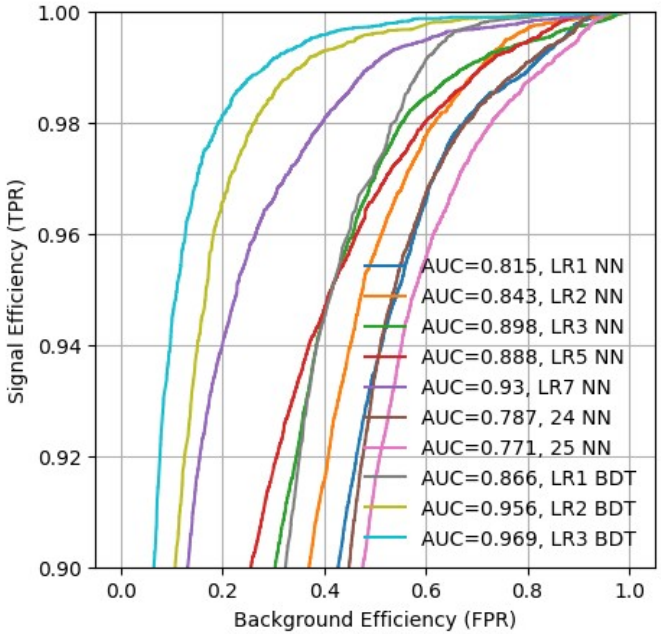


Model building

- We use NN (Keras → hls4ml) and BDT (scikit learn → Conifer) models to test.
  - NN: 2~3 hidden layers.
  - BDT: depth = 3, 10~15 estimators.
  - CNN is also tested but it's not very good.

- Among all the options, BDT is suprising good!
  - It can reject ~65% of bkg at 99% signal eff.



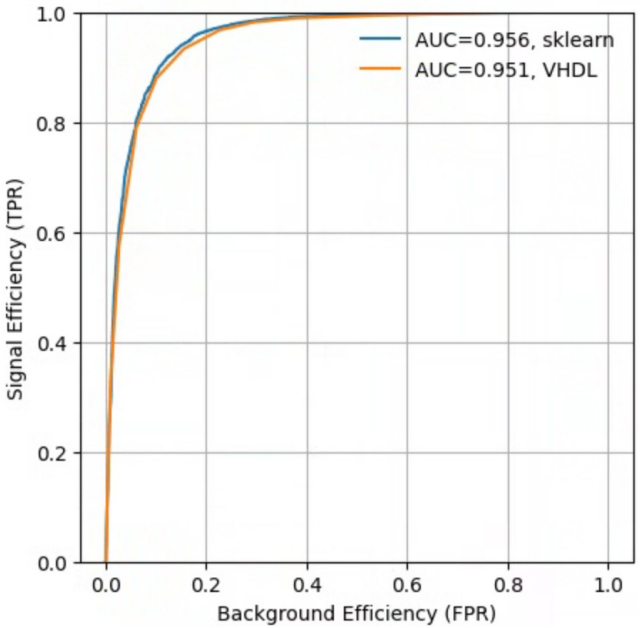


- **LRX:** 1 point at TDC + 2*X points at left and right.
  - Total 1 + 2*X features
- **24**: All points of the entire window.
- **25**: All points of the entire window and the position of TDC.

HLS by Conifer

- We use Conifer to performance inference of BDT in FPGA based on HLS.
  - Afterquantization, the HLS model has almost the same poerformance as the scikit-learn moedl.

- In the model for LR2 BDT, I am using
  - N of estimators = 15, depth = 3.

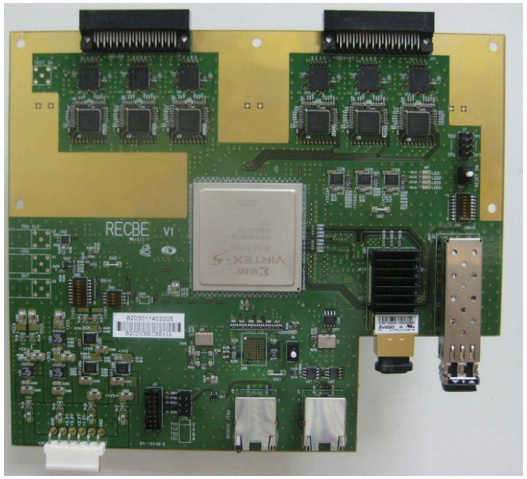


Implementation in FEE FPGA

- The FEE device of Belle II CDC, including the upgraded version with new ASIC and FPGA.

- The present BDT HLS model consumes 3.7K LUT and 1.6K FF by Vitis HLS.
  - For the present FEE (Virtex-5), it is still using Xilinx ISE without HLS tool. Plain HDL on BDL is needed.
  - Further optimization on the model will be done to reduce the resource and to realize chanel-by-channel BDT implementation.

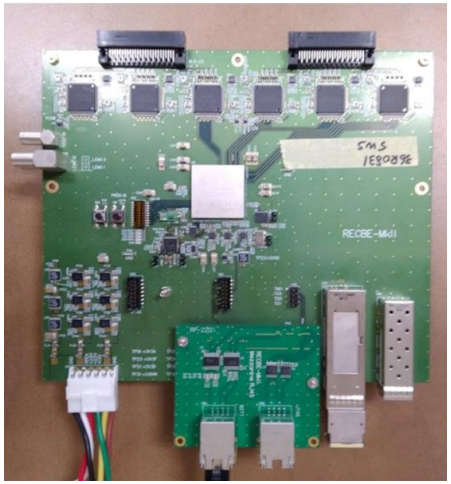
Present FEE:
Xilinx Virtex-5



LUT: 97,280
FF: 97,280
DSP: 128

At most 32 BDT

Upgraded FEE:
Xilinx Kintex-7 (Under study)



LUT: 203,800
FF: 407,600
DSP: 840

At most 67 BDT

Summary & To do

- In the Belle II CDC detector, the cross-talk noise frequently occurs and causes high fake track rate in Level-1 trigger.

- Based on the concept of AI/ML in FEE, we are working on an approach of implementing small-scale ML in the FEE FPGA as a waveform filter.
  - So far, NN and BDT are tested.
  - Effective reduction on the cross-talk noise is observed.
  - More studies on the model building, optimization, and inference in FPGA will be performed.

- In Belle II, we are also trying to promote such a concept of AI/ML in FEE.
  - Many potential application in such design of channel-by-channel small-scale ML on waveform.
  - More application on the other detectors are also under planning.