Introduction to eFPGAs and Their Application to High Energy Physics

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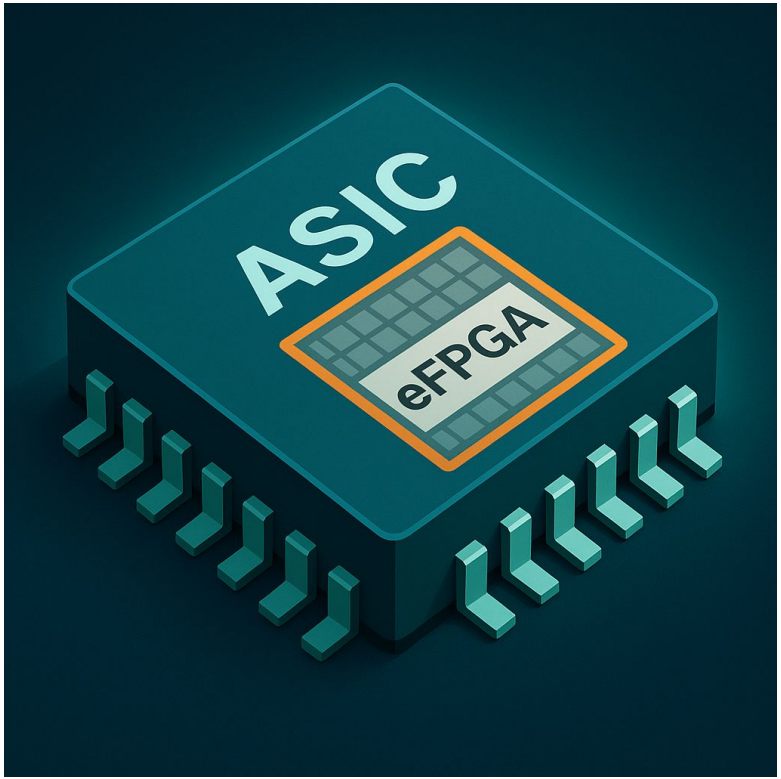
SLAC NATIONAL ACCELERATOR LABORATORY

What is an embedded FPGA (FPGA)?

- An IP core integrated programmable logic into an ASIC or SoC
- Provides **FPGA-like flexibility** within ASIC or SoC designs
  - Enables post-manufacturing updates and feature changes
- Can be used for hardware acceleration, security, AI/ML, or protocol adaptation
  - Speeds up critical functions or adapts to evolving standards



Rise of the eFPGA Open Source Frameworks

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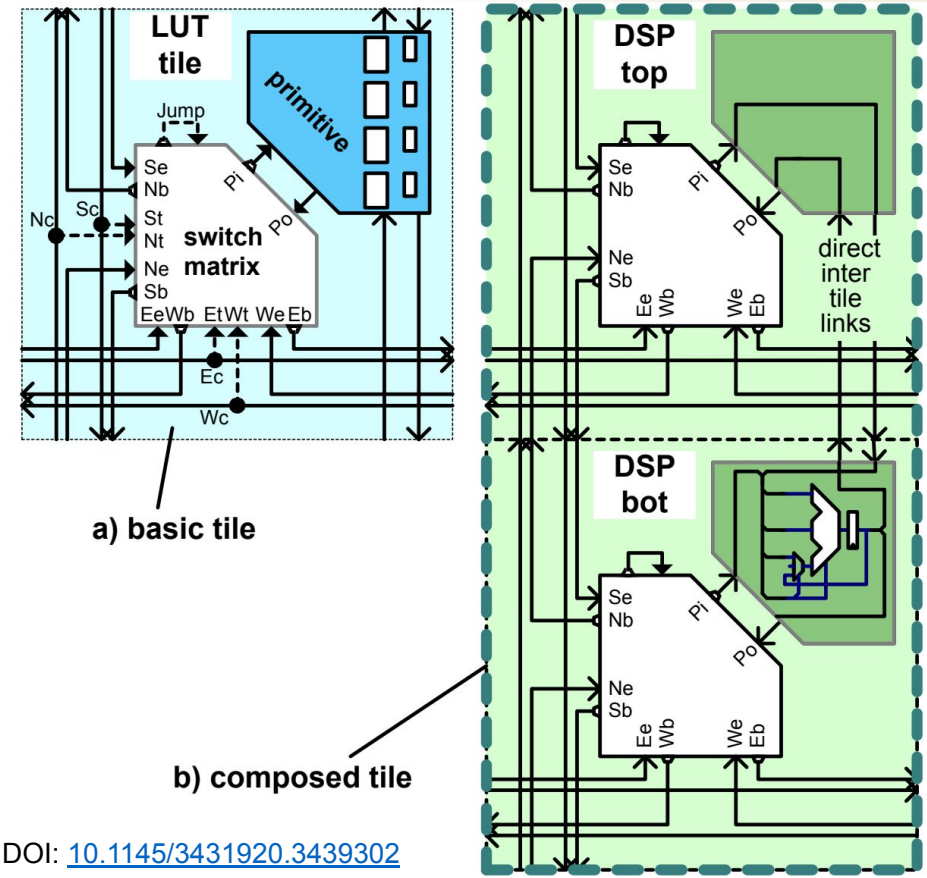
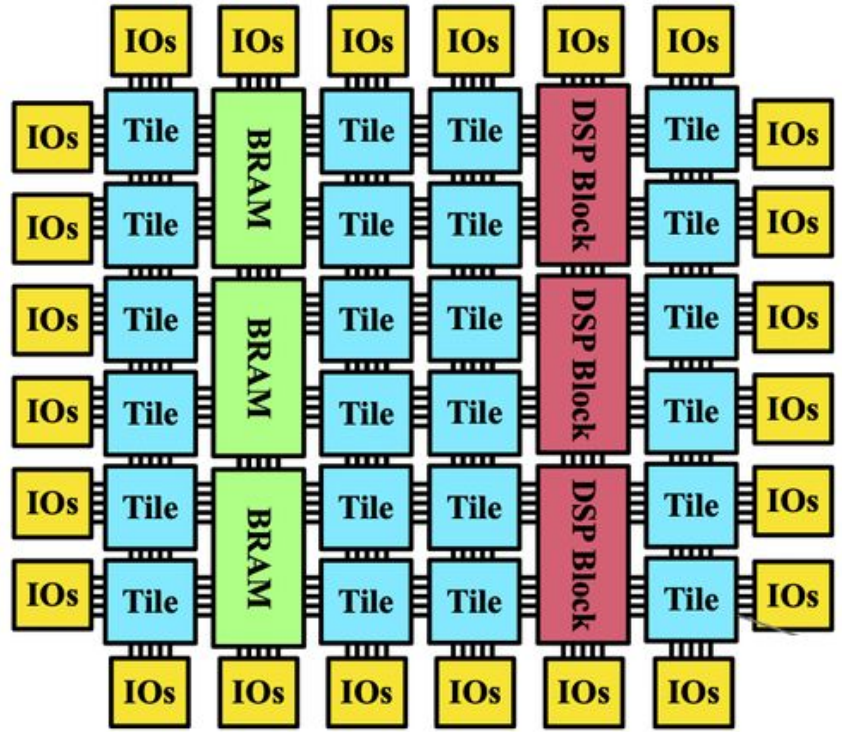
- Mature FPGA architectures are now **20+ years old**
  - Includes Spartan-3 and Virtex-II FPGAs from AMD/Xilinx
- Key patents on FPGA logic and architecture have **expired**
- Emergence of open-source eFPGA toolchains
  - Tools like **FABulous** and **OpenFPGA**
- **Lower barrier to entry** for startups and academia
  - Flexible, royalty-free alternatives to commercial eFPGA IP

What does a custom eFPGA architecture look like?

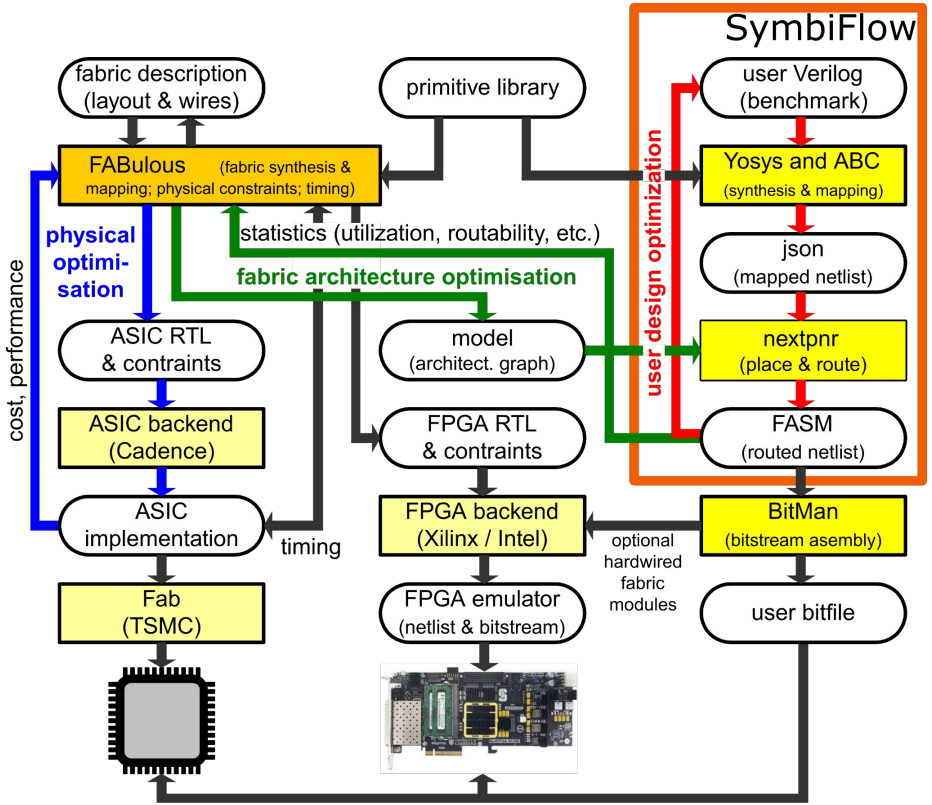


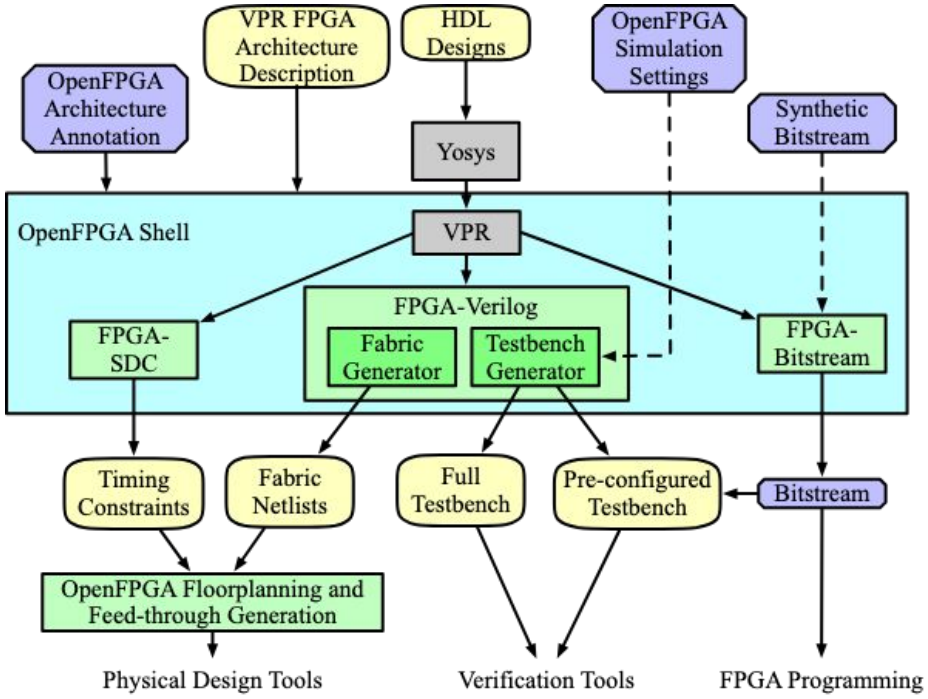


DOI: 10.1145/3431920.3439302

DOI:10.1109/MM.2020.2995854

How to Program Open Source eFPGAs?

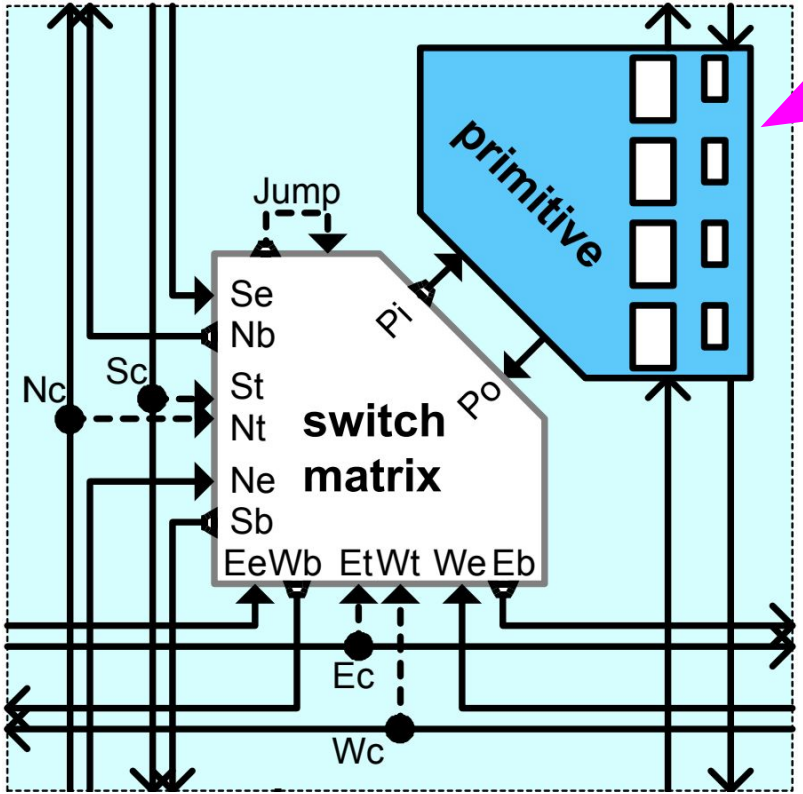




https://fabulous.readthedocs.io/

https://openfpga.readthedocs.io/

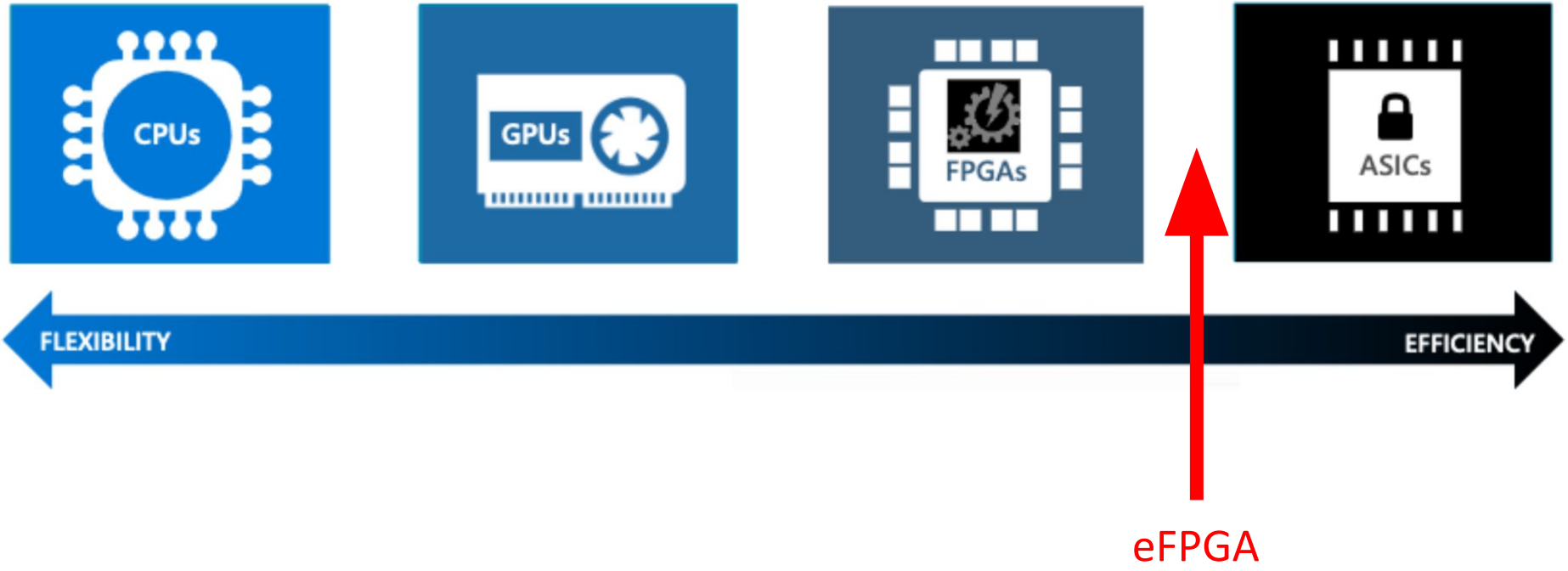
What can go into the custom primitive?



YosysHQ/**yosys**

Yosys Open SYnthesis Suite

When does an eFPGA make sense?



Why eFPGAs for HEP?

Future energy frontier colliders (EIC, FCC, muC) will face key front-end detector challenges:

- **High granularity** → Drives **high data rates**
- **Tight spatial constraints** → Requires **low material usage and low power consumption**
- **High radiation exposure** → Demands **custom, robust electronics design**

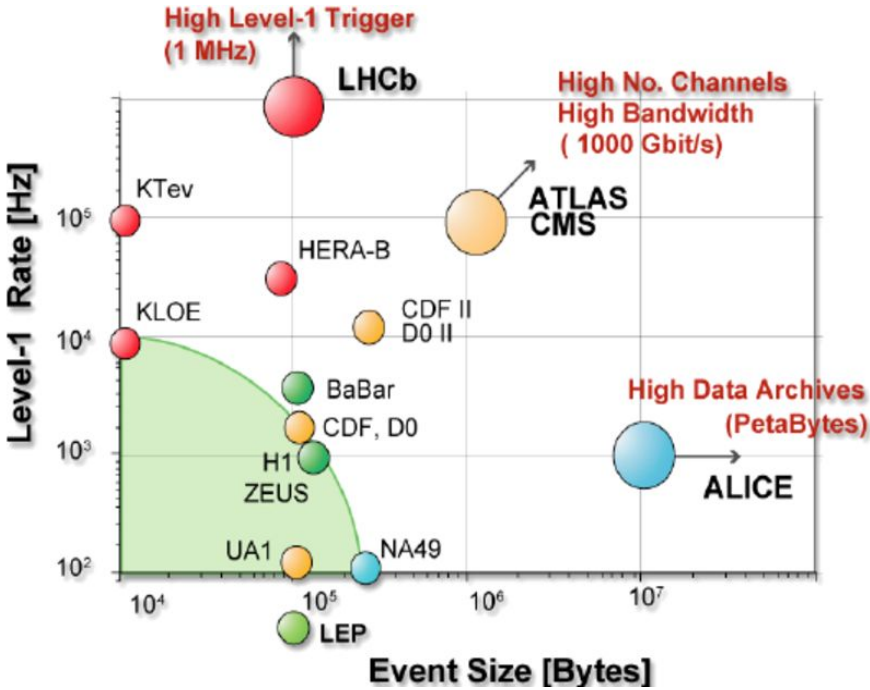
Key bottleneck:

Transmitting raw data off-detector is inefficient.

→ Solution: process data closer to the detector (at the front-end)

Role of eFPGAs with HEP:

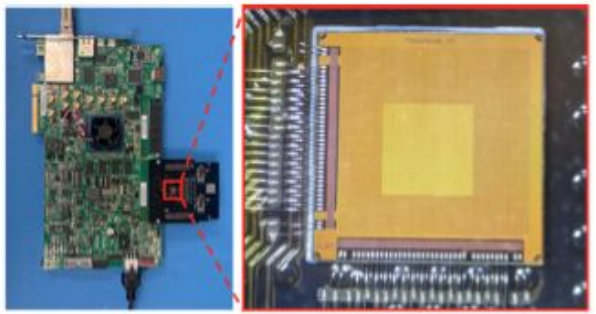
- Enable **intelligent, real-time filtering and feature extraction**
- Operate **at the source**, before data transmission
- Essential for managing:
  - Large data volumes (from high granularity)
  - High pileup
  - Signal efficiency in complex environments



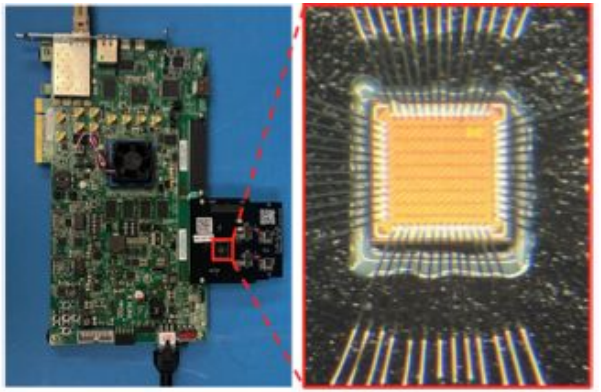
eFPGA Prototypes Efforts

- SLAC has successfully taped out two eFPGAs leveraging the open-source **FABulous** framework
  - 130nm & 28nm CMOS designs:
    - 8 x 8 tiles
    - Small logical capacity (~500 LUTs)

- "**Reconfigurable Pulse-Shape Discrimination Algorithm Implementations using eFPGAs**"
  - Talk by Carl Grace (LBNL)



130nm CMOS (SLAC)



28nm CMOS (SLAC)

J. Gonski et al 2024 JINST 19 P08023

Physics Test Case: Smart Pixel Readout

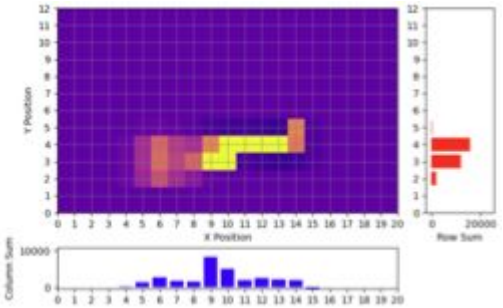
Goal: Perform inference on low-level pixel sensor data at the source

- Leverage Fermilab “smart pixel” dataset
- Train a ML model to identify high-pT tracks from pileup
- Compress and deploy the model to run on eFPGAs

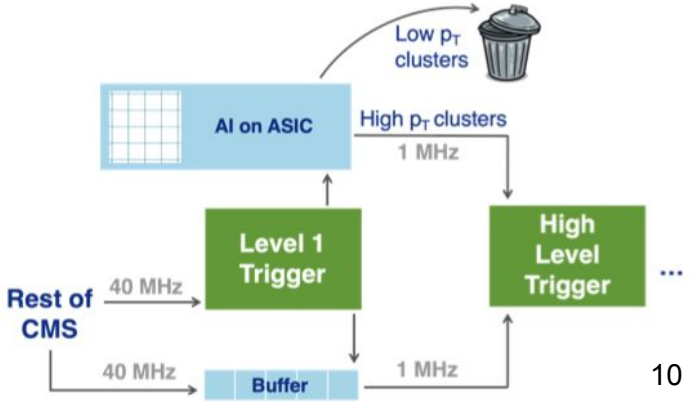
Proof of Concept:

- **Achieved**:
  - eFPGA running a Boosted Decision Tree (BDT) classifier
  - Matched quantized software results with **100% classification accuracy**
- **Challenges**:
  - Background rejection still limited (~few %)
  - Current implementation is small (310 of 448 LUT4AB cells)
  - **Next step**: Scale up logic capacity → requires **more eFPGA tiles**

- **“Application to colliders: Smart Pixels”**
  - Talk by Lindsey Gray (Fermilab)



“Smart pixels with data reduction at source”



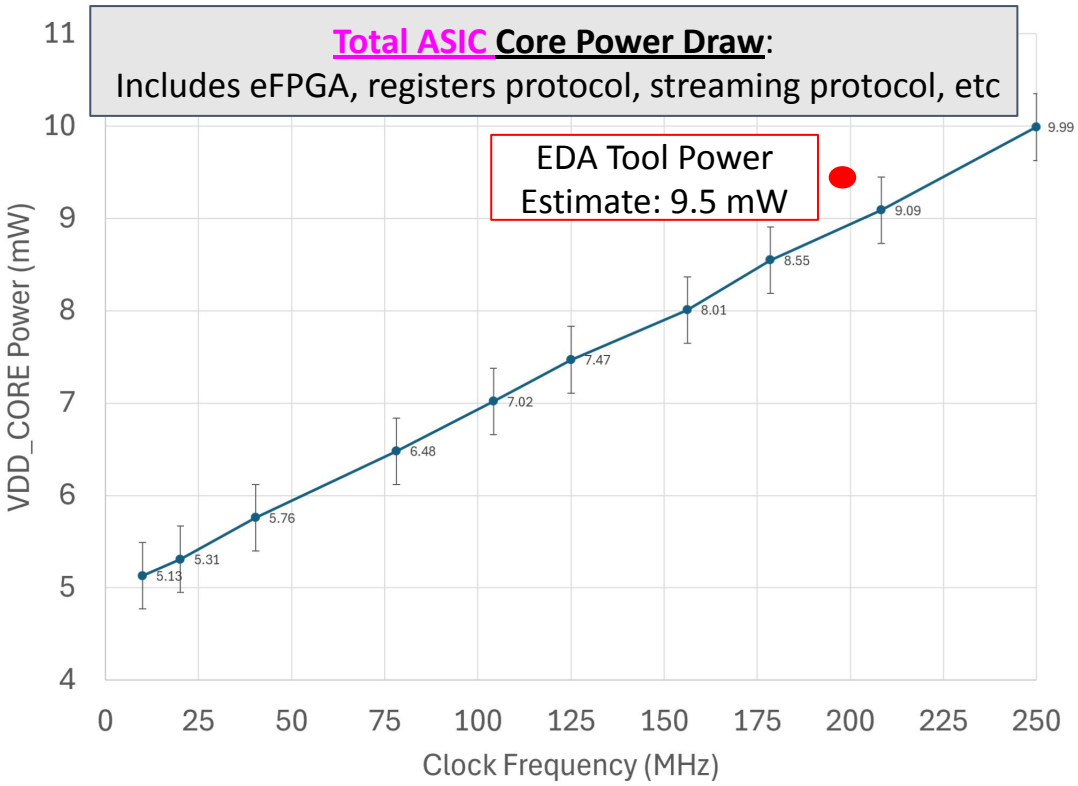
28nm eFPGA Power Measurements

Assuming 50 MHz eFPGA clock and current design:

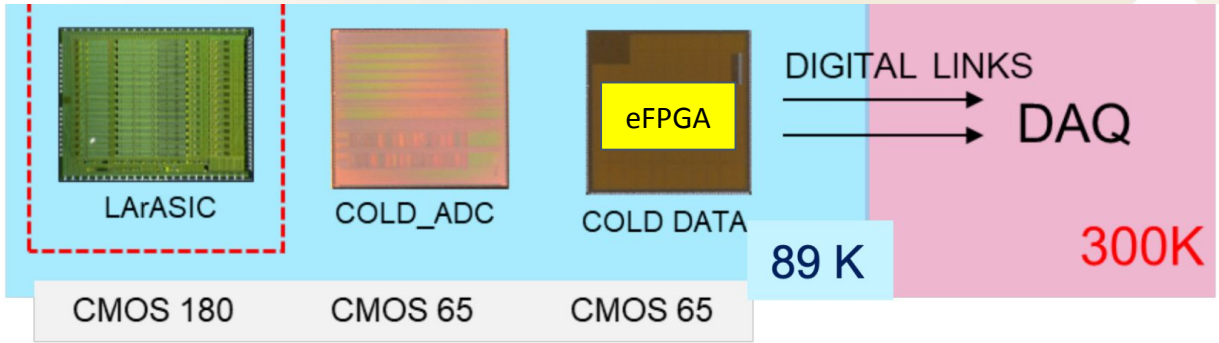
- EDA tool Power Estimate of **eFPGA only:**
  - 3.7 mW
- **1.8W/cm2**
  - = 3.7mW/0.002025cm^2

- E.g. FCC-ee electronics will need extremely low power density
  - Vertex - O(20 mW/cm^2)
  - Tracker - O(200 mW/cm^2)

- **Need to aggressively explore power optimization strategies** in a proper front end ASIC design
  - Not just “drag and drop” open source code with EDA tool auto-router

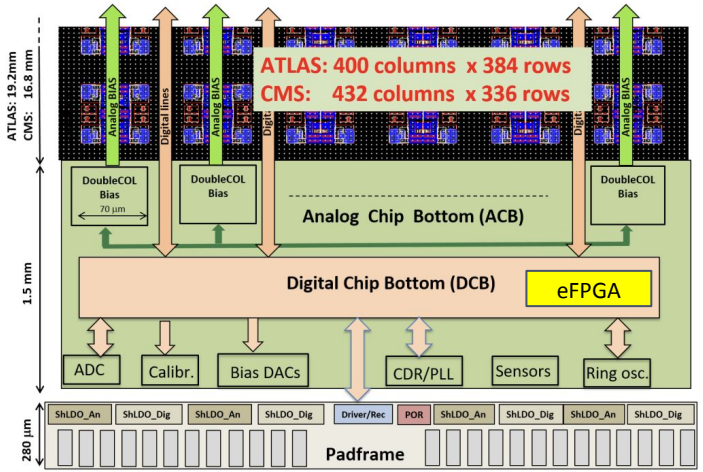


Possible HEP Configuration: Front End



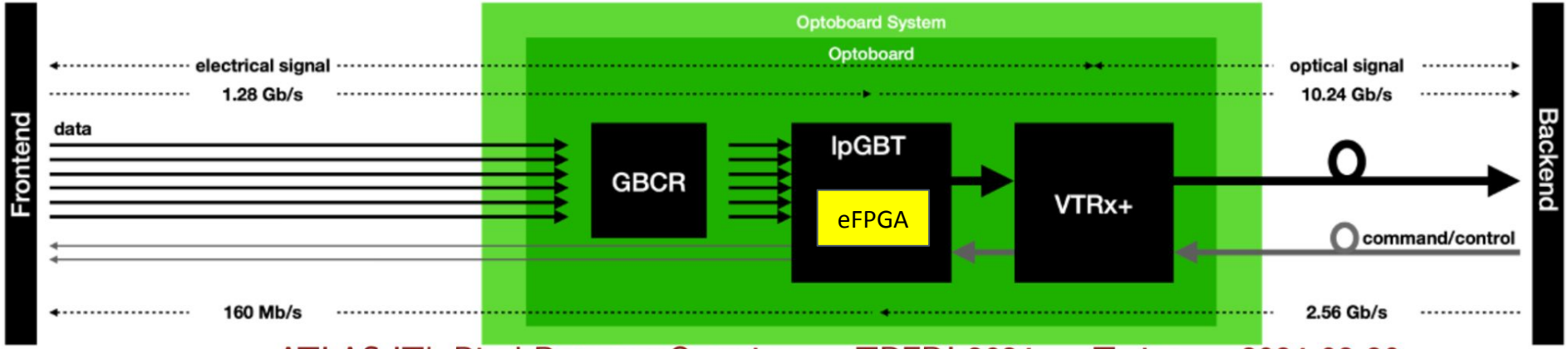
Mukim, P., *CHARMS250*, LIDINE 2024, CERN Indico, Aug. 2024

- Not advocating this for current DUNE or ITK designs
- Familiar HEP front ends to help illustrate the possibilities



https://cds.cern.ch/record/2890222/files/rd53cATLAS1v92.pdf

Possible HEP Configuration: Intermediate Stage



ATLAS ITk Pixel Detector Overview — TREDI 2024 — Torino — 2024-02-20

- Not advocating this for current ITK design
- But a intermediate architecture that people are familiar with

Future Work

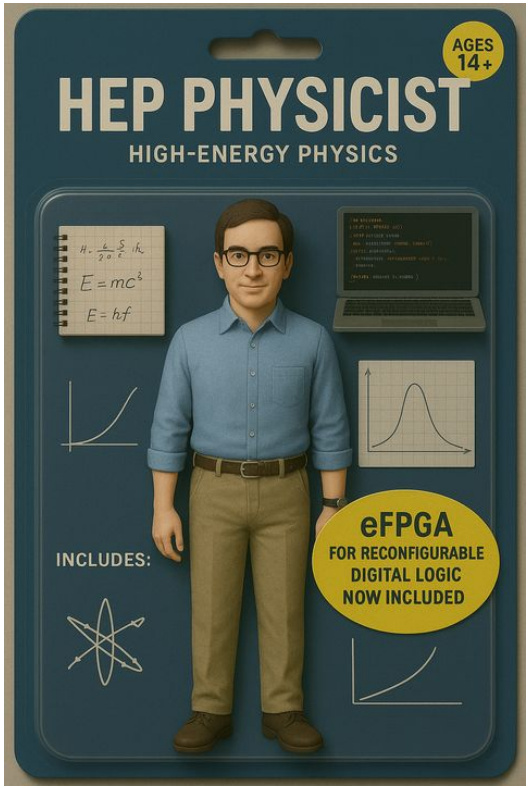
Proposal Submitted:
Hardware-Aware AI for HEP (NOFO#: LAB 24-3305)
"Enhancing Collider and Cryogenic Experiments with AI-Based Smart Detectors Using Reconfigurable Digital Logic and Analog Computing"

Collaborators:
- SLAC, LBNL, FNAL, University of Hawaii

Project Goals:
- Advance **eFPGA technology** for high-energy physics (HEP)
- Integrate **analog compute** with eFPGAs
- Develop **physics-informed co-design** approaches
- Perform **extensive testing in extreme conditions**
  - Focus on **radiation** and **cryogenic environments**
- Support **open-source tools** and **community outreach**

Summary and What's next?

- eFPGA have the potential to be a **very powerful tool** in future HEP experiments
- Initial eFPGA prototyping show promise but **require scaling and potentially power optimizations** for practical HEP applications
  - Investigation ongoing into application to Future Circular Collider/Higgs factory detectors: dual readout calorimeters, drift chamber trackers, …
- **Lots of opportunities** for the HEP community
  - Optimize eFPGA for area and power efficiency (key for FCC and front-end systems)
  - Collaborate with Yosys to enhance behavioral RTL inference for new custom primitives
  - Expand knowledge and community outreach



Acknowledgement

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Back Up

Custom 8 x 8 Tiles eFPGA Configuration

- Area = 0.002025 cm^2

- **LUT4AB Tile:**
  - A logic cell comprising a Look-Up Table (LUT) with 4 inputs and a Flip-Flop (FF)

- **(DSP_top & DSP_bot) Tile Pair:**
  - Digital signal processor (DSP) primitive, providing 8x8 multipliers with 20-bit accumulators

- **Total Resources:**
  - DSP: 4
  - LUT4AB: 448
    - LUTFF: 194

```
Info: Device utilisation:
Info:            FABULOUS_LC:   310/  448    69%
Info:   InPass4_frame_config:    32/   32   100%
Info:  OutPass4_frame_config:    48/   48   100%
Info:                MULADD:     0/    4     0%
Info:          Global_Clock:     1/    1   100%
Info:          FABULOUS_MUX2:    0/  224     0%
Info:          FABULOUS_MUX4:    0/  112     0%
Info:          FABULOUS_MUX8:    0/   56     0%
Info:          Config_access:    0/   16     0%
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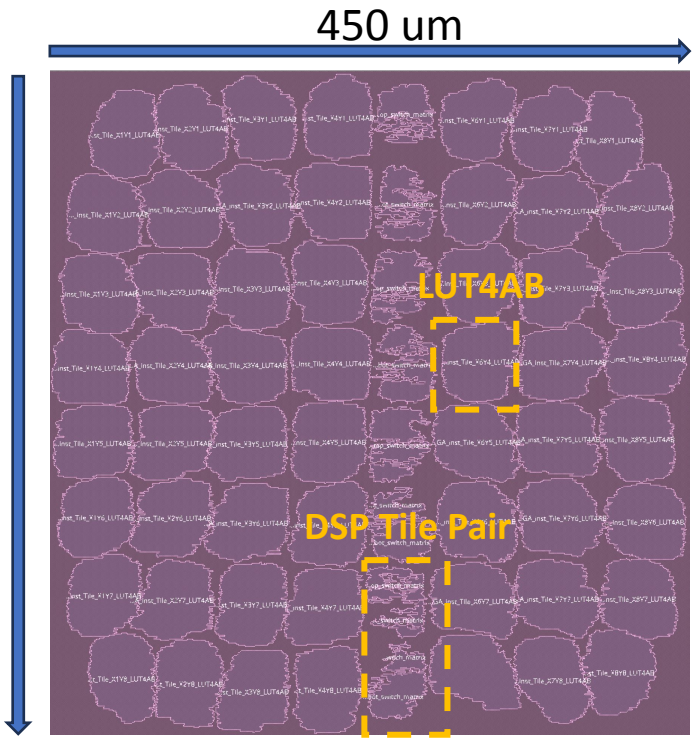

Screenshot from ASIC PnR tool