# **Fast Machine Learning Inference** for Scientific Discovery

### Particle Physics Seminar, University of Hawaii, Manoa March 28, 2024



Elham E Khoda

Data-Driven Discovery



# **Standard Model of Particle Physics**



### Elham E Khoda



# **Physics Beyond the Standard model**



### **Big Questions**

**Nature of Dark Matter** 

Matter AntiMatter Asymmetry

**Origin of Neutrino Mass** 

**Origin of Flavor** 

**Evolution of the Early Universe** 



# Mediator to the Dark Sector

### **Standard Model**









### **Extension to the SM**





# How to search for such Mediators in Collider Experiments?



# Large Hadron Collider (LHC) and the ATLAS experiment

- World's largest and most powerful particle collider
- Collides protons bunches (~10<sup>11</sup> protons) spaced by 25 ns



cle collider s) spaced by 25 ns



# The ATLAS Experiment

### ATLAS is a general purpose detector



Elham E Khoda



# How to search for such Mediators in the ATLAS Experiment?

# **Dijet Final State**







# **Theory model-driven Discovery Regime**

# Model-dependent Search

Most sensitive approach for a particular new physics scenario  $\rightarrow$  Unlikely to probe a different scenario



**Elham E Khoda** 



# **Example: 2-jet final state**





### **Data-driven Discovery Regime**

# **Anomaly detection**

### Identify data with features that appear inconsistent with those of the majority of the dataset



Elham E Khoda

For HEP application: Interested in an ensemble of events rather than a single outlier



**Dilepton/ dijet / di-gamma invariant Mass** 



15

### **Resonant Anomaly Detection Search**

### **Assumption:** Signal is localized at least in one of the feature spaces (x) $p_{\text{signal}}(x)/p_{\text{background}}(x)$ is high







# **Increase Signal Sensitivity**



Reduce background keeping as much signal as possible



# VAE as density estimator



Elham E Khoda

Loss:  $L_{VAE} = (1 - \beta) \times L_{MSE} + \beta \times KL$ 





# Predict the background in the signal region







### Model the multiple observables in the sideband regions



# My Strategy to estimate the density





### Elham E Khoda

**Generative models (Generative Adversarial Network or Variational Autoencoder)** to estimate the densities





# Model background in the side-band





# Features in the SR



### Elham E Khoda





# **Compare Data and Prediction**







# Weakly Supervised Method

### Weakly supervised = noisy labels

Let's assume we have: Two mixed samples of events with no label information

### **CWoLa** (Classification Without Labels) method shows:

It is possible to train a classifier to distinguish red from green

Training on impure samples (different admixture) of S and B) is asymptotically equivalent of training on pure samples



**Bkg-dominated sample S** << **B** 



### Classifier

JHEP 10 (2017) 174





# Let's use Generative Models



Elham E Khoda

**Fast ML Inference for Scientific Discovery** 

Training on impure samples (different admixture of S and B) is asymptotically equivalent of training on pure samples









# How Fast Machine Learning contributes to such Scientific Discovery?

### ASIC

















# Are we storing them?

- New physics is clearly very good at hiding from us
- Depending on anomaly, we could have none left in recorded data



Elham E Khoda

**Fast ML Inference for Scientific Discovery** 

iding from us /e none left in recorded data





### More ML algorithms here?

**Fast ML Inference for Scientific Discovery** 

Elham E Khoda



### How to run an ML algorithm on FPGAs?

# What is an FPGA?

### Field Programmable Gate Arrays (FPGAs) are reprogrammable integrated circuits

- Contain many different building blocks ('resources') which are connected together as you desire
- Originally popular for prototyping ASICs, but now also for high performance computing

### Building blocks:

- Multiplier units (DSPs) [arithmetic]
- Look Up Tables (LUTs) [logic]
- Flip-flops (FFs)

[registers] - Block RAMs (BRAMs) [memory]











# What is an FPGA?

- Run at high frequency O(100 MHz)
  - Can compute outputs in O(ns)
- Low-level Hardware Description Language for programming Verilog/VHDL
- Possible to translate  $C/C++ \rightarrow Verilog/VHDL$  using High Level Synthesis (HLS) tools

### Building blocks:

- Multiplier units (DSPs) [arithmetic]
- Look Up Tables (LUTs) [logic]
- Flip-flops (FFs)

[registers] - Block RAMs (BRAMs) [memory]








# What is an FPGA?

- **DSPs** (Digital Signal Processor) are specialized units for multiplication and arithmetic
- DSPs are often the most scarce for NNs
- Faster and more efficient than using LUTs for these types of operations

#### Building blocks:

- Multiplier units (DSPs) [arithmetic]
- Look Up Tables (LUTs) [logic]
- Flip-flops (FFs)

[registers] - Block RAMs (BRAMs) [memory]





# What is an FPGA?

- Logic cells / Look Up Tables perform arbitrary functional operations on small bit-width inputs (2-6)
  - boolean, arithmetic
  - small memories
- Flip-Flops control the flow of data with the clock pulse

### Building blocks:

- Multiplier units (DSPs) [arithmetic]
- Look Up Tables (LUTs) [logic]
- Flip-flops (FFs)

[registers] - Block RAMs (BRAMs) [memory]





# Example: AMD Xilinx FPGA

#### AMD Xilinx VIRTEX UltraScale+ VU13P

- •12288 Multipliers
- •1.7M LUTs
- •3.4M FFs
- •95 Mb BRAM









 $\vec{x}_M$ 



Elham E Khoda



Credit: Dylan Rankin





Elham E Khoda









 $\vec{x}_M$ 



Elham E Khoda



Credit: Dylan Rankin







#### Elham E Khoda



# High Level Synthesis with Machine Learning (hls4ml)



Elham E Khoda





# High Level Synthesis with Machine Learning (hls4ml)



A software interface for implementing Neural Networks on an FPAG

- Supports many common layer like DNN, CNN, RNN, Graph NN etc
- Transformers were not implemented until December, 2023

#### All these ML algorithms could be used for several low-level tasks **Example:**

- Jet Energy Calibration
- Missing Transverse Energy reconstruction

<u>https://fastmachinelearning.org/hls4ml/</u> arXiv:2103.05579



# **Resource Limitation**

### **Regardless of toolkit**, FPGA size is the limitation of doing low latency ML

• Bigger FPGA  $\rightarrow$  more resources  $\rightarrow$  more computation  $\rightarrow$  larger networks

### AMD Xilinx VIRTEX UltraScale+ VU13P

- •12288 Multipliers
- 1.7M LUTs
- 3.4M FFs
- •95 Mb BRAM

### So efficient model design to reduce weights is crucial







# **Efficient Model Design**



#### Elham E Khoda

![](_page_46_Figure_4.jpeg)

Train a smaller model using a bigger model

![](_page_46_Picture_6.jpeg)

#### Neural Architecture Search

Finding the optimal model architecture

![](_page_46_Figure_9.jpeg)

![](_page_46_Picture_11.jpeg)

![](_page_46_Picture_12.jpeg)

# **ML Inference with FPGA**

#### **Tranformers**

![](_page_47_Figure_2.jpeg)

![](_page_47_Figure_3.jpeg)

EK et al, NeurIPS 2023, <u>arXiv 2402.01047</u>

**Recurrent Neural Networks** 

EK et al, Mach. Learn.: Sci. Tec. 4 025004

#### **Autoencoders and Variational Autoencoders**

![](_page_47_Figure_10.jpeg)

![](_page_47_Picture_12.jpeg)

# Example: Jet tagging

![](_page_48_Figure_1.jpeg)

**Fixed Set of variables** Dense Neural Network

> Variable sets Deep sets model

Images Convolution NN

Sequence of particles Recurrent NN, Transformers

> **Graphs** Graph Neural Network

![](_page_48_Figure_9.jpeg)

![](_page_48_Picture_10.jpeg)

# b-tagging with transformer model

### Identify b/c jets from light-flavored jets

Jets are treated as sequence of particles

![](_page_49_Figure_3.jpeg)

 Very effective for natural sequences (collection of particles)

![](_page_49_Figure_7.jpeg)

![](_page_49_Picture_8.jpeg)

# **Transformer Architecture**

![](_page_50_Figure_1.jpeg)

### No. of parameters ~9k

#### Note:

Positional encoding was not used for this model

• It is not crucial for this application

$$O_h = \operatorname{softmax}\left(\frac{\zeta}{\zeta}\right)$$

![](_page_50_Picture_9.jpeg)

![](_page_50_Picture_10.jpeg)

**T** 7

# Model performance: ROC

- All the benchmark models are trained using Keras + TensorFlow
- Weights and biases are represented by 32 bit floating point numbers

![](_page_51_Figure_3.jpeg)

# ing Keras + TensorFlow

![](_page_51_Picture_7.jpeg)

# Quantization

### **Quantization – Reducing the bit precision used for NN arithmetic**

#### Why this is necessary?

- Floating-point operations (32 bit numbers) on an FPGA consumes large resources
- Not necessary to do it for desired performance
- hls4ml uses fixed-point representation for all computations
  - Operations are integer ops, but we can represent fractional values

![](_page_52_Picture_7.jpeg)

# 0101.1011101010

fractional

width

**Example:** <20, 10> Total Integer Width

![](_page_52_Picture_17.jpeg)

# AUC after HLS conversion

# Relative AUC = $\frac{\text{HLS AUC}}{\text{Floating - point AUC}}$

 Post-training quantized Transformer models (with optimal precision) performs similar to the floatingpoint models

> **Best Config** Integer bits = 10 Fractional bits = 10

![](_page_53_Figure_6.jpeg)

![](_page_53_Picture_7.jpeg)

![](_page_53_Picture_8.jpeg)

# **Quantization Strategies**

![](_page_54_Figure_1.jpeg)

![](_page_54_Figure_2.jpeg)

### **Quantization-Aware Training**

- QKeras
- PyTorch (limited options)
- QONNX (in development)
- Bravitas

## **Post Training Quantization**

![](_page_54_Figure_12.jpeg)

## HLS Conversion

(hls4ml)

• TensorFlow (limited options)

![](_page_54_Picture_16.jpeg)

### **HLS** Conversion (hls4ml)

![](_page_54_Figure_19.jpeg)

![](_page_54_Figure_20.jpeg)

![](_page_54_Picture_21.jpeg)

![](_page_55_Figure_1.jpeg)

### PTQ = Post training Quantization QAT = Quantization-aware Training

![](_page_55_Picture_6.jpeg)

![](_page_55_Picture_7.jpeg)

# Implementation Details

- Pipelining the MHA into 4 stages
- •Using FIFOs for the data stream across stages to save the FF usage
- Enable parallel processing for multiple heads
- Applying reuse factor to optimized the resource usage for DSP, and other resources
- Using an optimized softMax layer in stage 3

**Single-head attention** 

$$O_h = \operatorname{softmax} \left( \frac{Q_h}{M_h} \right)$$

![](_page_56_Figure_10.jpeg)

![](_page_56_Picture_11.jpeg)

- Trade-off between latency and FPGA resource usage determined by the parallelization of the calculations in each layer
- Configure the "reuse factor" = number of times a multiplier is used to do a computation

![](_page_57_Figure_3.jpeg)

# Parallelization

![](_page_57_Picture_9.jpeg)

# **HLS synthesis: DSP and LUT usage**

- **DSP usage** as a function of **Total bit width** after HLS synthesis
- The Jumps correspond to DSP input width

![](_page_58_Figure_3.jpeg)

Elham E Khoda

#### Synthesized using Xilinx Kintex UltraScale **FPGA part:** xcvu13p-fhga2104-2L-e

![](_page_58_Figure_7.jpeg)

![](_page_58_Picture_9.jpeg)

![](_page_58_Picture_10.jpeg)

Reuse and clk	Interval (cycle)	Latency (cycles)	Latency(time)
R1 (6.577 ns)	49	269	2.077 us
R2 (6.215 ns)	65	449	3.467 us
R4 (4.723 ns)	100	768	5.853 us

![](_page_59_Picture_5.jpeg)

**Observed Inference Latency ~ 2-6** µs

![](_page_59_Picture_7.jpeg)

# **Transformer Models: beyond particle physics**

![](_page_60_Figure_1.jpeg)

Elham E Khoda

#### Transformer Models

![](_page_60_Figure_5.jpeg)

Real-time Inference on Hardware

![](_page_60_Picture_7.jpeg)

#### **Custom Hardware**

![](_page_60_Picture_9.jpeg)

#### Custom Chip: ASIC

![](_page_60_Figure_11.jpeg)

![](_page_60_Picture_13.jpeg)

![](_page_60_Picture_14.jpeg)

![](_page_60_Picture_15.jpeg)

# One Possible Method: Autoencoder

### Autoencoders or Variational Autoencoders

- Reconstruction loss between input and output could be used as anomaly score
- CMS is already using this idea in their Run-3 trigger

![](_page_61_Figure_4.jpeg)

Elham E Khoda

### output could be used as anomaly score in-3 trigger

![](_page_61_Figure_8.jpeg)

![](_page_61_Picture_9.jpeg)

# Latent Factor Analysis via Dynamic Systems (LFADS)

### LFADS is a sequential model based on VAE

- •LFADS assumes the observed spikes are samples from a Poisson process with firing rates
- Decoder learns the firing rates a function of time
- Training objective: Decoder is trained to infer a reduced set of latent dynamic factors

![](_page_62_Figure_5.jpeg)

Elham E Khoda

![](_page_62_Figure_10.jpeg)

![](_page_62_Picture_11.jpeg)

![](_page_62_Picture_12.jpeg)

![](_page_63_Figure_1.jpeg)

• High Luminosity LHC (HL-LHC) in ~2029:

• 4 times the current data taking rate

Shutdown/Technical stop

Commissioning with beam

Hardware commissioning

Protons physics

Ions

# **Future of the LHC**

NDJFMAMJJASONDJF		2033										2034								2035									2036												2037										20						0																									
LS4	ND	D	J	F	= N	4	Α	Μ		J.	ןנ	A	S	50	)	N	D	J	F	١	1/	4	Ν	J	J	1	4	S	С	) [	۱I	D	J	F	P	1/	4	Μ	J	J	1	4	S	0	Ν		J	I	FN	٩	A	М	J	J	Α		50	DI	1	D	J	F	Μ	Α	۱M	1	ן	J	A	S	5	0	N	D	J	F	Ν	1/	4	М	J	J
																		52	1																																								F	R	u	n	5	5																		

![](_page_63_Picture_8.jpeg)

### LHC

![](_page_64_Picture_2.jpeg)

**Fast ML Inference for Scientific Discovery** 

# 4x more collision rate

### HL-LHC

![](_page_64_Picture_7.jpeg)

![](_page_64_Picture_8.jpeg)

# **ATLAS HL-LHC Data Processing: Online**

![](_page_65_Figure_1.jpeg)

## **ATLAS detector upgrade:**

#### **Upgrade in Detector Readout**

• 10x faster data collection

• Better hardware in Level-O and EventFilter

#### Many subsystems will be upgraded to be compatible with high occupancy / trigger rates

![](_page_65_Picture_11.jpeg)

# Phase II ATLAS Trigger Overview

![](_page_66_Figure_1.jpeg)

#### Elham E Khoda

![](_page_66_Picture_5.jpeg)

# **Online Jet Energy Calibration in ATLAS**

- BDT based regression model to predict the truth energy
- Could improve several physics analysis like di-Higgs

### Work-in-progress

- Preliminary BDT model is synthesized using FwX tool
- 25 ns average Latency
- Minimal resource usage: ~1% LUTs

Synthesized using Xilinx Kintex UltraScale FPGA part: xcvu9p

![](_page_67_Picture_8.jpeg)

![](_page_67_Figure_13.jpeg)

![](_page_67_Picture_14.jpeg)

![](_page_68_Figure_1.jpeg)

Elham E Khoda

![](_page_68_Figure_5.jpeg)

![](_page_68_Picture_7.jpeg)

# **Application:** Neuroscience

## **UW demo:** Real time detection of neural states from high-density electrophysiology measurements to drive closed-loop manipulations

Motivation:

- Measure individual neurons
- But computations are performed by groups of neurons
- Auto-encoder models learn latent factors that seem to better capture the "computational units" in the brain
  - LFADs algorithm
- Don't have many tools to compute these in real time, •
- Will help us do experiments to test if they are meaningful computational units

![](_page_69_Picture_10.jpeg)

![](_page_69_Picture_11.jpeg)

#### Elham E Khoda

![](_page_69_Picture_15.jpeg)

- Increasingly possible to perform low latency inference of ML models
  - Also low-power, high radiation

 Many cases, ML offers improved performance over traditional algorithms

• Fast ML could help enable discovery!

• Applications in many fields, areas

Summary

#### Real-time Al mini-course at IEEE NPSS 2023 (Vancouver)

![](_page_70_Picture_11.jpeg)

![](_page_70_Picture_14.jpeg)

### Many thanks to my Collaborators!

# Thank You!
Extra Slides

### **General approach:**

each SoftMax output Si requires the calculation of the exponent of the difference between zj and zi, summed over all elements, and then inverted

**Modified approach:** 

Stage 1: **Element-wise exponent computation** 

Stage 2:

Sum of all the exponents -> Inverted using inverse look-up table -> stored in register

Stage 3: **Element-wise multiplication** 

# **Softmax Optimization**











Fig. 4. Block diagram of gFEX. FPGA A, B, and C are the same ultrascale FPGAs; the Hybrid FPGA is ZYNQ FPGA. The FELIX is a PCIe module designed for ATLAS System.

# gFEX: Phase I Trigger upgrade



# **Computing Chalenges in ATLAS**



### To preserve current physics:

• 4 times the current data taking rate

Lacking sufficient budget to sustain required computing



# **Closing the Gap**





## Heterogeneous Computing Model

### • Support for different type of hardware is becoming important

### **Direct Connection**

CPUs and GPUs are connected





- Simple support for mixed hardware
- Scaleable
- Throughput optimization for multiple-core





## **Summary: Transformers**

### Three benchmark cases

- **Binary classifier:** ~3.3k parameters 1. - Car engine anomaly detection with Ford time series data
- 2. **3-class classifier:** ~10k parameters - particle physics application
- 3. 4-class classifier: ~3.3k parameters - LIGO gravitational wave detection application

### **Other Future applications:**

Modeling Neural population Dynamics with **Transformer-based architecture** 







# What's Next? Transformers?

- Good for long sequences
- Potentially more useful for Gravitation Wave applications
- Using on LIGO signal background classification model

## **B-tagging Model 3-class classifier:** ~10k parameters Classify b/c/light jets



- Latency of 2-3  $\mu$ s



Involves a lot of large matrix multiplication

• Implemented the on an FPGA

• Successfully synthesize







# **Other Applications: LIGO and Neuroscience**

## **LIGO Gravitational Wave Experiment**



## **Neuroscience: Detecting brain activities**

**Real time inference based on neuron activities** 





### **Classification:** Signal, Glitch, Background







## **Generated Events Signal Region**



### Elham E Khoda



# High Level Synthesis with Machine Learning (hls4ml)









This is not a exhaustive list

Mostly from Physics

Elham E Khoda



# Large Hadron Collider at CERN

• World's largest and most powerful particle collider • Collides protons (most of the time) bunches (~10<sup>11</sup> protons in a bunch) spaced by 25 ns



## Four major experiments on the LHC ring: ALICE, ATLAS, CMS, LHCb

centre of mass energy 2011: 7 TeV 2012: 8 TeV **2015 - 18** : 13 TeV 2022 - 25:13.6 TeV 2028 -: High Lumi LHC

In this talk





# **The ATLAS Experiment**

### **General purpose detector**

### **Muon Spectrometer:** Four different detector technology

### **Calorimeter:**

Electromagnetic (Liquid Argon), Hadronic (Liquid Argon (endcap) & Tile (barrel))

Solenoid Magnet: 2.0 T

### **Inner Detector:**

Three different detector technology

- 1. Silicon Pixel
- 2. Silicon Strip
- 3. Straw Tubes: Transition Radiation Tracker (TRT)





## **Particle Reconstruction**

Particles are reconstructed combining signatures from different sub-detectors

**Electrons:** Inner detector track + calorimeter deposit

**Photons:** Calorimeter deposit

**Jets:** Inner detector tracks (charged), Calorimeters

**Muons:** Inner detector and Muon spectrometer tracks

**Neutrinos:** Cannot detect, mostly resolved using missing transverse energy





## **ATLAS Phase-II Data Processing**



• Usage of ML is growing over time

## Active R&D Further improvements driven by more complicated algorithms

Usage of GPUs will be beneficial for the future LHC Runs (after 2026)



## **ATLAS Phase-II Data Processing**



- ML has potential to improve physics performance in the trigger system
- Strict latency requirements:  $\mu$ s (ms) for Level-0 (Event Filter) For Level-0 trigger  $\rightarrow$  we need to run ML on FPGAs



## **ATLAS Phase-II Data Processing**



**LO Trigger** (hardware: FPGAs) – O(µs) hard latency • Typically coarse selections are applied

**Event Filter** (software: CPUs) – O(100 ms) soft latency

## **Offline** (software: CPUs)

• Full event reconstruction, bulk of machine learning usage in ATLAS/CMS

More complex algorithms (full detector information available), some BDTs and DNNs used



## **Example: Jet Classification**



## Perhaps an unrealistic example for L1 trigger, but lessons are useful



## Jet Classification: 5-class classifier

## **Five class classifier**

### **Sample:** ~ 1M events with two boosted WW/ZZ/tt/qq/gg anti-kT jets







Elham E Khoda

### **Fast ML Inference for Scientific Discovery**

### q/g background





# Jet-tagging ROC



Elham E Khoda



# **Jet-tagging ROC: Post Quantization**

### his4mi

## Used precision: <16,6> Integet bits: 6 fractional bits: 10



Elham E Khoda

**Fast ML Inference for Scientific Discovery** 



## Scan to find optimal precision



Elham E Khoda

## Scan fractional bits

Integer bits fixed to 6





# (Example) 5-class jet-tagging: DSP usage



Elham E Khoda



# (Example) 5-class jet-tagging: Timing





### **Recurrent Neural Networks**

- Designed to work with sequential data • Text, audio, video, strokes, etc
- RNNs have a state,  $h_t$ , that is updated at each time step as the sequence is processed
- Recurrence relation at every time step



# **Recurrent Neural Network (RNN)**





Output

Input

past memory

### **Implementation of RNN models:**

- LSTM (Long Short-Term Memory)
- GRU (Gated Recurrent Unit)



## LSTM vs GRU



- **3 gates:** Input, Output, Forget
- **2 States:** Cell state ( $C_t$ ) and Hidden state ( $H_t$ )



- **2 gates:** Update and Reset
- **Single** Hidden state  $(H_t)$
- Less number of matrix multiplications
- Faster to train





# **Gated Recurrent Unit (GRU)**







## **Benchmark Examples**

### **Three benchmark cases**

- **Binary classifier:** ~4k parameters 1. Identify top-quarks
- **3-class classifier:** ~60k parameters 2. Classify b/c/light jets
- 5-class classifier: ~130k parameters 3. QuickDraw dataset: differentiate between Bees, Butterflies, Mosquitos, Snails, Ants





### **QuickDraw dataset**





- All the benchmark models are trained using Keras + TensorFlow
- Weights and biases are represented by 32 bit floating point numbers









- point models
- Small performance degradation (< 5%) in the **GRU models** after quantization



Elham E Khoda

Post-training quantized LSTM models (with optimal precision) performs similar to the floating-

**Fast ML Inference for Scientific Discovery** 





# **HLS Synthesis (RNN): DSP Usage**

## • **DSP usage** as a function of **Total bit width** after HLS synthesis • The Jumps correspond to DSP input width



Mach. Learn.: Sci. Tec. 4 025004

Synthesized using Xilinx Kintex UltraScale FPGA FPGA part: xcku115-flvb2104-2-i







• RNN-based models could give good performance at trigger-level jet identification

Implemented LSTM and GRU layers inside hls4ml source code

- b-tagging cannot be done in ATLAS hardware trigger, but possible in CMS





Due to QCD confinement we do not see quarks in isolation  $\rightarrow$  only exists in confinement of a hadron

**Parton Shower** Cascade of gluons



Elham E Khoda

## Jets



Due to QCD confinement we do not see quarks in isolation  $\rightarrow$  only exists in confinement of a hadron

**Parton Shower** Cascade of gluons

Jets: Collection of particles



Collision

## Jets



Due to QCD confinement we do not see quarks in isolation  $\rightarrow$  only exists in confinement of a hadron

**Parton Shower** Cascade of gluons

Jets: Collection of particles

**Jets** are experimental signature of quarks and gluons



Collision

## Jets

108
# Structures within jets

#### **QCD jets** Could have different substructure







109

## **High Momentum Particles**





110

### **B-hadrons have measurable lifetime**

- Creates displaced vertex
- Important quantity to identify b-jets



# **B-jet tagging**





# **Physics Beyond Standard model**



The Standard model does not describe the major portion of 5% the universe 68% Dark energy



