SCIPP
SANTA CRUZ INSTITUTE FOR PARTICLE PHYSICS
UC SANTA CRUZ

Ultrafast semiconductor sensors and electronics in particle physics

Utilizing ML/AI for 4D/5D Tracking Detectors

Jennifer Ott

University of Hawai'i at Manoa, March 12-13 2024

Outline

- **Personal introduction**
- **Semiconductor sensors and thin film technology**
  - Oxide thin films as coupling dielectric and surface passivation
  - Thin film materials for charged particle tracking?

Research motivation & background

- **Precision tracking and timing in particle physics**
  - Tracking detector upgrades
  - Sensor development for timing detectors

Current and potential future research directions

- **Towards 4D (5D) Tracking**
  - Physics motivations
    - *Nuclear physics, precision measurements, flavor universality: EIC, PIONEER, …*
    - *Energy frontier: future colliders*
    - *Non-collider science*
  - Sensor and electronics development
  - Machine Learning / AI across 4D/5D Tracking
- **Collaborative and funding environment in the US and international particle physics community**

Introduction

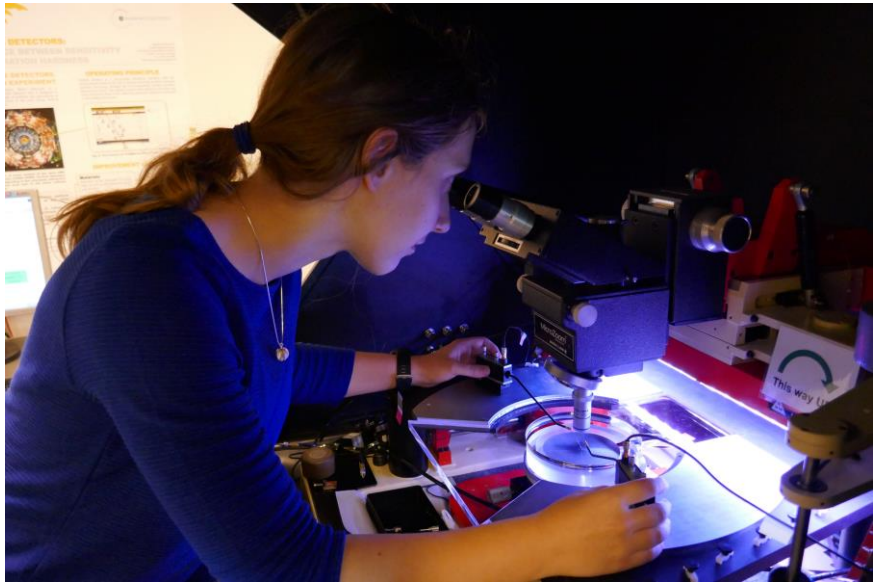
Jennifer Ott

B.Sc., University of Helsinki, chemistry (2014)
M.Sc. University of Helsinki, radiochemistry (2015)

D. Sc. (Tech.) Helsinki Institute of Physics & Aalto University (spring 2021)

Development, processing and characterization of silicon pixel and timing detectors for the CMS Experiment

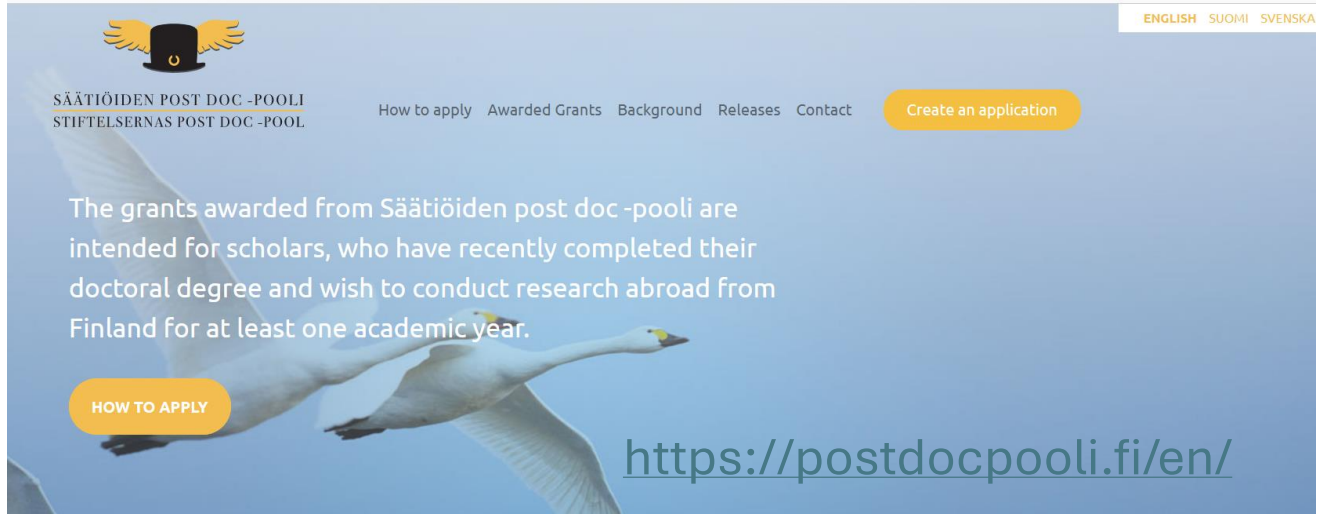
Especially: using thin films grown by atomic layer deposition in semiconductor detectors



Introduction

Postdoctoral researcher, Santa Cruz Institute for Particle Physics (SCIPP), University of California at Santa Cruz (September 2021 → present)

- *1st September 2021 - 31st August 2023: personal postdoctoral scholarship from the Finnish Cultural Foundation*



Research background

- Process development, fabrication, testing, characterization of diodes and pixel sensors using aluminium oxide thin films
- Towards using thin films as active sensor layers: leading sensor characterization for projects in collaboration with ANL, UCSC ECE department
- Electrical characterization of low-gain avalanche diodes for the CMS Phase-2 endcap timing layer upgrade
- Pixel module electrical testing, US cluster coordination for ATLAS Phase-2 Inner Tracker upgrade
- Member since L-o-I phase and initial proposal draft for PIONEER Experiment; one of the fast sensor and electronics leads for the Active TARget detector; head of the conference and speakers committee
- Sensor testing with emphasis on charge sharing and capacitance characterization, radiation hardness for EIC-ePIC time-of-flight particle ID subsystem; characterization of fast analog preamp and digitizer chip as alternative readout ASIC path

Overview of planned research

Fast readout electronics, fast sensor development for time-of-flight particle ID layer

- **Electron-Ion-Collider / ePIC Detector**
- ***Belle-2 Upgrade? Time projection chamber has been proposed, would not be feasible without a timing layer***

Fast readout electronics, fast sensor development, simulation, reconstruction for 4D/5D tracking of charged particles

- **PIONEER Active TARget detector**

ML/AI along the signal path, in front-end

- Signal classification based on digitized waveform
- t0 timestamp/trigger in connection with other detector layers
- Track trigger in high-occupancy environments
- 4D/5D track reconstruction

Radiation-hard sensors & electronics

- Radiation-hard fast sensor testing and development, fast & rad-hard (analog/digital) ASIC design

Transformative technology for charged particle detection

- Thin film detectors

Electronics projects

Challenge: electronics

Fast electronics:

- Reduction of jitter
- Time walk correction / CFD
- Fast digitization
- Low noise
- Low power consumption

Examples:

- **Waveform digitization - Varner Lab / Nalu: HD-SoC, HP-SoC**

- **Fast, low-power, low-noise SiGe bipolar CMOS: UniGe and Anadyne projects**

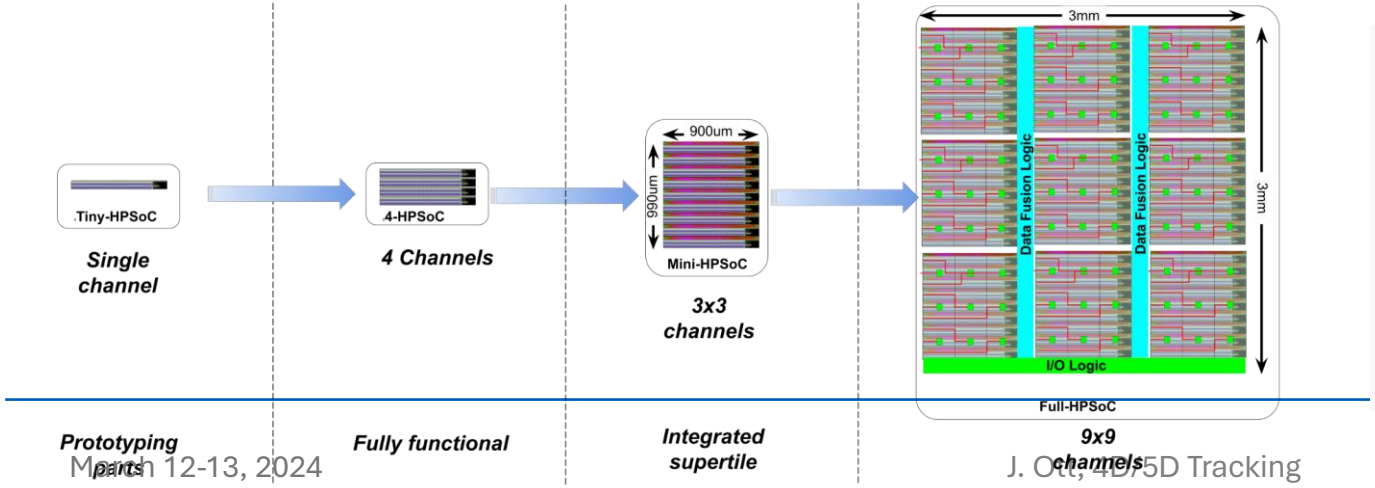
HP-SoC: specifications and targets

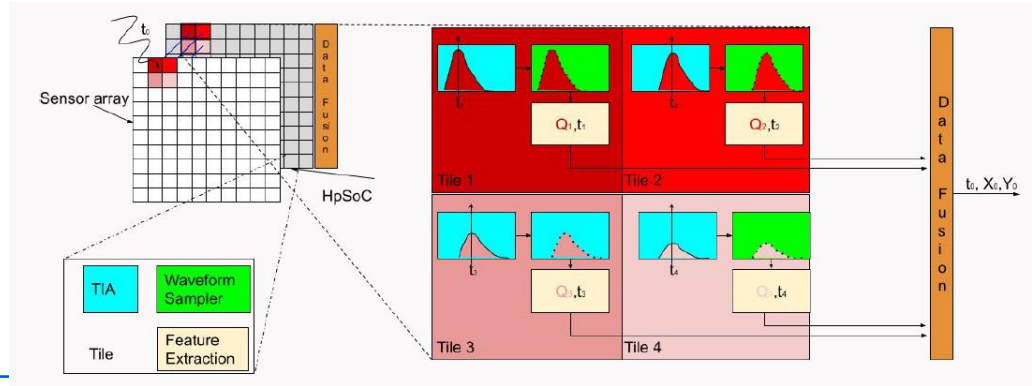
NALU SCIENTIFIC
ENABLING INNOVATION

65 nm TSMC CMOS

- Input preamplification handling fast current-based sensors (~100 ps rise times)
- Very large integration (100+ channels) with modular tileable, scalable structure
- Timing resolution (jitter) better than 10 ps, down to 5ps
- Waveform digitization of at least 10 Gs/s, allowing for pulse shape discrimination
- Autonomous chip triggering and storage virtualization
- On-chip feature extraction and multi-channel data fusion

HP-SoC CPAD presentation



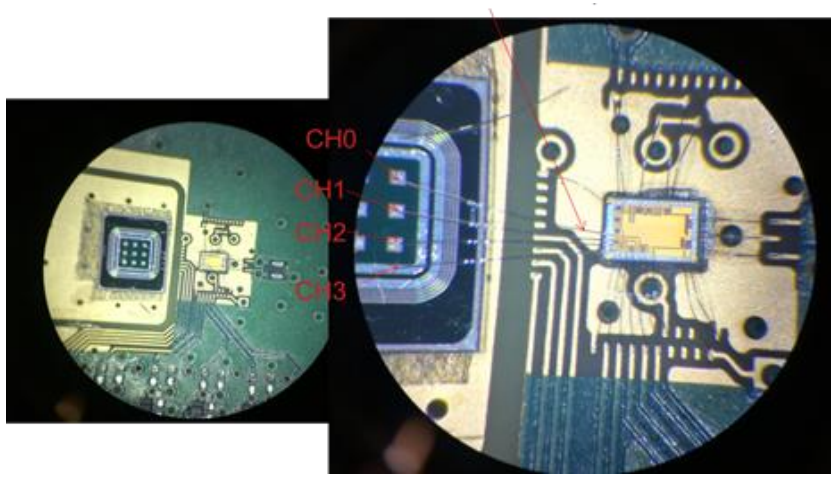


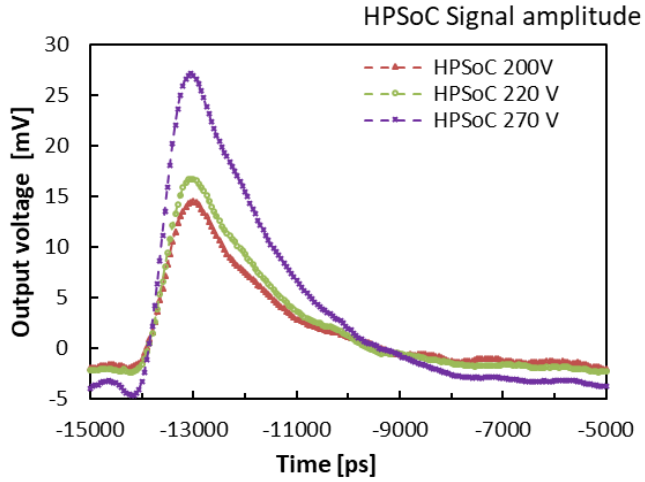
HP-SoC v1

First prototype developed, fabricated and tested through SBIR Phase-1 funding

- 4 channels, sampling array and conversion logic, digital control but limited functionality
- Focus on characterization on 1-ch transimpedance amplifier and gain stage with LGAD sensor

Reached 600 ps rise time and ~45 ps jitter: main issue was the lower than expected output signal amplitude = front-end gain





TWEPP 2022:
https://indico.cern.ch/event/1127562/contributions/4904727/

https://arxiv.org/abs/2210.09555v2

HP-SoC v2

Co-funded by FY23 EIC/Jefferson Lab Generic R&D grant

Optimized front-end design informed by the testing results from the initial prototype chiplet

- Improved TIA and gain stage: higher signal amplitude

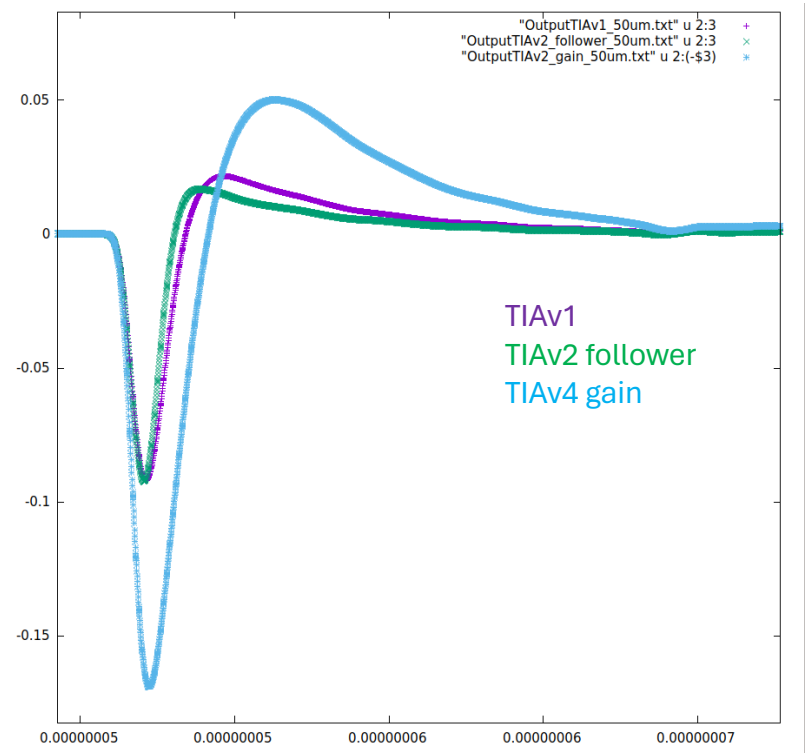
Independent front-end amplifier to permit separate evaluation of the analog performance

Full digitizer

New internal discriminator

On-chip autonomous operation via self-triggering

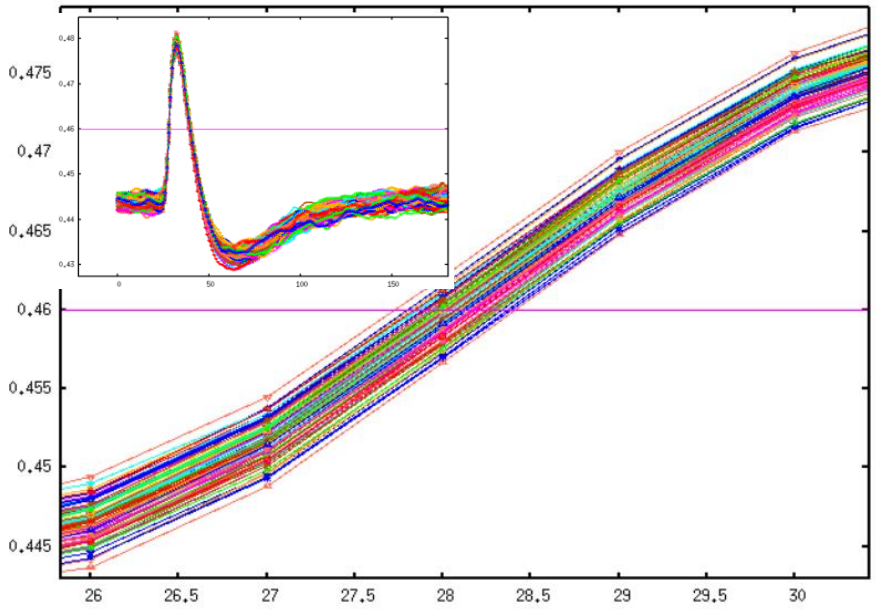
Chip submitted in May, received in September 2023

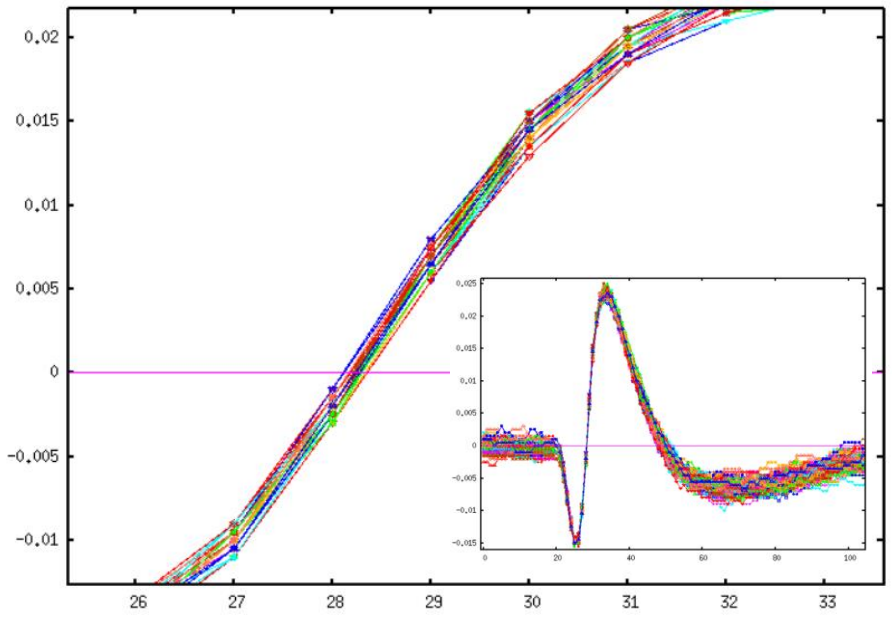


Waveform digitization

Waveform digitization at 10 GS/s (10-bit): allows digital baseline correction, constant fraction discrimination and other algorithms for improving jitter component of the timing resolution

- Simulated HP-SoC v2 output digitized waveforms with noise: estimated reduction from 13.7 ps (leading edge) to 5 ps
  - **Classification of digitized waveforms with machine learning?**

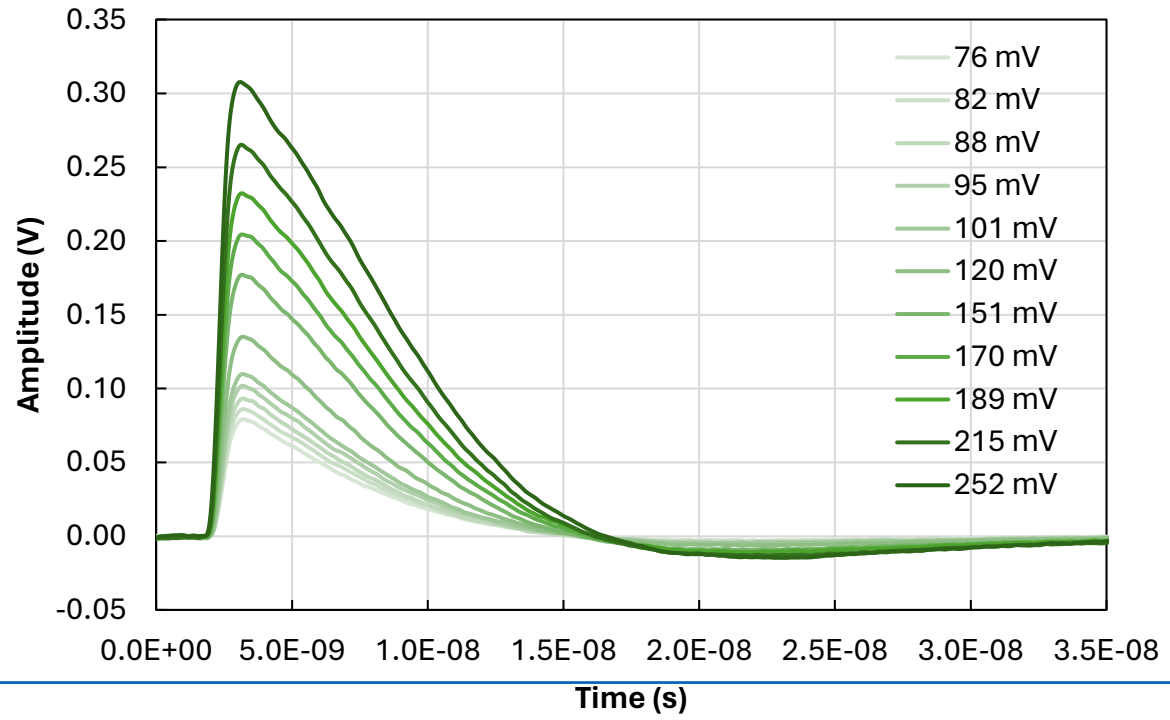


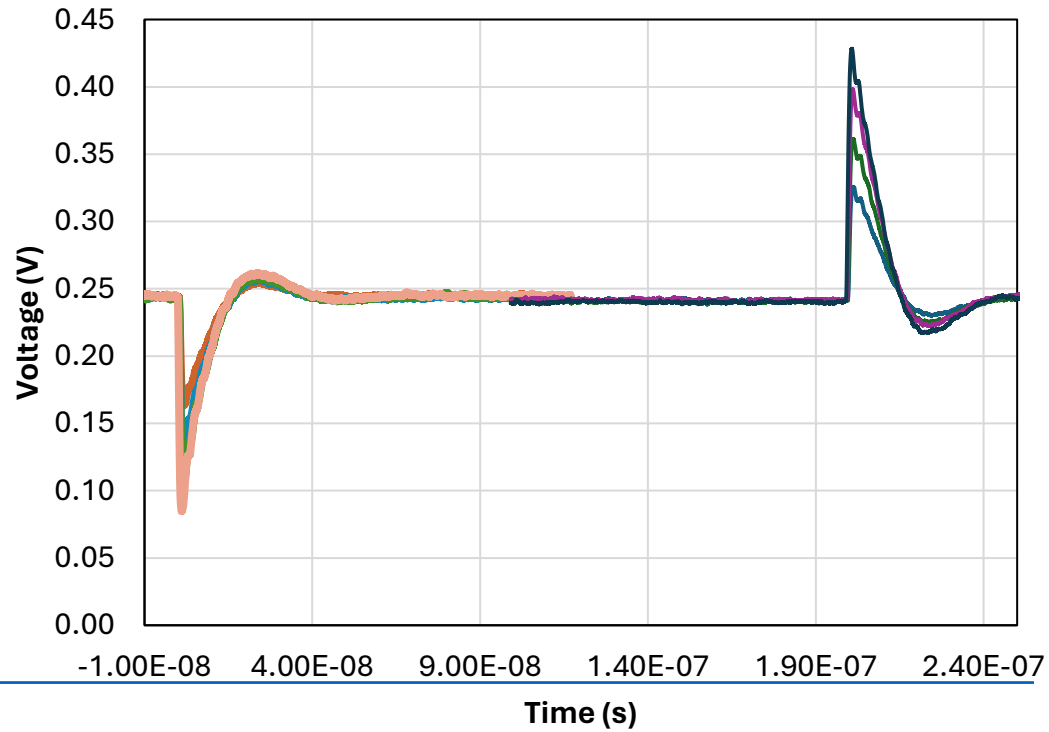


Calibration with external injection

After adjustment of transimpedance amplifier bias, signals of either polarity could be detected without reaching saturation

- On chip, triggering is targeting only the expected signal polarity from p-type sensors



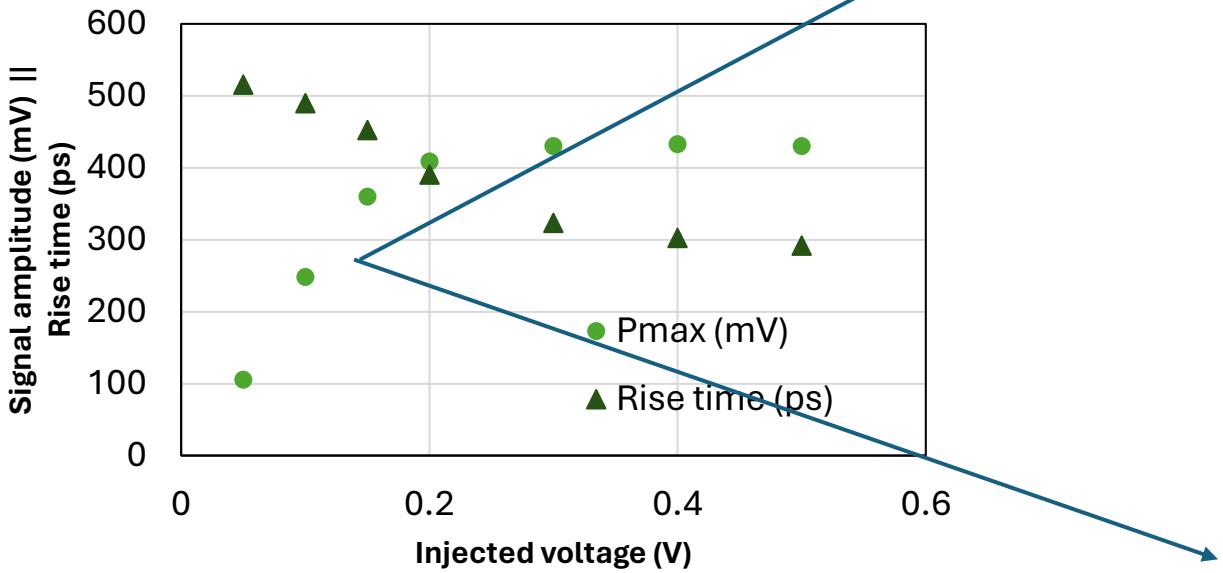


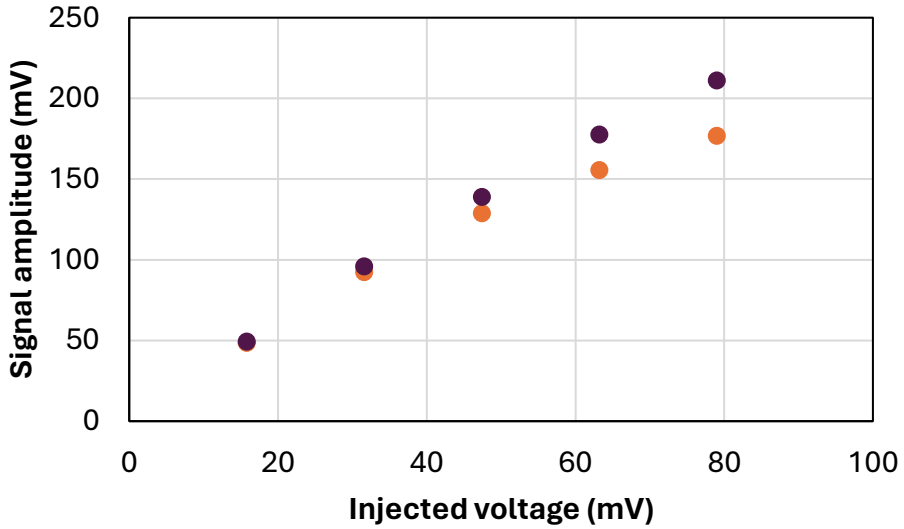
Calibration with external injection

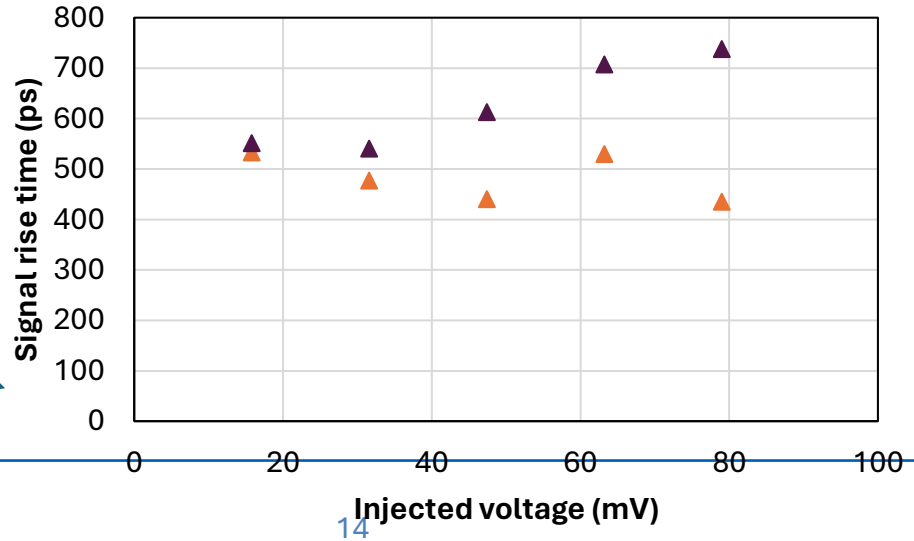
Signal linear up to ~200 mV = 100 fC

Gain (at highest setting) is improved significantly compared to v1

Rise times down to 450-500 ps!







Characterization with sensors

HPK AC-LGADs, 500 µm pitch

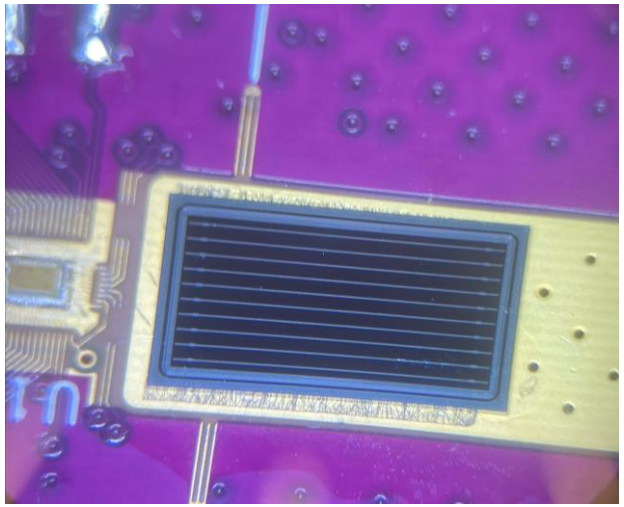
4x4 pad array, type C600, 50 µm thick, 300 and 450-µm pad size

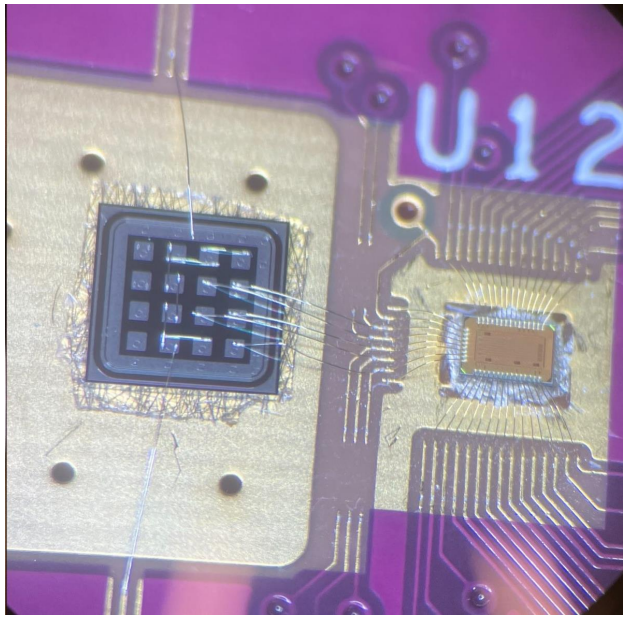
- Tested with laser and Sr-90 beta source

1 cm strip, 50 µm thickness, 50 µm metal width, type C600

- Tested with laser, tests with source to be done soon
- Noise: on the order of 2 mV – **has not degraded significantly with larger strip sensor capacitance**

Data acquired using GHz probe and oscilloscope connected to standalone TIA output – 3-4 channels are connected for full digitization, but were not read out yet

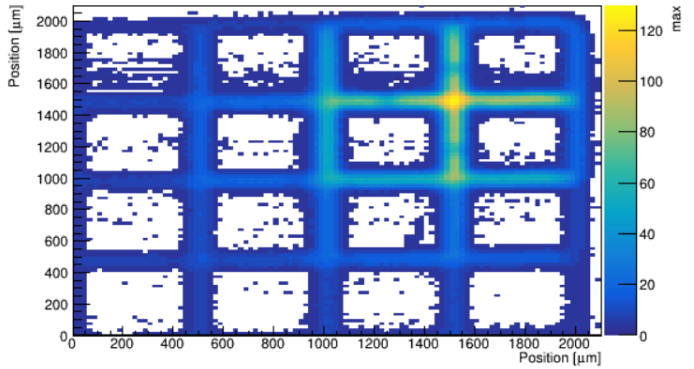


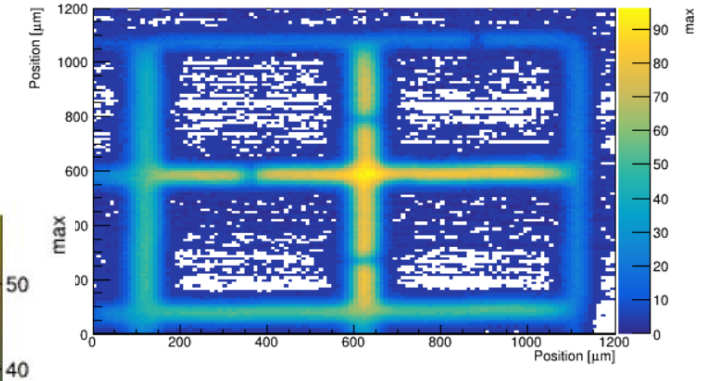


Characterization with sensors

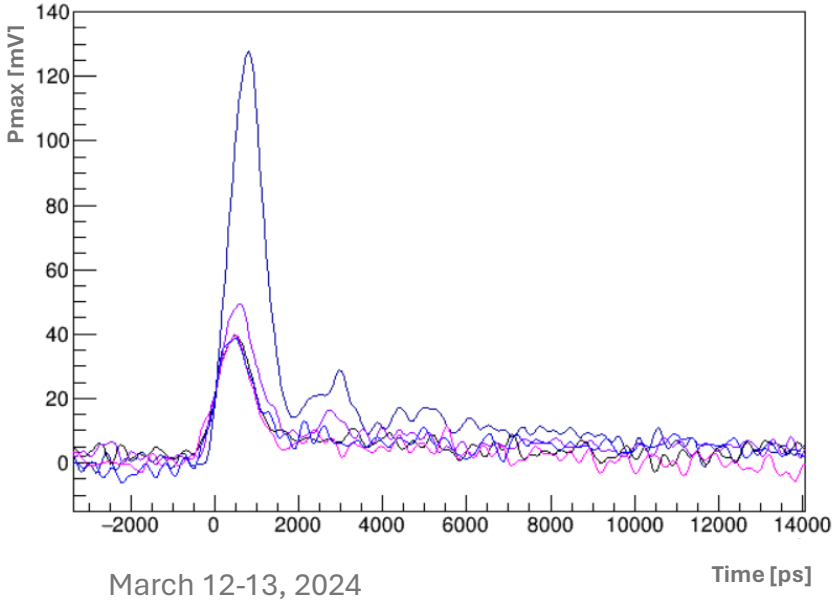
x-y scans of pad and strip sensors were conducted

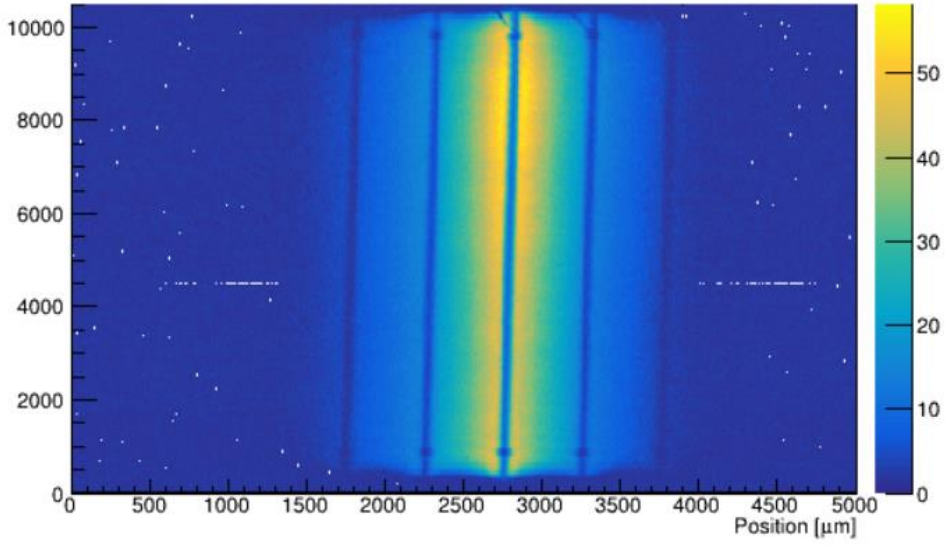
E.g. strip sensor: rise time 600-750 ps, jitter ~35 ps





Beta source exposure of pad sensor (self-triggered): MPV 40 mV, rise time 550 ps, noise rms 1.8 mV





Digitizer evaluation

So far operated only at Nalu with calibration input and/or supplied waveform

Firmware development finished recently

- Will be made available also at SCIPP for evaluation of the full system with sensor and multiple channels

Initial testing of internal delay line, internal conversion clock generation and counter, comparator, ramp has been conducted

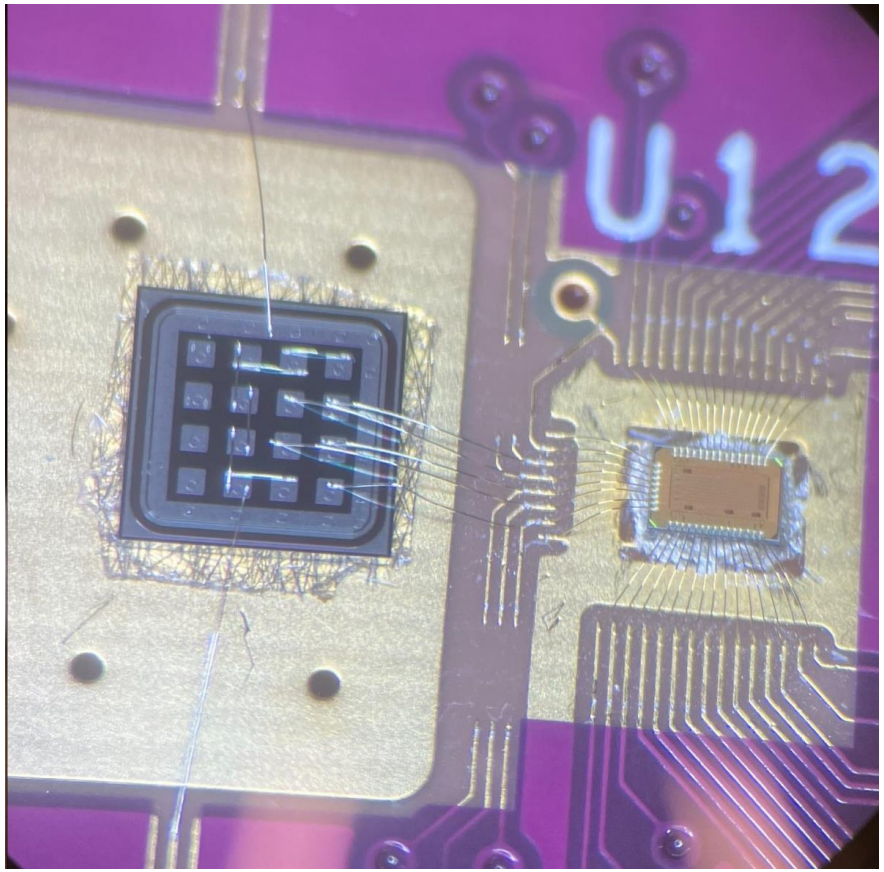
- Functional bug in joint control of ramp and counter prevents full internal conversion
- Planning to submit a corrected version of the chip immediately, at the end of the month

Alternative approaches still allow majority of chip testing, including pedestal acquisition and synchronous wave acquisition & conversion

Power consumption: 24 mW for 4 channels with full digitization + 1 additional TIA + clock. Adjustment not perfect yet – may reach closer to targeted 3.3 mW/channel

Recent project activities and updates

- Waveform digitization ASIC / Nalu LLC
- HP-SoCv2 received and tested in Fall 2023 – improved gain compared to v1, fast rise time, 4 channels with full digitization architecture and triggering.
  - Bug in digitizer (joint ramp and counter control) discovered, adjusted in immediate **follow-up production: expected for February 2024**
- Funding through Jefferson Lab EIC call renewed for coming year – fabrication of 3x3 ch HP-SoCv3



HP-SoC CPAD presentation

Conclusions

The second revision of HP-SoC has been designed and fabricated, incorporating most of the functionality envisioned for the final implementation

First results of testing with both calibration inputs and sensors are encouraging:

- Pre-amplification seems compatible with high performance readout of state-of-the-art LGAD sensors
- Most digitizer modules perform according to the specifications
- Functional errors precluding full architecture assessment are being addressed with additional testing of present and old prototyping and new fabrication
- Bug in digitizer (joint ramp and counter control) discovered, adjusted in immediate **follow-up production: expected for February 2024 – delivered past week**

Funding through Jefferson Lab EIC call was renewed for coming year → design and fabrication of 3x3 ch HP-SoCv3

HP-SoC v3: 9-channel module

- To utilize results from previous front-end and digitizer evaluation
- Optimization of feature extraction mechanisms based on acquired data
- Channel fusion information based on experimental data from multiple channels
- ***Explore options for ML/AI integration "readiness"?***

https://indico.jlab.org/event/751/contributions/13575/attachments/10453/15696/EIC-HPSoC%202023-24-%20response%20to%20reviewers%20(1).pdf

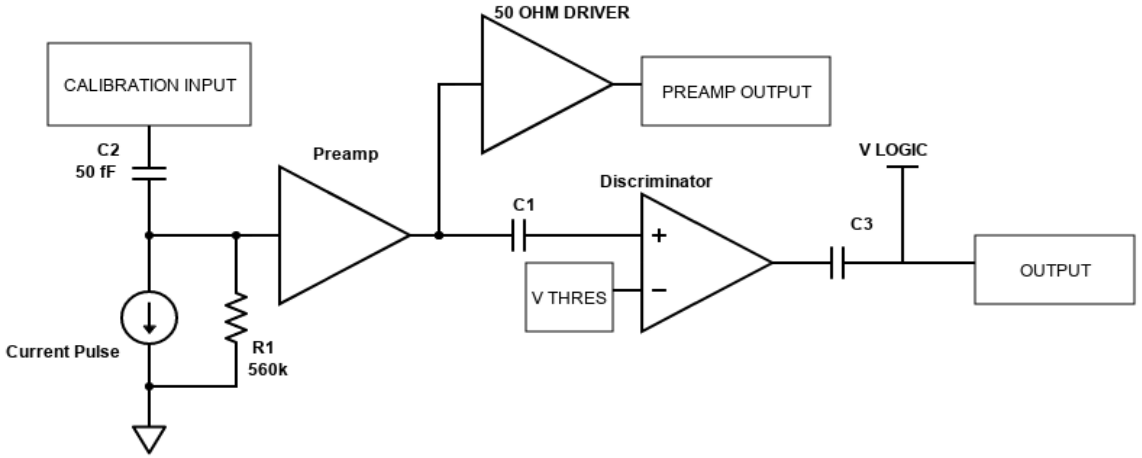
ASROC

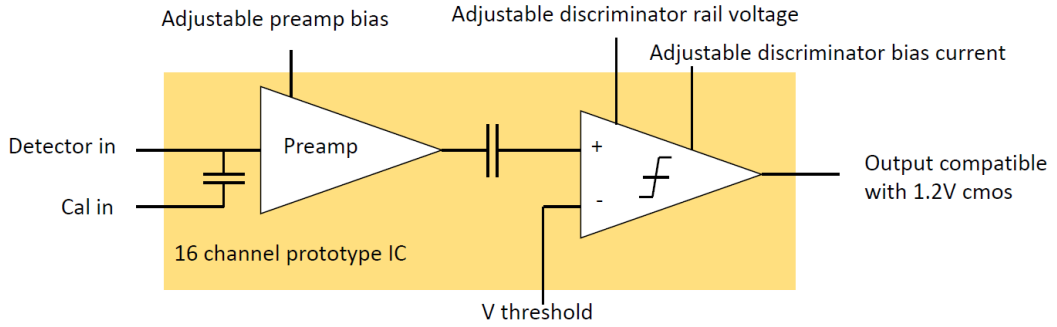
Anadyne
Precision Analog Design

16-ch SiGe BiCMOS analog (preamp. and discriminator) chip, developed under SBIR Phase-1 funding

- Tower Semiconductor 130 nm 10 GHz f_t process
- Common emitter transimpedance front-end, custom discriminator circuit designed for low current, moderate frame rate

- **Focus on low power consumption (~300-800 µW / channel → 0.7-1.1 mW), 10 ps timing resolution (jitter) for 4 fC input signal**
- **ROC design finalized, tapeout: Dec 2022**
- **Readout board designed at SCIPP**





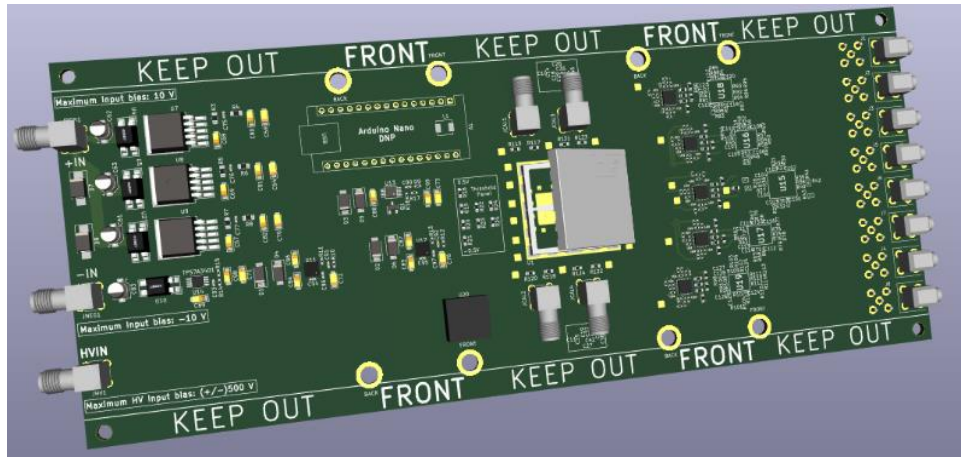
ASROC

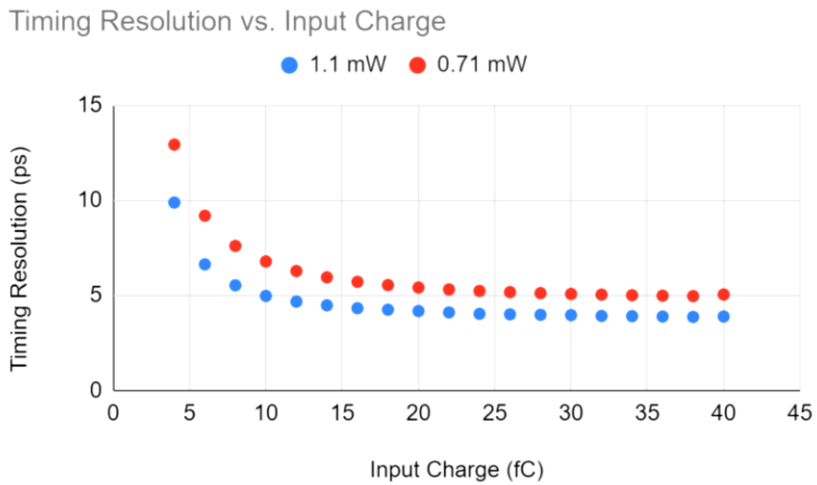
Anadyne
Precision Analog Design

16-ch SiGe BiCMOS analog (preamp. and discriminator) chip, developed under SBIR Phase-1 funding

- Tower Semiconductor 350 nm 10 GHz f_t process
- Common emitter transimpedance front-end, custom discriminator circuit designed for low current, moderate frame rate

- **Focus on low power consumption (~300-800 µW / channel → 0.7-1.1 mW), 10 ps timing resolution (jitter) for 4 fC input signal**
- **ROC design finalized, tapeout: Dec 2022, received August 2023**
  - ➢ Readout board designed at SCIPP
  - ➢ Chip characterization conducted at SCIPP with support from Anadyne

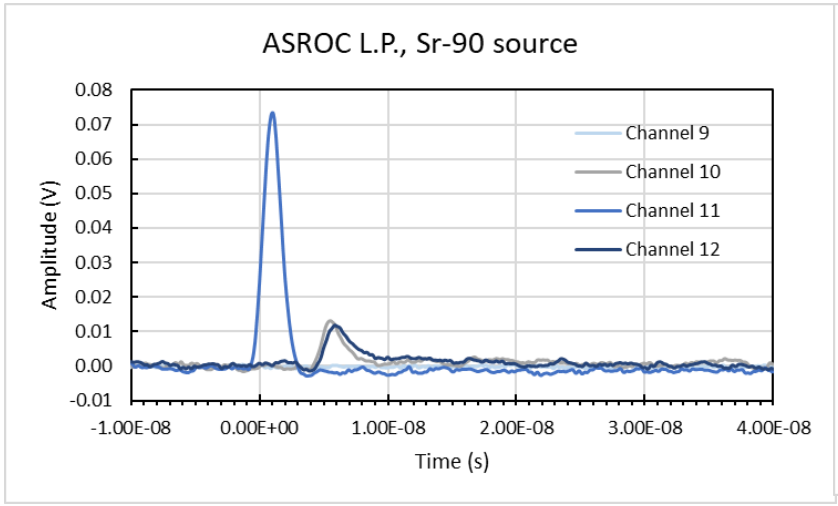


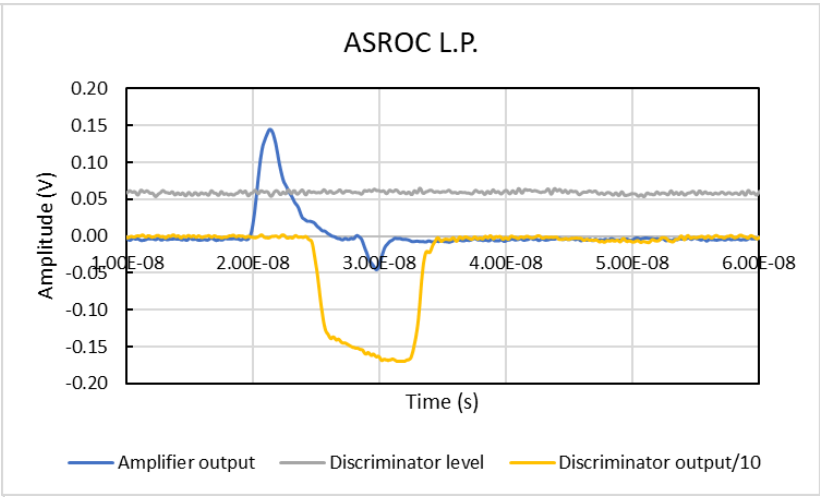


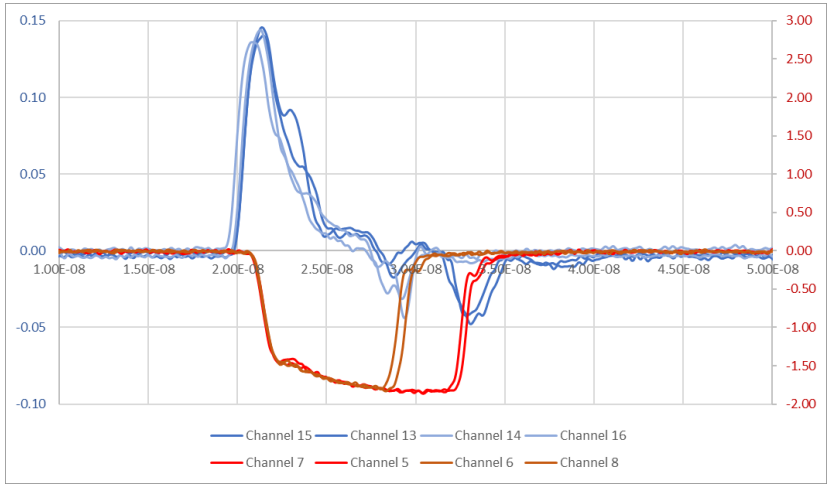
TWEPP2021: https://indico.cern.ch/event/1019078/contributions/4444426/

ASROC

- Preamplifier and discriminator tested with calibration input and AC-LGAD sensor, laser and radioactive source
- Power consumption: 0.88 mW / 1.44 mW per channel, rise time down to 500 ps**, noise 0.4-0.7 mV**
- Remaining issue: cross-talk between preamplifier channels to be quantified; cross-talk from discriminator back into preamplifier output – likely related to discriminator output *driver*, not discriminator circuit itself







[ASROC SiGe chip, TWEPP presentation]

J. DeWitt et al, article revised

Open questions on SiGe

SiGe biCMOS offerings currently limited to 130nm CMOS feature size: does that preclude these processes from being used due to digital back end power consumption?

Slightly faster transistors would improve performance, but past around 25 Ghz ft the design will probably suffer from bad matching, fragile transistors, increased cost, without analog performance benefit. There is an optimum process speed that we suspect is much lower than the latest and greatest SiGe developed for telecom. How fast is appropriate?

What are the input requirements for upcoming 10 ps timing TDC circuitry?

Appropriate discriminator design for timing resolution/low power/high rep rate is much more challenging than preamplifier design in our opinion

Establishing and validating a process with a vendor takes significant time and resources

FAST (INFN Torino)

FAST ASIC family: 110 nm CMOS, 16-(20)-ch discriminator & TDC

- Programmable high- and low-gain stages
- longer rise and fall time

FAST and FAST2 analog chips have been tested at SCIPP with different signal polarities and injected charge

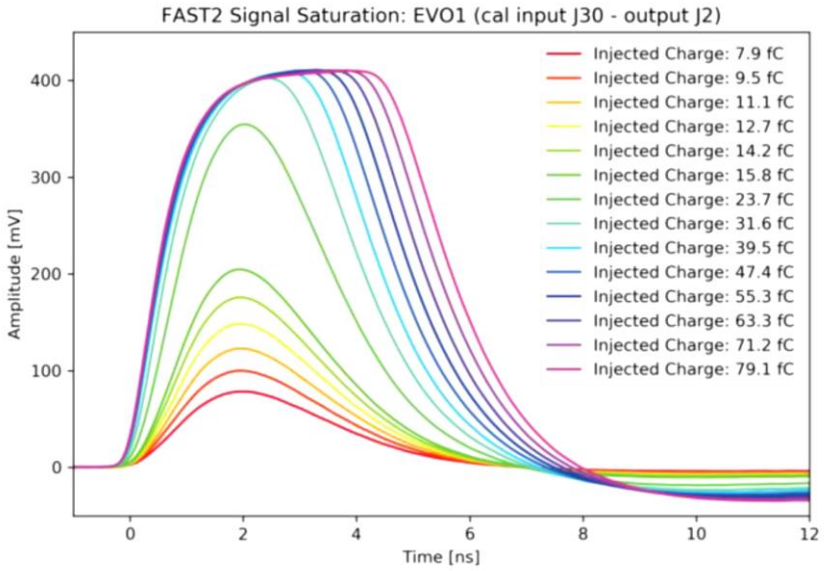
Custom readout board developed for FAST2

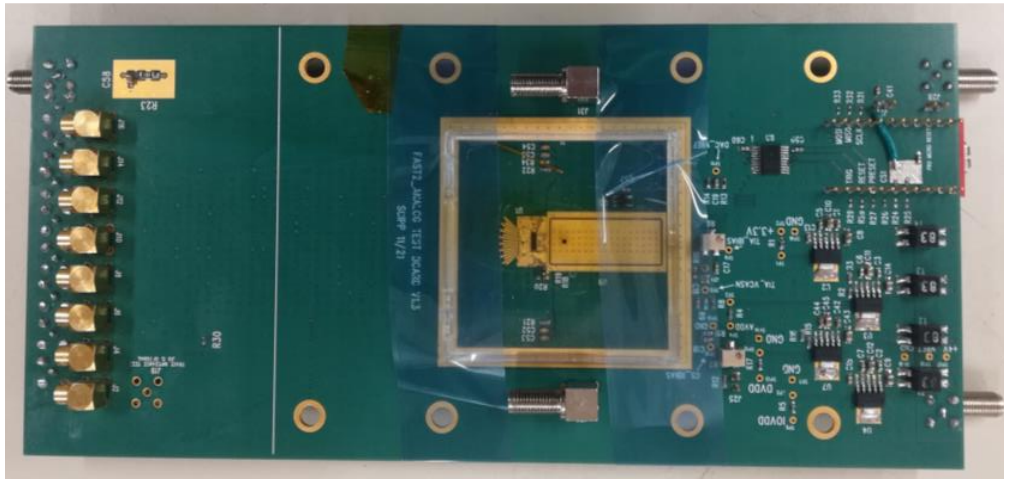
➢**Based on this, board with sensor stack and FAST2 chips developed for beam tests: in production**

In practice, some problems with the gain register setting

FAST3 should be available soon

- FAST2: designing stackable board together with U Washington for a PIONEER ATAR prototype, reading out 2-4 planes of strip AC-LGADs
- FAST3: awaiting chips from INFN Torino, can use existing readout boards designed by SCIPP





E.J. Olave et al (FAST): https://www.openaccessrepository.it/record/74450#.Y7WoDRXMJPZ
A. Martínez Rojas et al (FAST2): https://ieeexplore.ieee.org/document/9875441

ML/AI in particle physics
ML/AI in the front-end

Machine Learning / Artificial Intelligence in the front-end

- Challenges

- *Radiation hardness*
- *Spatial resolution*
- *Timing resolution*
- **Electronics**
- **Data handling**
- **Efficiency**

- Implementation

On-sensor

In front-end ASIC
- Analog
- Digital

On-detector (dedicated ASIC or FPGA)

Trigger

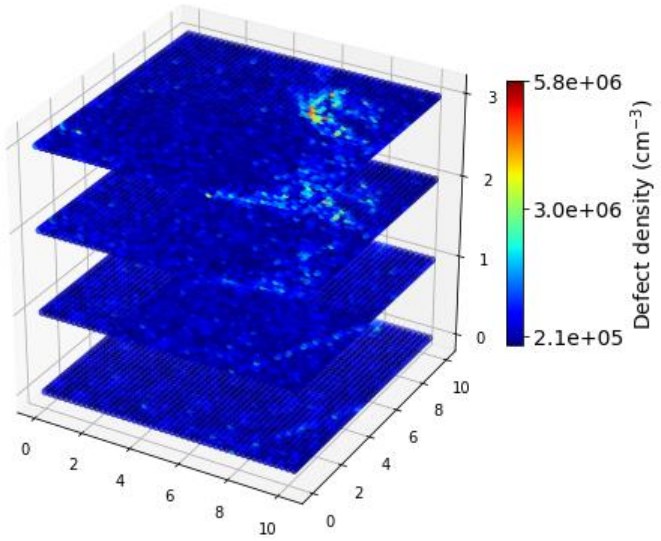
Buffer / memory / data readout

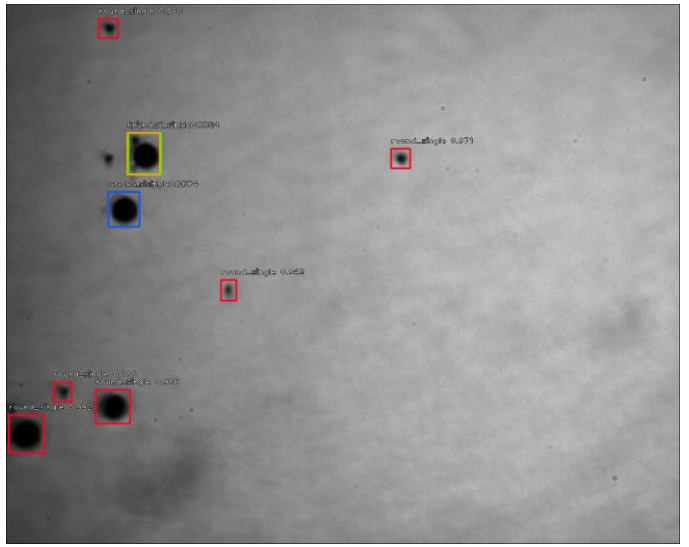
Data reconstruction, analysis

ML/ AI in particle physics instrumentation

- ***Classification: e.g. identification and classification of defects in (optical) images***

- **Infrared microscope scans of CdTe detectors: identification of defects (e.g. ‘round’, ‘trigonal’, ‘undefined’) and x-v size**





S. Kirschenmann et al, incl. J. Ott, *Quality assessment of Cadmium Telluride as a detector material for multispectral medical imaging*, Journal of Instrumentation (2022), 17, C01070

ML/ AI in particle physics instrumentation

- **Spatial resolution in AC-LGADs: hit position reconstruction from signal amplitudes in laser and test beam data**
  - ***Achieves equivalent or better resolution than chi2 or sum formula calculation***

- **Ongoing research, first initial results: inclusion of time-of-arrival information as a parameter improves spatial resolution down to ~3 µm**

- **So far, reconstructions have been based on full waveform data from fast digitizer = oscilloscope readout – little or no studies yet on datasets from in sensor-FE chip assembly**

ML/ AI in particle physics instrumentation

- **Multispectral / ‘dual-readout’ sensors (LGADs), quasi-5D-tracking: energy deposit and maximum amplitude might be the same, but charge carrier drift → rise time and signal shape reveal differences**

- **Classification of signals into point-like energy deposit (x-ray) vs charged particle, gives information about depth of energy deposit with respect to the gain layer, could distinguish pi/p/e/mu**
  - ***Related to LGAD gain mechanism & suppression***
  - ***To use this full potential, would need fast waveform digitization: HP-SoC (Nalu) or other FE technology developed in Varner Lab!***
  - ***I have briefly suggested this in the UCSC-Nalu collaboration: so far we focused on the analog side characterization in the lab, but are/were getting into digital testing as well –resubmission for v2-2 chip →to be delivered this week***

- **Possible applications: PIONEER, ePIC**

ML/ AI in particle physics instrumentation

PIONEER readout and trigger:

- Not decided yet: interplay between detector design, Calo, ATAR, DTAR and their trigger roles
- Highly active phase in simulations at the moment
- Trigger: scheme still open
- Likely streaming readout or semi-streaming

- Generally: on-chip or on-detector to reduce trigger latency

➢ **PIONEER triggering and decay reconstruction: digitized waveform, using 4D-5D information from multiple layers to identify decays – primary opportunity to implement ML/AI models**

ML/ AI in particle physics instrumentation

ePIC (TOF-)PID readout

- **Streaming readout**
- **ePIC detector is standardizing readout/DAQ over the detector as much as possible**
- **Some decisions can be made in subsystems: looking for input**
- **High spatial and timing precision required, but low-occupancy environment for TOF-PID: limiting full readout would be tempting**
- **'region-of-interest' –based triggering or full digitization: e.g. AC-LGADs – if one pixel or strip is above threshold, digitize (or stream from buffer) all neighboring channels to some extent**
  - (not sure whether this needs adaptive ML/AI or if a simpler numerical algorithm would suffice…)

ML/ AI in particle physics instrumentation

Considerations where to apply:

On-ASIC

- Adaptive analog FE (feasible?)
- Digital FE
- Computing → power consumption in FE: especially in innermost pixel layers, problematic!
- Dedicated production
- Can be truly application-specific

- MAPS with ML/AI ? Active volume + preamplification + logic + adaptiveness?

FPGA

- **commercial product, more flexible**
- **further away from – data transfer, delay/latency, …**

➢ **May come down to specific application, what is feasible (also in terms of design / fw development)**

PIONEER

PIONEER Experiment

New pion decay experiment approved at PSI, data taking to be started in 2028
First test beam time assigned in May 2022, second in November 2023

Phase 1

$$R_{e/\mu} = \frac{\Gamma(\pi^+ \to e^+ \nu(\gamma))}{\Gamma(\pi^+ \to \mu^+ \nu(\gamma))}$$

Lepton flavor universality → charged lepton flavor universality violation?

SM prediction ca. 15x more precise than experiment!

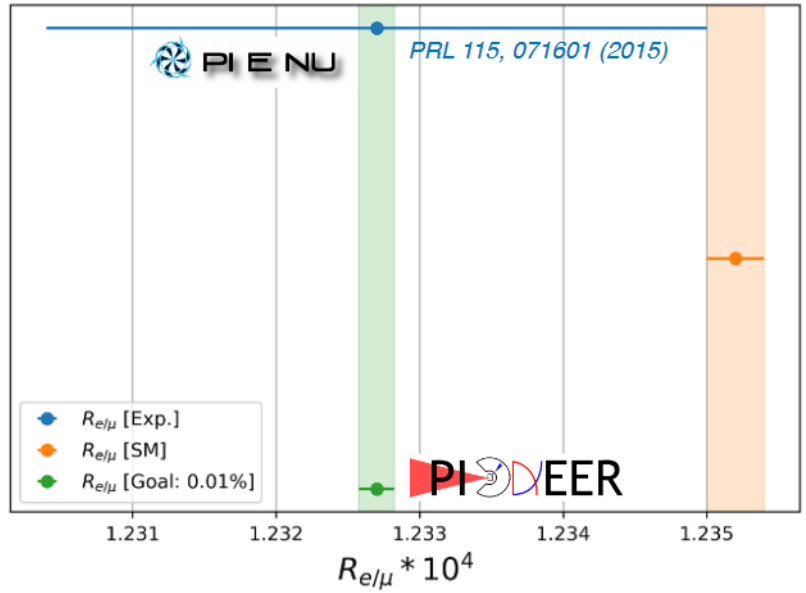
Heavy neutrinos; light New Physics

Phase 2

$$\pi^+ \to \pi^0 e^+ \nu(\gamma)$$

CKM unitarity

$|V_{ud}|$

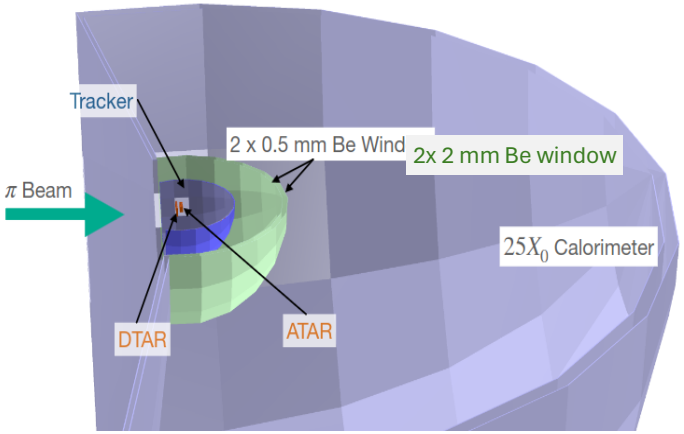


https://arxiv.org/abs/2203.01981

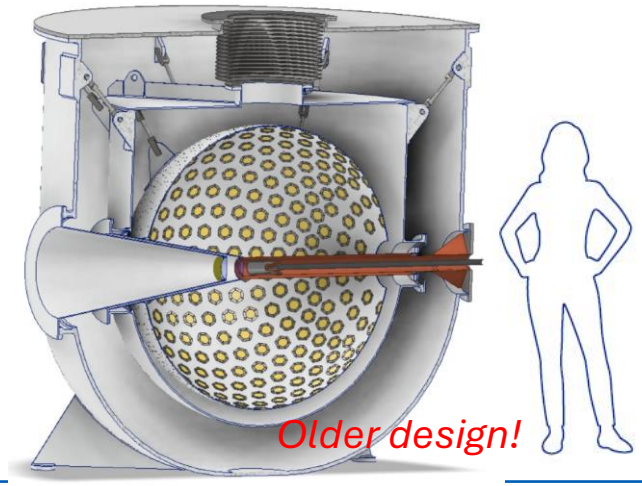
Detectors in PIONEER

Tracker
μ-RWELL

- Nominal design: homogeneous, cylindrical tracker
- Optimized experiment geometry: bullet-shaped or spherical?



Active Target



~2π calorimeter
7t LXe

- Dense, uniform
- Fast response, excellent energy resolution

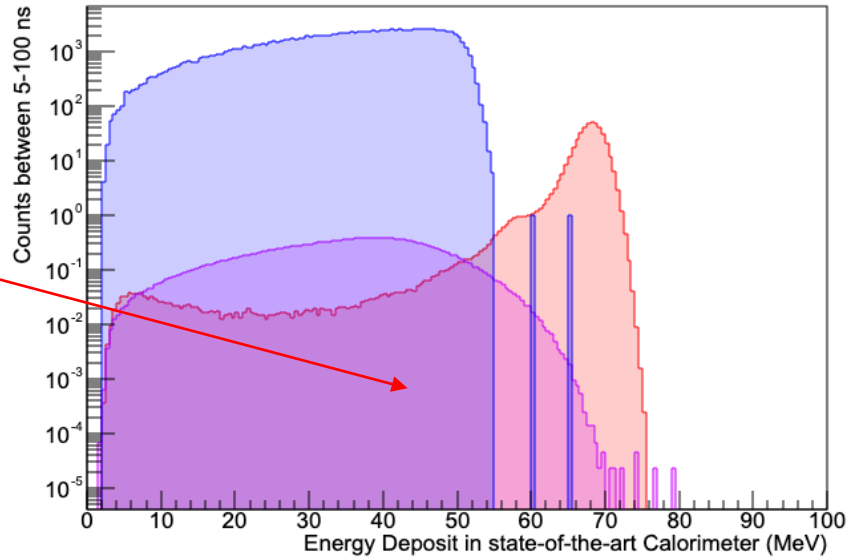
- Challenges: photosensors, cost, photonuclear effects
- **Alternative: LYSO:Ce crystal scintillators**
  - Recent beam test at PSI

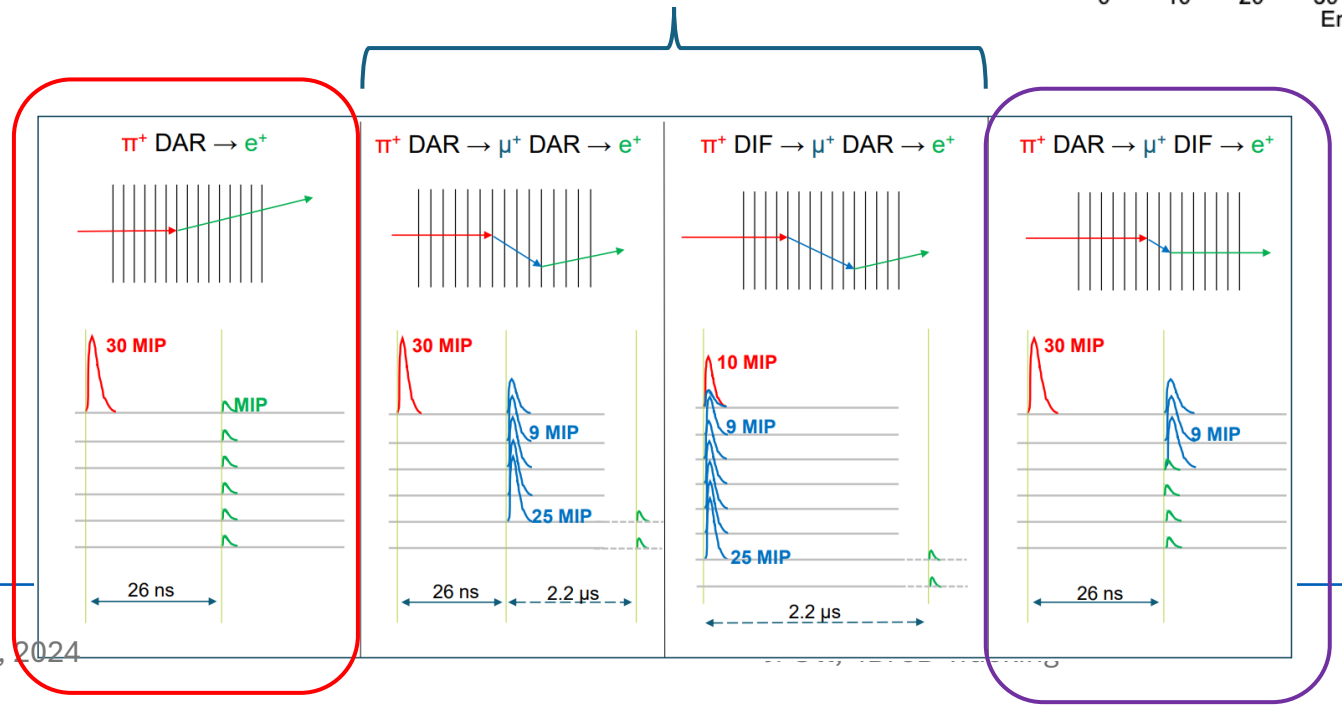
Degrader Target

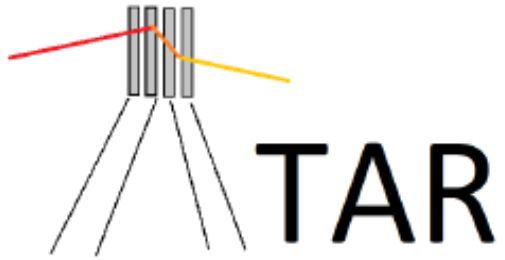
- Additional planes to slow down pion beam and potentially provide backward trigger/veto

Towards 4D (5D) tracking: Active TARget detector

To achieve the PIONEER physics target, it will be crucial to **separate the low-energy tail of $\pi \to e$ events** from $\pi \to \mu \to e$ decays in-flight and at-rest







Towards 4D (5D) tracking: Active TARget detector

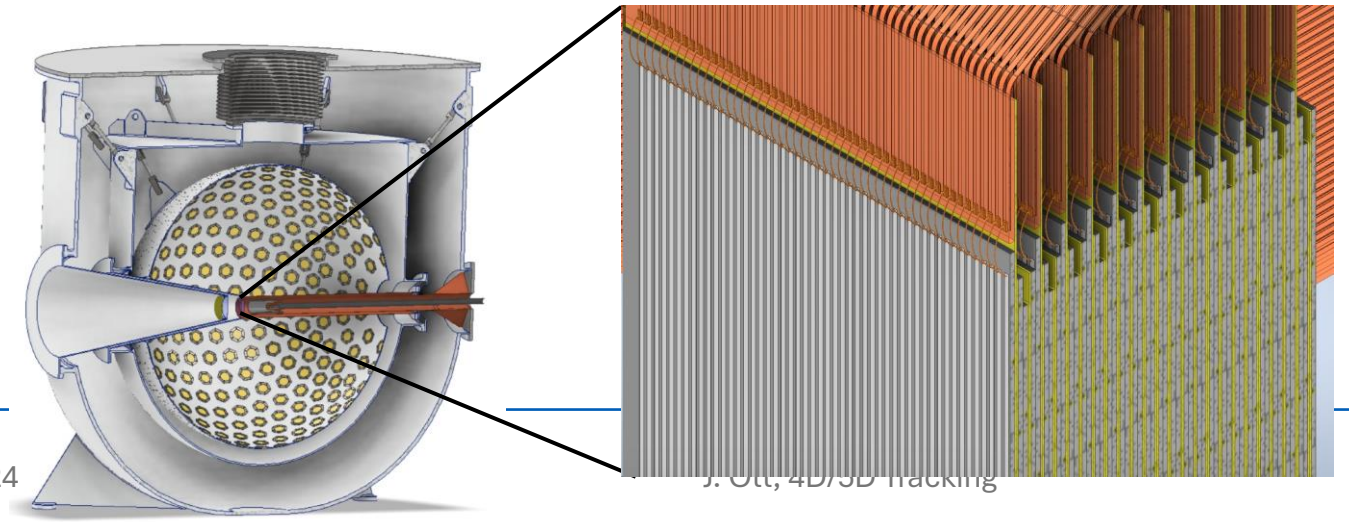
Active TARget: 2x2 cm^2 area, ca. 6 mm thick: 60-75 MeV/c pions stop ~centrally

ATAR requirements:

- Spatial resolution <200 μm
- Timing resolution < 100 ps
- Large fill factor: traditional LGADs with gain termination structures not feasible
- Inactive material not desirable! Support wafers cannot be used.
  - ➢ **Design baseline: 48 stacked planes of 120 μm thick AC-LGAD strips, pitch ca. 200 μm**

Challenge: large energy deposits by stopping particles, up to 4 MeV muon kinetic energy as opposed to minimum-ionizing (30 keV) positron

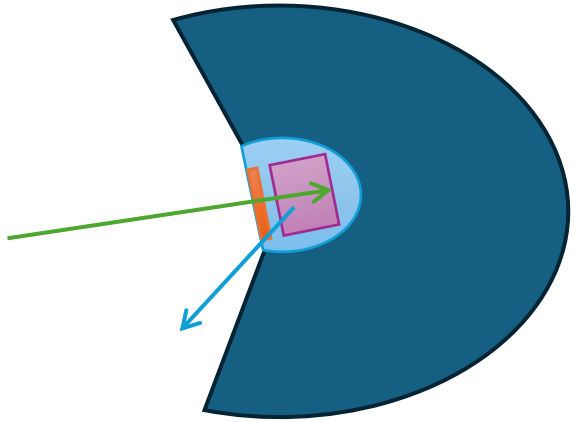
- Investigating possibility of using pin sensors: simplification of energy response, but drawbacks in spatial resolution, signal-to-noise ratio, electronics integration time / timing resolution requirements



Trigger and DAQ

Final design decisions not yet made – targeting streaming readout, but may have a simple layer of trigger that is vetoing hits outside the Calo range and/or from old beam muons based on timing stamp

ATAR was originally not intended to have a role in trigger (to avoid biases): might be revised, or this might be taken up by the Degrader TARget



ATAR readout

Baseline: FAST ASIC analog preamp + Nalu HP-SoC full waveform digitization at 2-10 GS/s

University & INFN Torino FAST family ASIC (current version FAST2, FAST3 just delivered)

- Good rise time even for larger capacitances, different gain settings adjustable per channel
- Considering e.g. split signal preamplification or dynamic gain switching
- Full waveform from digitizer: baseline correction, time walk correction and time-of-arrival with constant fraction discrimination
- Rise time and signal shape in addition to maximum amplitude or CFD: distinguish linear from suppressed gain, energy deposit depth for pion/muon decay

➢ **Excellent use case for ML/AI in front-end**

➢ **Small experiment: looking for contributions and eager to pioneer new technology**

PIONEER Collaboration

A next generation rare pion decay experiment

W. Altmannshofer,[1] O. Beesley,[2] E. Blucher,[3] A. Bolotnikov,[4] S. Braun,[2] T. Brunner,[5] D. Bryman,[6,7] Q. Buat,[2] J. Carlton,[8] L. Caminada,[9] S. Chen,[10] M. Chiu,[4] V. Cirigliano,[2] S. Corrodi,[11] A. Crivellin,[9,12] S. Cuen-Rochin,[13] B. Davis-Purcell,[7] J. Datta,[14] K. Dehmelt,[14] A. Deshpande,[14,4] A. Di Canto,[4] L. Doria,[15] J. Dror,[1] M. Escobar Godoy,[1] S. Foster,[8] K. Frahm,[16] A. Gaponenko,[17] A. Garcia,[2] P. Garg,[14] G. Giacomini,[4] L. Gibbons,[18] C. Glaser,[19] D. Göldi,[16] S. Gori,[1] T. Gorringe,[8] C. Hamilton,[7] C. Hempel,[7] D. Hertzog,[2] S. Hochrein,[16] M. Hoferichter,[20] S. Ito,[21] T. Iwamoto,[22] P. Kammel,[2] B. Kiburg,[17] K. Labe,[18] J. Labounty,[2] U. Langenegger,[9] C. Malbrunot,[7] A. Matsushita,[22] S. Mazza,[1] S. Mehrotra,[14] S. Mihara,[23] R. Mischke,[7] A. Molnar,[1] T. Mori,[22] J. Mott,[17] T. Numao,[7] W. Ootani,[22] J. Ott,[1] K. Pachal,[7] D. Pocanic,[19] C. Polly,[17] X. Qian,[4] D. Ries,[9] R. Roehnelt,[2] T. Rostomyan,[9] B. Schumm,[1] P. Schwendimann,[2] A. Seiden,[1] A. Sher,[7] R. Shrock,[14] A. Soter,[16] T. Sullivan,[24] E. Swanson,[2] V. Tishchenko,[4] A. Tricoli,[4] T. Tsang,[4] B. Velghe,[7] V. Wong,[7] M. Worcester,[4] E. Worcester,[4] C. Zhang,[4] Y. Zhang,[4] and Y. Li[4]

Supported by the U.S. Department of Energy, Office of Science, Offices of High Energy Physics and Nuclear Physics; the U.S. National Science Foundation; JSPS KAKENHI (Japan); Natural Sciences and Engineering Research Council (Canada); TRIUMF; the Swiss National Science Foundation and PSI.

EIC - ePIC

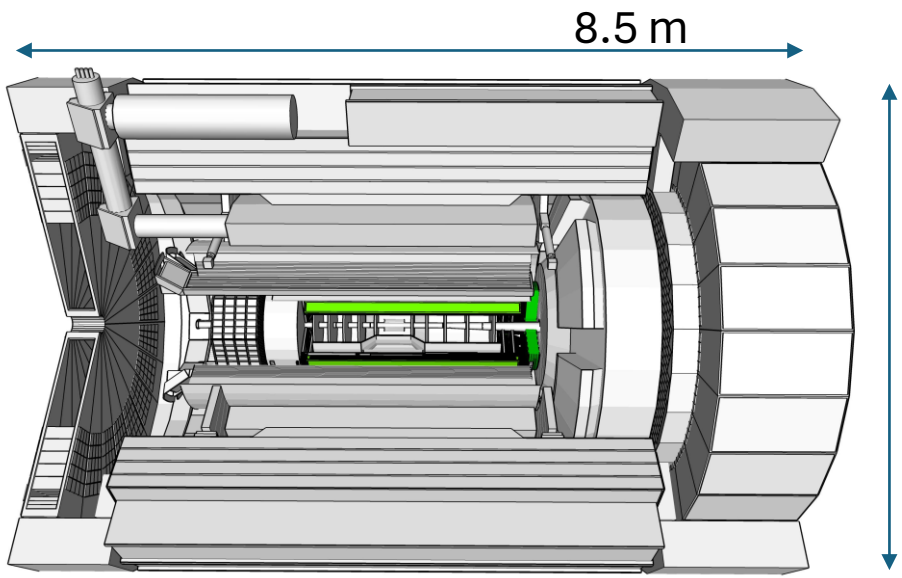
ePIC detector at the Electron-Ion Collider

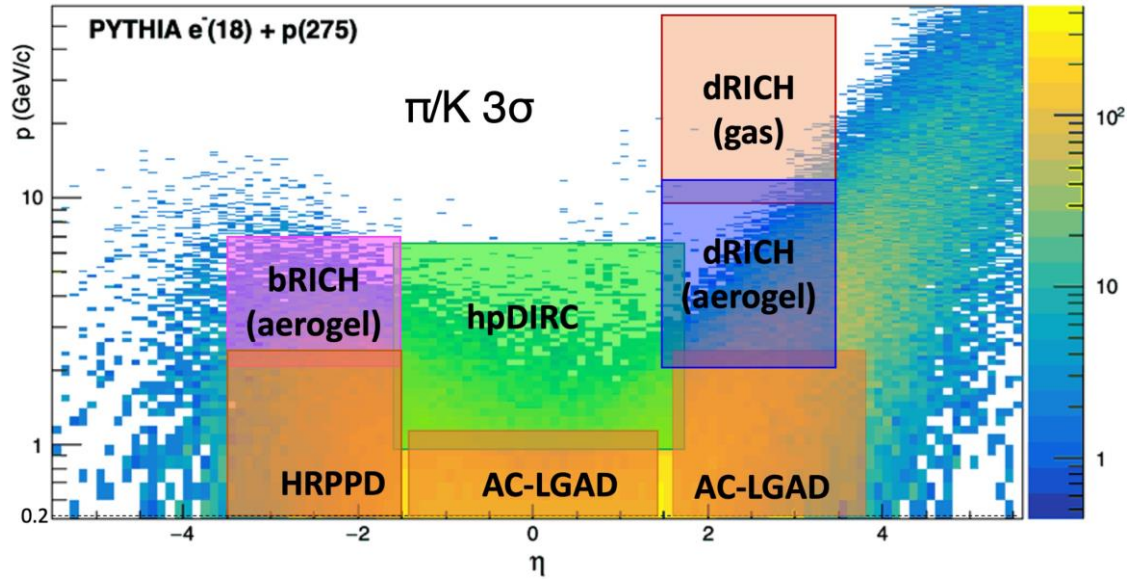
EIC Detector 1: recently issued recommendation, based on two proto-collaborations

- Emerged as ePIC Detector collaboration in summer 2022

Design includes AC-LGADs for time-of-flight particle ID, t_0 determination and timing, and serving as additional layer in Tracking

- Efforts organized in the TOF-PID working group, and eRD112/LGAD consortium





TOF-PID at ePIC

EIC Detector 1: recently issued recommendation, based on two proto-collaborations

- Emerged as ePIC Detector collaboration in summer 2022

Design includes AC-LGADs for time-of-flight particle ID, t_0 determination and timing, and serving as additional layer in Tracking

- Efforts organized in the TOF-PID working group, and eRD112/LGAD consortium

Radiation hardness of timing detectors not very challenging - more important:

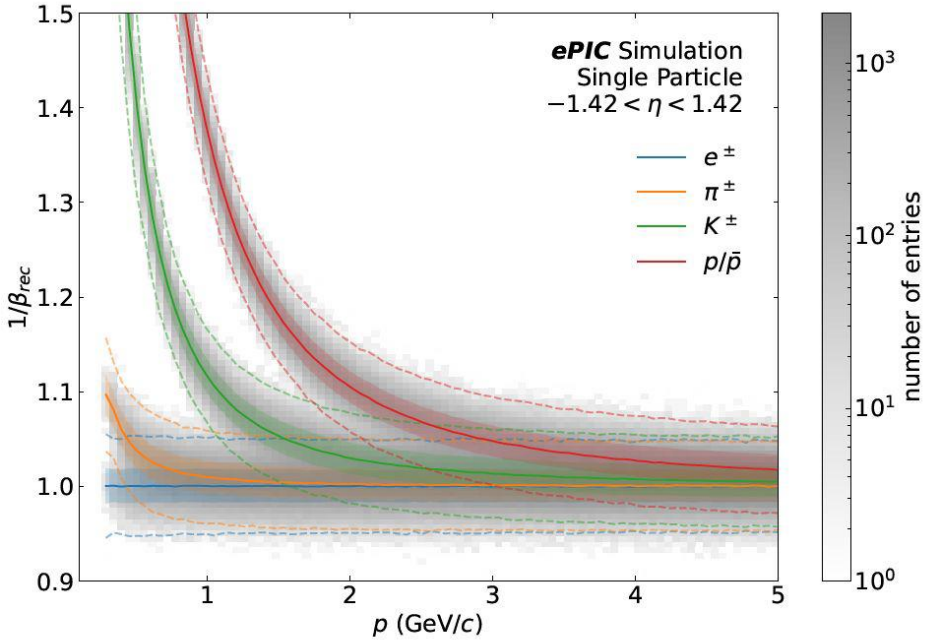
- **Combination of precise temporal and spatial resolution: 25 ps and 30 μm / hit**
- Low material budget

Current sensor design baseline:

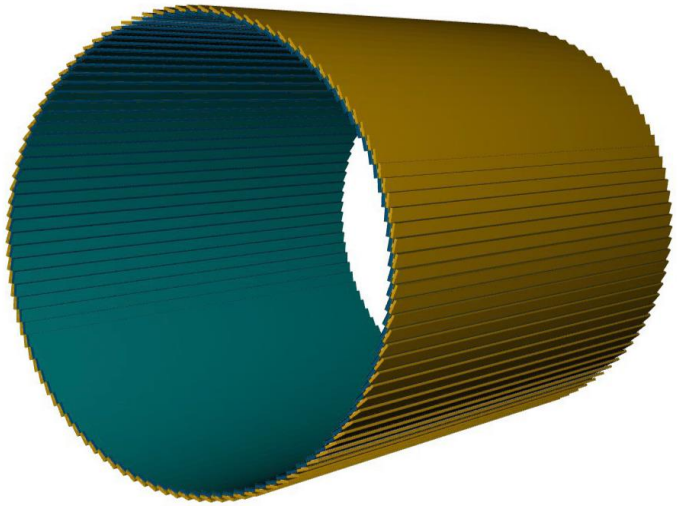
- Barrel: **strips, 500 μm pitch and 1 cm length**
- Hadronic endcap (and Roman Pots): **pads, 500 x 500 μm**

TOF-PID in ePIC

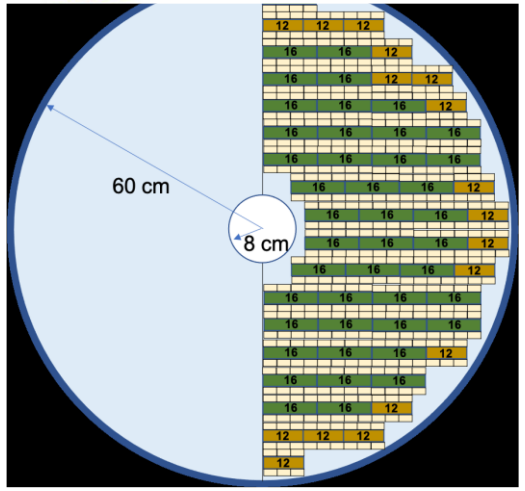
ParticleID in ePIC



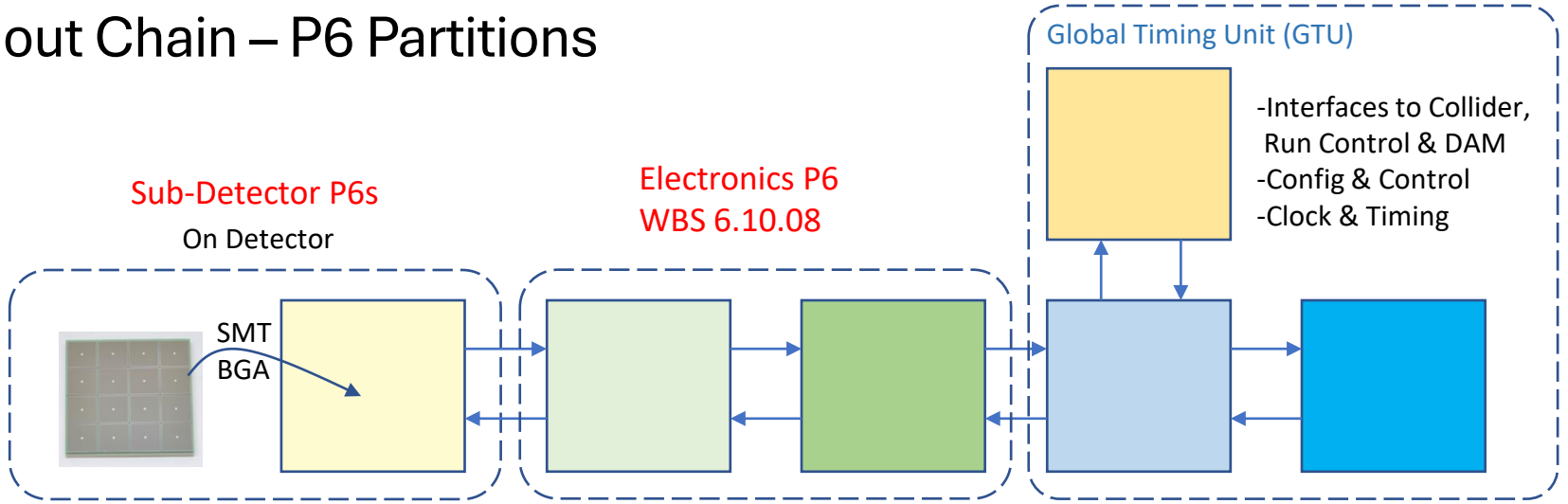
Barrel TOF
Strip sensor modules tilted at 18 deg, similar to STAR tracker



Forward TOF
Similar to CMS ETL



Streaming Readout Chain – P6 Partitions



Name	Sensor	Adapter	Front End Board (FEB)	Readout Board (RDO)	Data Aggregation Module (DAM)	Computing
Design	Detector Specific	Detector Specific	Detector Specific	Few Variants	Common	Common
Function	-Multi-Channel Sensor	-HV/Bias Distribution -HV divider -Interconnect Routing	-Amplification -Shaping -Digitization -Zero Suppression -Bias Control & Monitoring	-Communication -Aggregation -Formatting -Data Readout -Config & Control -Clock & Timing	-Computing Interface -Aggregation -Software Trigger -Config & Control -Clock & Timing	-Data Buffering and Sinking -Calibration Support -QA/Scalers -Collider Feedback -Event ID/Building -Software Trigger -Monitoring
Attributes	-MAPS -AC-LGAD -MPGD -MCP-PMT -SiPM -LAPPD	-Sensor Specific -Passive	-ASIC/ADC -Discrete -Serial Link	-FPGA -Fiber Link	-Large FPGA -PCIe -Ethernet	-COTS -Ethernet

Detector R&D collaboration environment

Collaborations and funding opportunities

CERN / International: transition from RD's to *DRD* collaborations

US: *RDC*'s through APS-DPF Coordinating Panel for Advanced Detectors

Both are currently in the process of forming and establishing their leadership, work packages, and future R&D directions

Strong incentive to have university groups actively participate in and lead projects!

US: CPAD

CPAD has (re)initiated its detector R&D Collaborations during 2023, orientation from the CERN and ECFA road map

11 RDCs with co-conveners

Currently organising themselves, aiming at identifying common R&D interests – and resulting work packages, proposals – within the community

- So far, only funding instrument confirmed by DoE is the Fall 2024 Comparative Review: aiming to have 'blue-sky' R&D oriented towards a scope of application ~10+ years in the future; likely funding ca. 5 proposals selected across all RDCs, $100k in the first year with increases in the following years

Strongly motivated (required) to have university groups actively participate in and lead projects!

RDC#	TOPIC	COORDINATORS	MAILING LIST
1	Noble Element Detectors	Jonathan Asaadi, Carmen Carmona	cpad_rdc1@fnal.gov
2	Photodetectors	Shiva Abbaszadeh, Flavio Cavanna	cpad_rdc2@fnal.gov
3	Solid State Tracking	Anthony Affolder, Sally Seidel	cpad_rdc3@fnal.gov
4	Readout and ASICs	Angelo Dragone, Mitch Newcomer	cpad_rdc4@fnal.gov
5	Trigger and DAQ	Zeynep Demiragli, Jinlong Zhang	cpad_rdc5@fnal.gov
6	Gaseous Detectors	Prakhar Garg, Sven Vahsen	cpad_rdc6@fnal.gov
7	Low-Background Detectors	Daniel Baxter, Guillermo Fernandez-Moroni, Noah Kurinsky	cpad_rdc7@fnal.gov
8	Quantum and Superconducting Sensors	Rakshya Khatiwada, Aritoki Suzuki	cpad_rdc8@fnal.gov
9	Calorimetry	Marina Artuso, Minfang Yeh	cpad_rdc9@fnal.gov
10	Detector Mechanics	Eric Anderssen, Andreas Jung	cpad_rdc10@fnal.gov
11	Fast Timing	Gabriele Giacomini, Matt Wetstein	cpad_rdc11@fnal.gov

https://cpad-dpf.org/

Funding pathways (US)

- **Department of Energy**
- **National Science Foundation**
- NASA, NIH, …

Base grants

Project-specific funding

Consortia: e.g. US-Japan

SBIRs – interaction with industry

Land / Space / Sea grants ?

EPSCORE funding for states underrepresented in research – includes incentive for national laboratories to collaborate with institutions from such regions

Division line: High-Energy // Nuclear Physics (// Astro ?)

- *Somewhat frustrating in instrumentation…*
- ***Ideal case, goal: ability to demonstrate applicability of research and technology to either, obtain funding from both***

Summary: research plan(s) and directions

- Fast timing ASIC utilizing machine learning in waveform analysis and/or readout (data streaming) trigger decision
- Involvement in 4D tracking sensor/electronics (detector system) development
- Radiation-hard 4D/5D tracking electronics

- Drive delivery of PIONEER ATAR together with UCSC, UW, BNL
- Identify areas of application for technology developed here and actively engage in experiments that could provide such a platform (future collider proto-collaborations, EIC, Belle-2)
- Reconstruction in ATAR, other experiments

Silicon detectors in (partial) calorimetry: Astropix

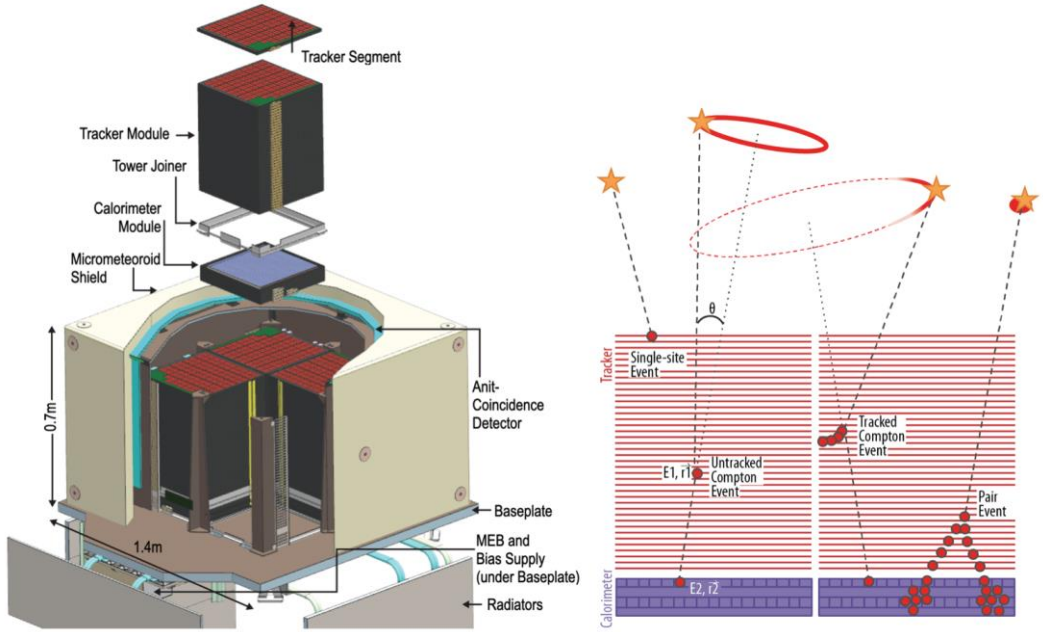
AMEGO-X satellite: Gamma ray telescope with stacks (towers) of segmented silicon detectors

- Tracking of Compton scattering and pair production events
- Energy measurement of scattered electron; single interaction < 100 keV

Astropix HV-CMOS: also to be used in inner layers of EIC ePIC barrel ECAL

- thicker active sensor – 700 µm bulk
- 500x500 um pixel pitch

Currently: Astropix v3 fabricated and being tested; challenges with depletion and leakage current in high-resistivity substrate – some laser edge-TCT studies at UC Santa Cruz conducted by J. Ott et al



R. Caputo et al, *The All-sky Medium Energy Gamma-ray Observatory eXplorer (AMEGO-X) Mission Concept*, https://arxiv.org/abs/2208.04990

Other disciplines

Astroparticle physics

Medical imaging

- ➢ **Hawai'i Cancer Center??**

Photon science

- **LGADs have become increasingly popular: low- to moderate, non-Geiger mode gain**
- ➢ **UH LINAC / FEL**

Precision tracking

The High-Luminosity LHC

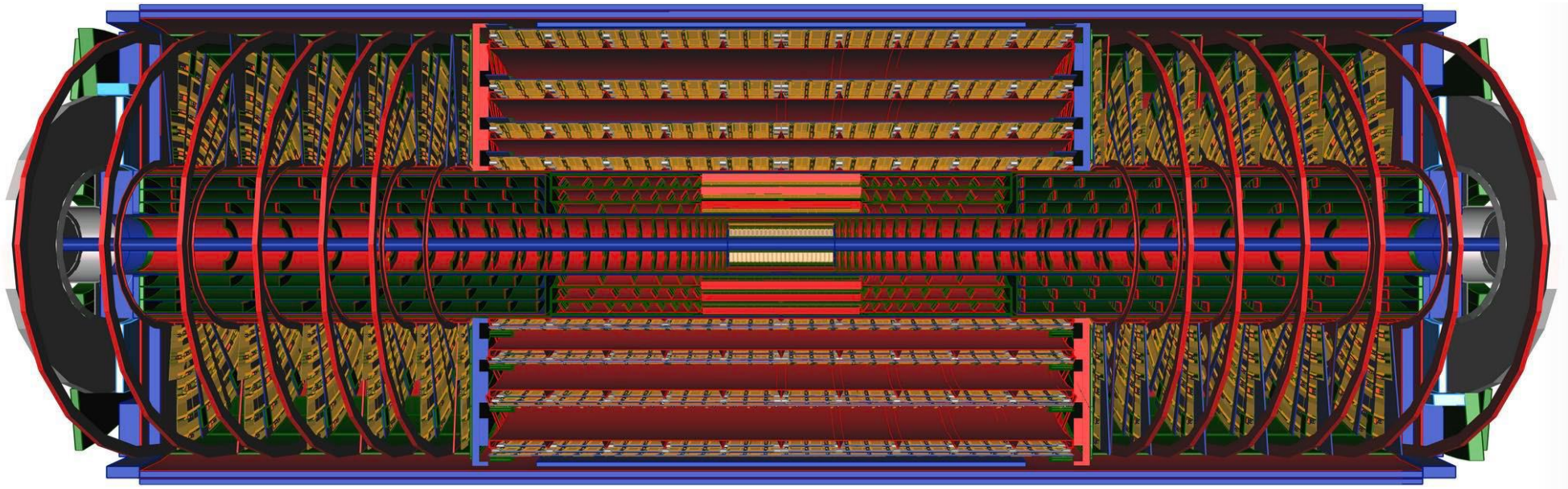
- Long shutdown in years 2026-2029: installation of Phase-2 upgrades and transition to High-Luminosity LHC
- Collision energy 14 TeV

- Luminosity up to $7x10^{34}$ $cm^{-2}s^{-1}$ (LHC: $2x10^{34}$ $cm^{-2}s^{-1}$)
- Up to 200 p-p collisions per bunch crossing (”pile-up”)
- Fluence, i.e. radiation dose, to the innermost silicon detector layers: $2x10^{16}$ n_{eq} cm^{-2}

- **E.g. CMS Experiment**
  - In the pixel tracker: ~ 140 000 pixels / chip (as compared to present 4160)
  - Pixel size 50x50 µm or 25x100 µm
  - Total number of channels: 1 924 M

ATLAS ITk

Phase-2 Upgrade for the ATLAS Experiment towards the HL-LHC features a new Inner Tracker detector: all-silicon, inner tracker with pixel sensors, outer region with strips



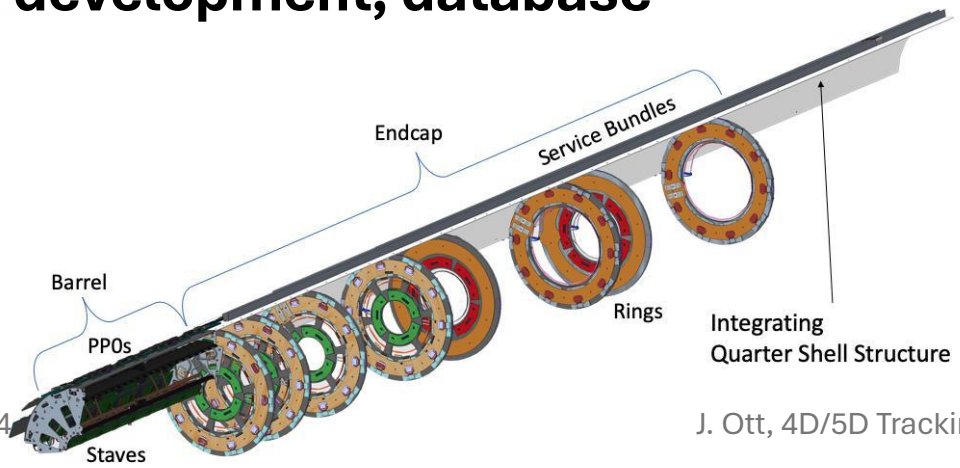
ATLAS ITk Pixel detector

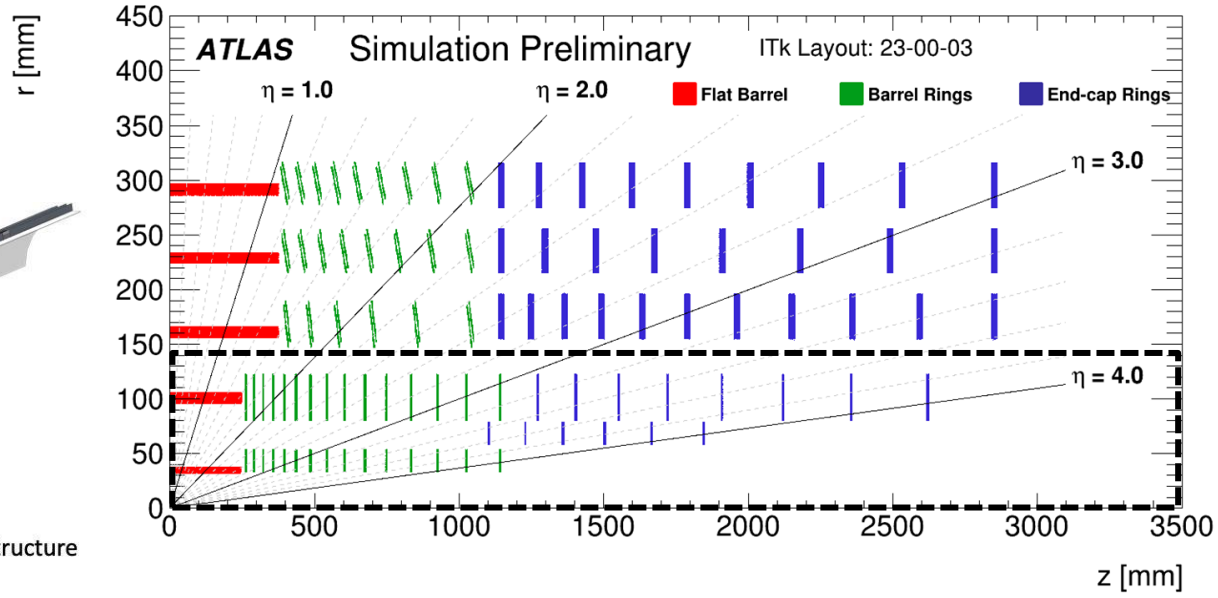
The US has committed to provide a standalone inner unit of the pixel tracker – the Inner System

- Modules, electronics, mechanics, cooling, services, data transmission, …
- Interfacing with international ITk project

UCSC contributes to:

- **Pixel Modules**
- **Pixel Services**
- **Software development, database**





Pixel module (pre)production in the US

1 assembly site, 3 testing sites (1 backup)

- Argonne National Laboratory, Lawrence Berkeley National Laboratory, University of Oklahoma, University of California, Santa Cruz
  - *Cluster 'manager' (coordination and reporting; no formal project responsibility): rotating, currently JOtt*
- *Loading onto mechanical supports and everything beyond is not formally included in Modules working group*

Production plan: ~1200 Layer-1 (planar n-in-p 100 µm-thick sensors) quad modules to be assembled, testing split between sites

- ~400 modules to be tested at UCSC
- Potential to accommodate more modules to support other sites

Qualification process for sites before (pre)production: according to the international project procedures, several qualification blocks and subblocks

Pixel module electrical testing and quality control

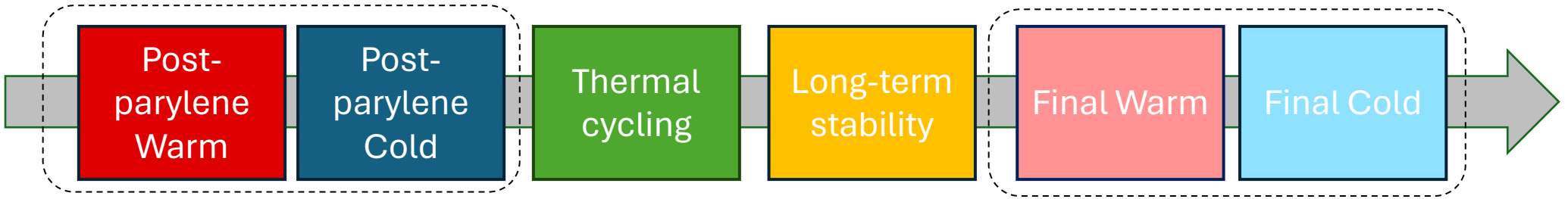
Objective: ensure functionality of modules before they are being installed in the detector

- Verify electrical performance in warm and cold operating conditions
- Identify thermal stress-induced degradation of bump connections
- Simulate continuous operation / readout as would be the case in the detector

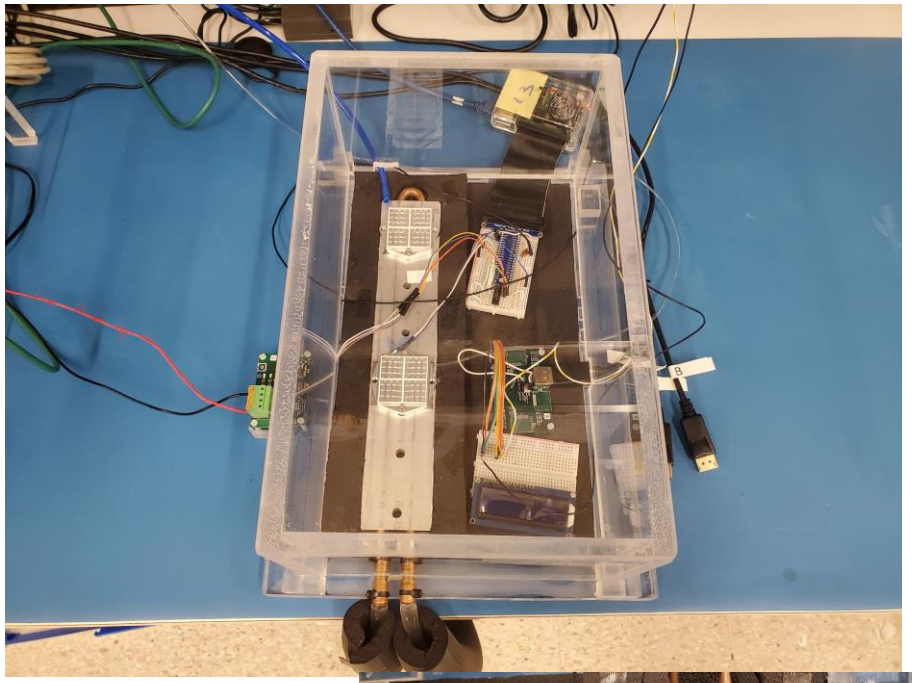
Non-electrical QC:
- Visual inspection
- Sensor IV

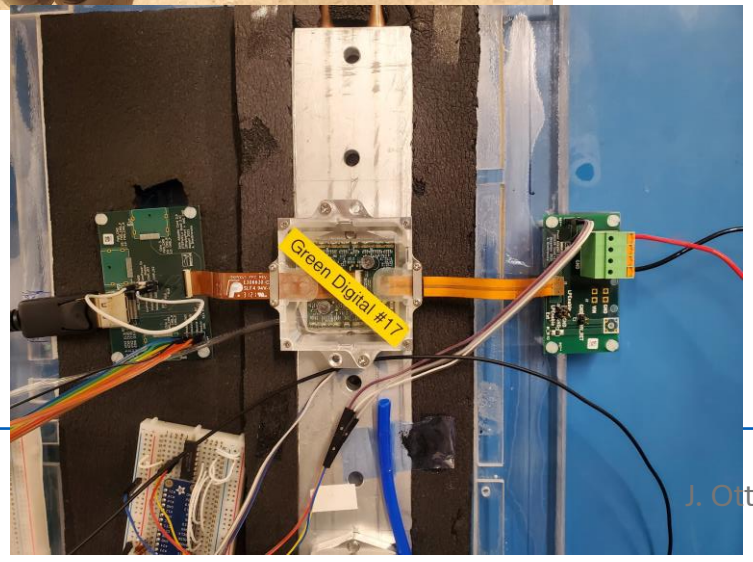
Electrical QC: chip-level functionality
- ADC calibration
- Analog-readback
- SLDO
- Low-power mode
- Overvoltage protection
- Undershunt
- E-fuse/Register
- Data transmission

Electrical QC: chip performance
- Minimum health (digital, analog)
- Threshold tuning
- Pixel failure (incl. disconnected bumps, **source scans**)



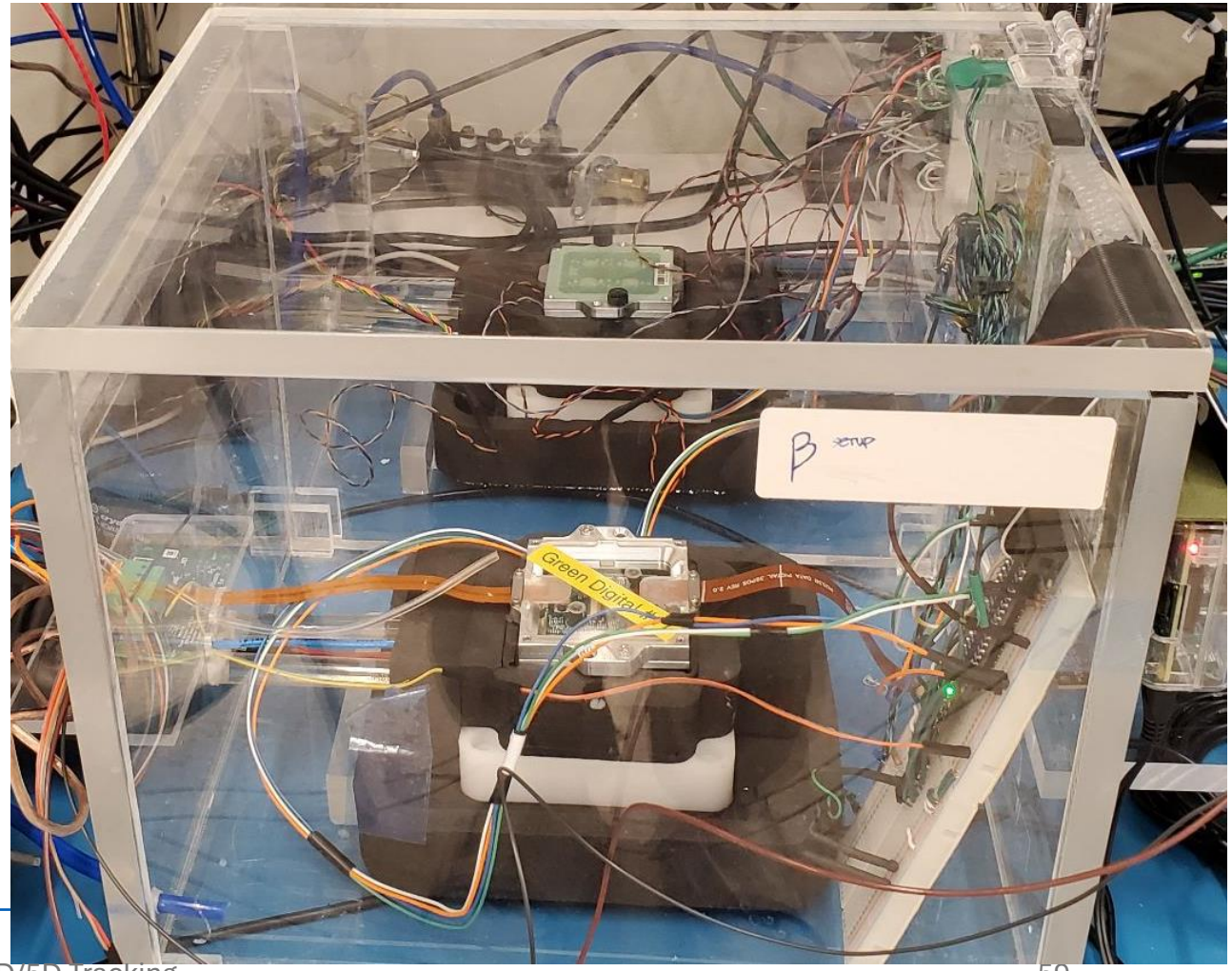
Module testing setups





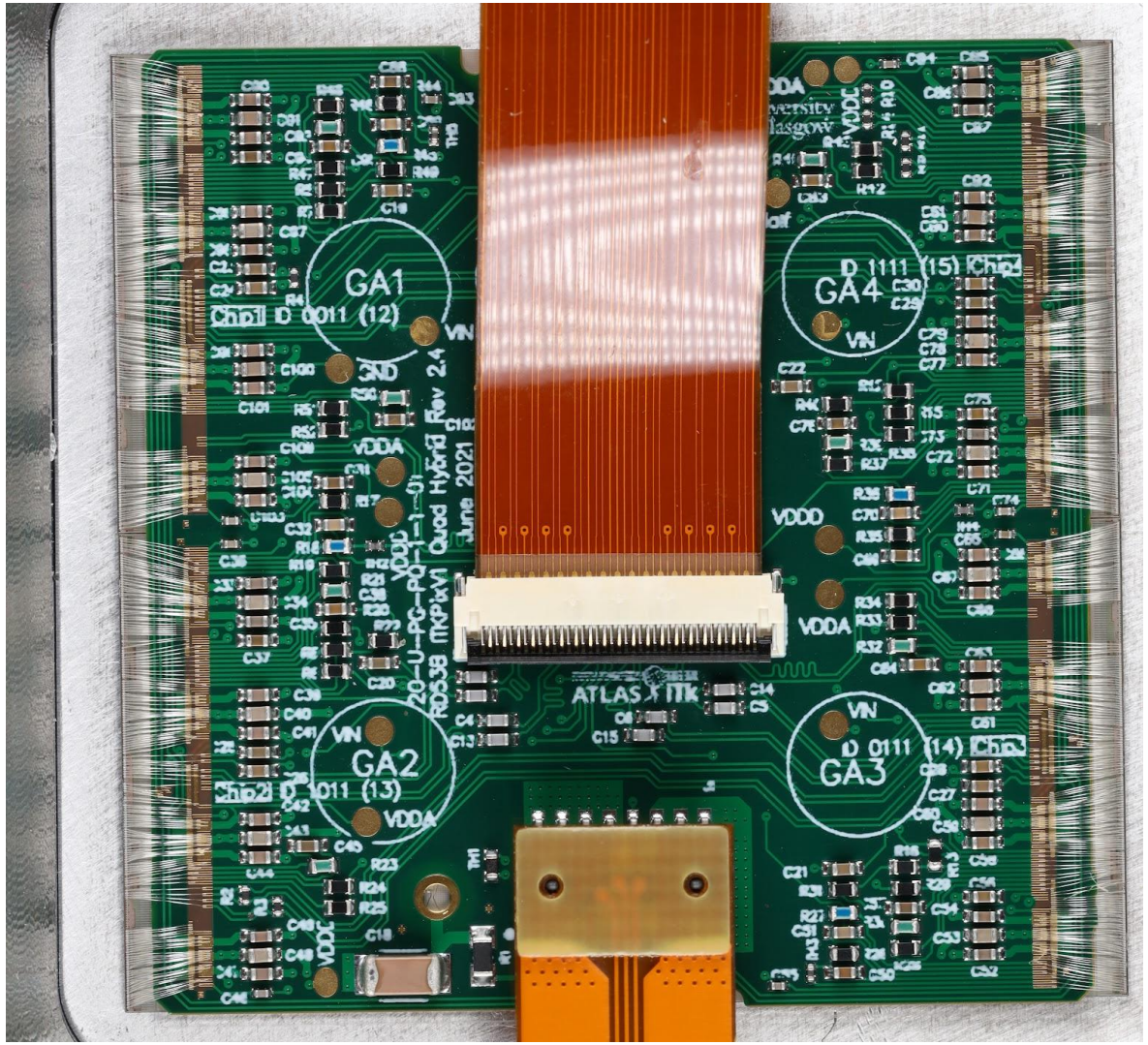
UCSC room temperature digital module setup

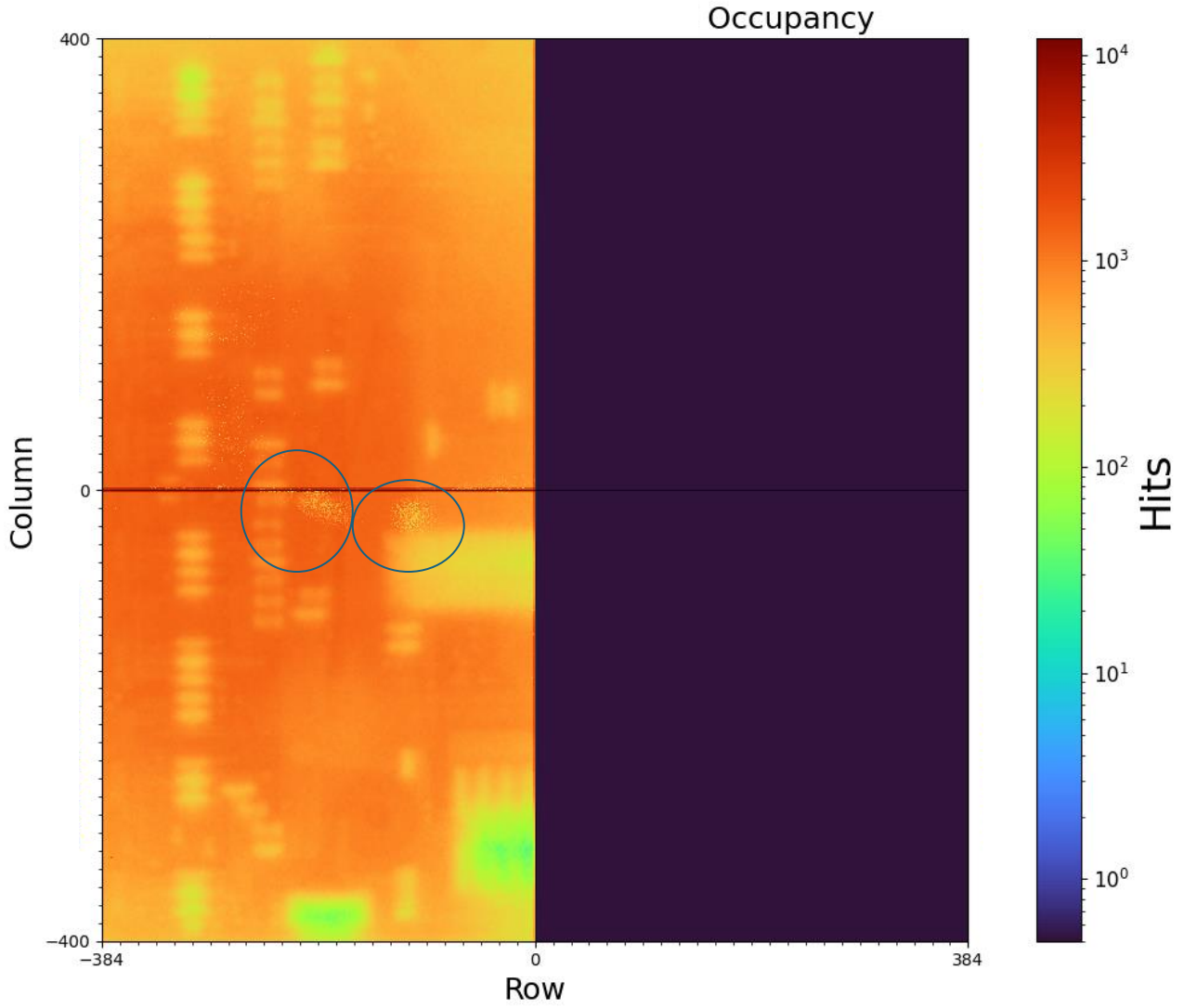
UCSC temperature-controlled module testing setups



Pixel module testing

Areas with disconnected bumps identified with Sr-90 source scan





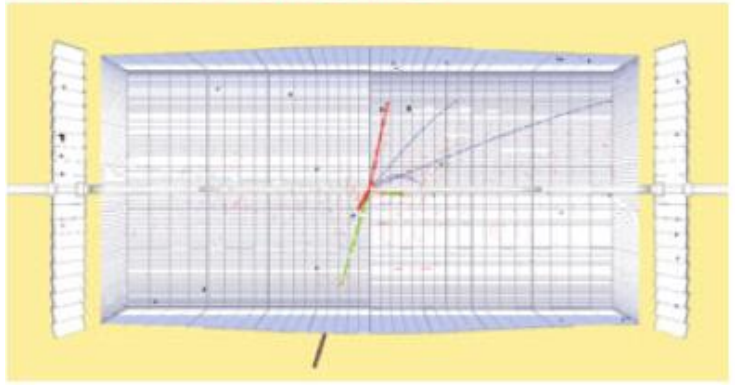
Precision timing

Precision timing

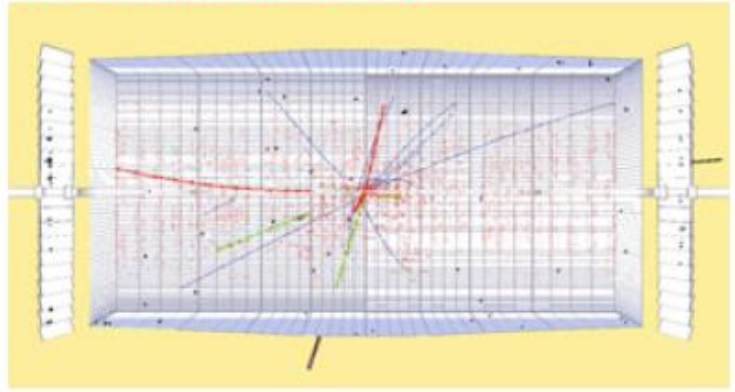
Pile-up of collisions increases to ~200

Timing resolution of 30-60 ps is needed to associated tracks to primary vertex (and improves many analyses performances)

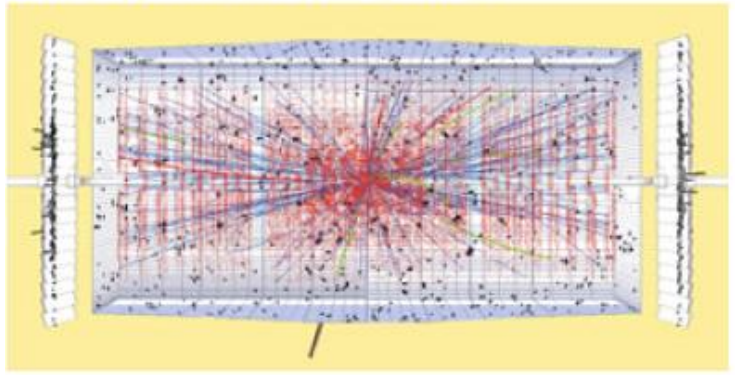
LHC initial: 10^{32} cm^{-2} s^{-1}



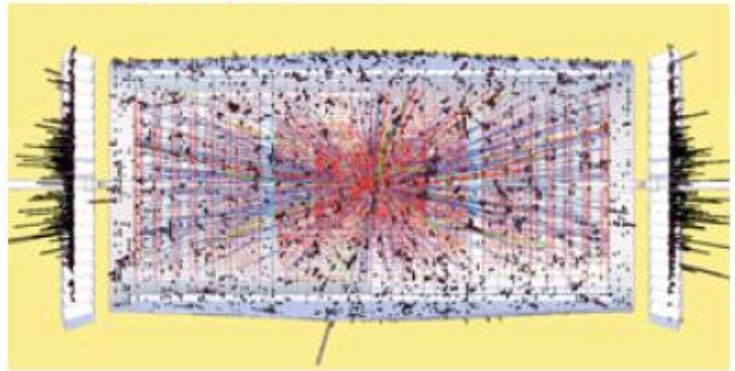
LHC initial: 10^{33} cm^{-2} s^{-1}



LHC nominal: 10^{34} cm^{-2} s^{-1}



HL-LHC: 10^{35} cm^{-2} s^{-1}



Precision timing

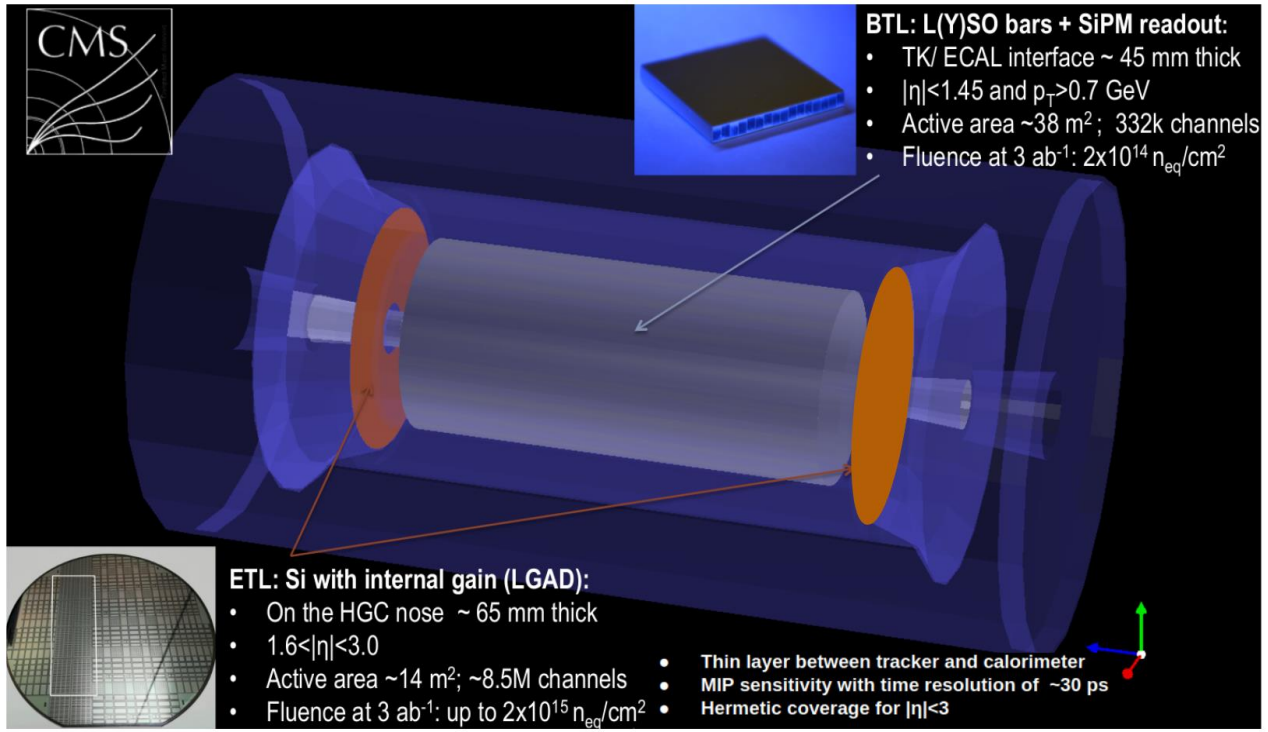
CMS and ATLAS experiments will install dedicated MIP timing detector layers in the Phase-2 upgrades, between tracking systems and calorimeters

CMS

- Barrel and endcap region with different technologies: barrel scintillators + SiPM, endcap with fast silicon detectors - LGADs

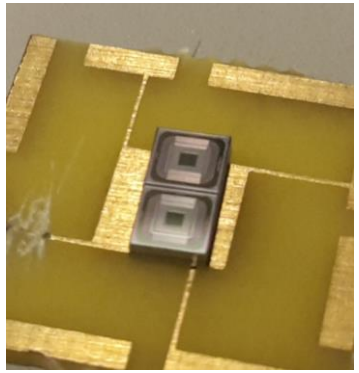
ATLAS

- Timing detectors only in the endcap region, with LGADs

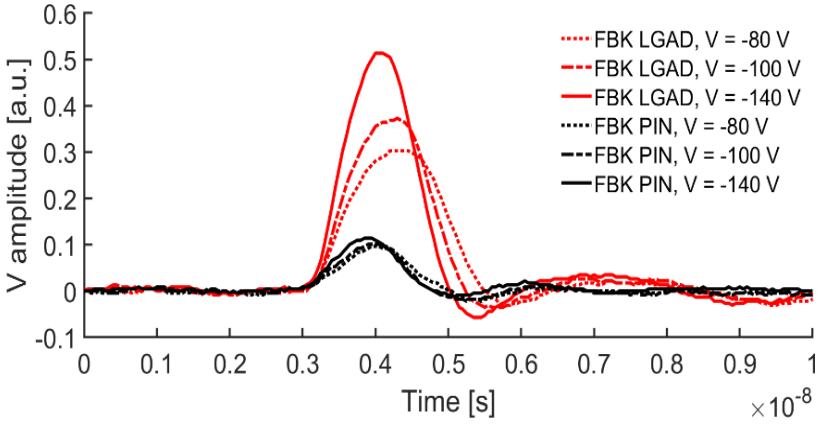


CMS MTD Technical Design report

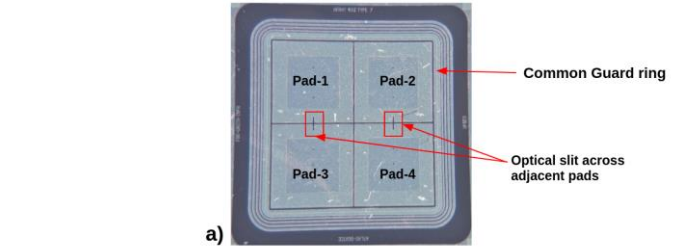
Vendor qualification and studies on no-gain region width in LGADs for the CMS endcap timing layer

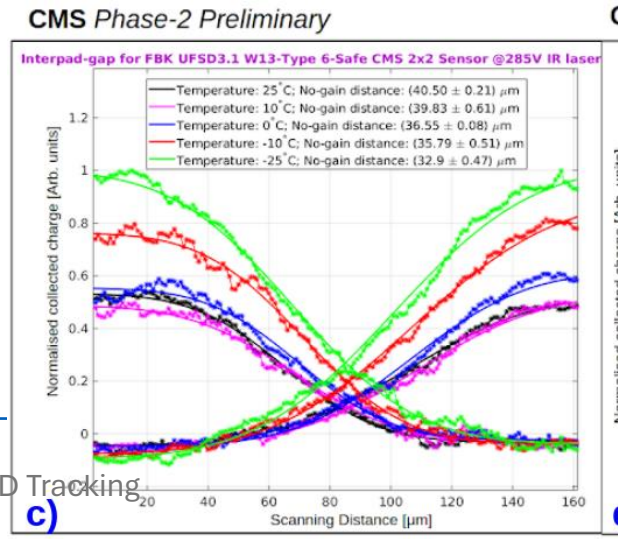


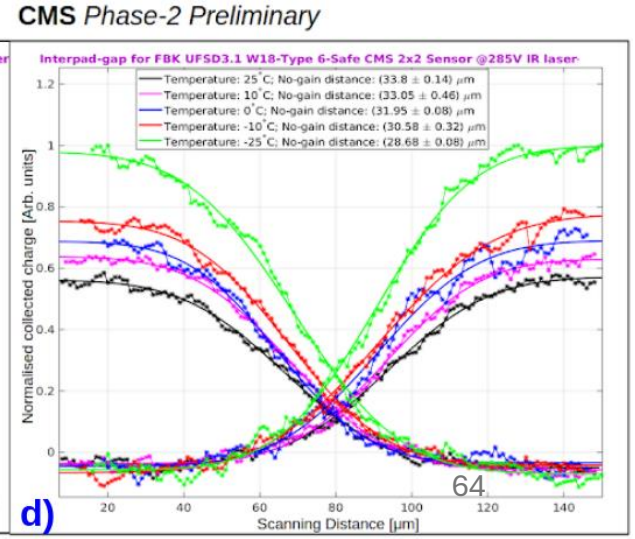
Gain determination with LGAD-diode pairs in laser TCT



Effective no-gain region varies with interpad termination structure, p-stop doping dose, temperature



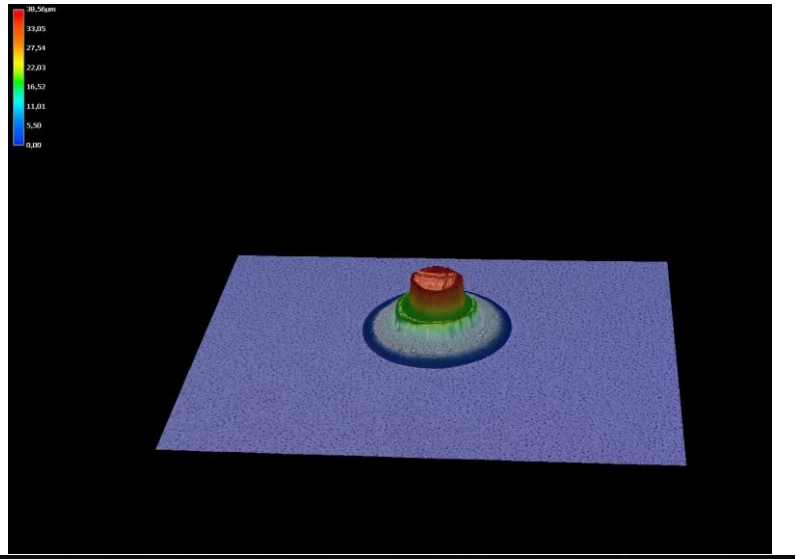


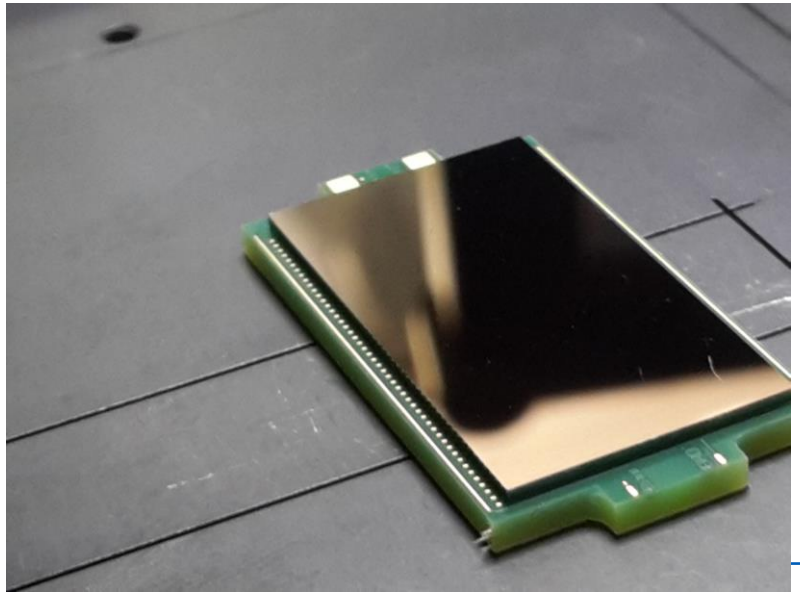


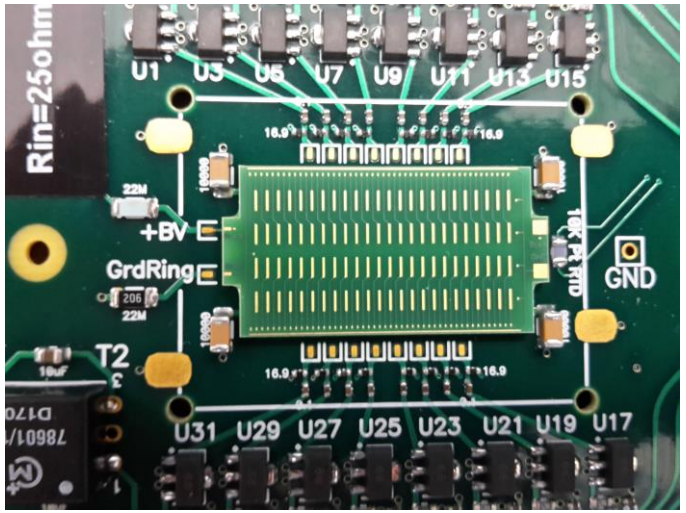
S. Bharthuar, **J. Ott** et al on behalf of the CMS Collaboration, *Study of no-gain distance of HPK 3.1 production LGADs with Transient Current Technique*, Nuclear Instruments and Methods in Physics Research A (2020), 979, 164494

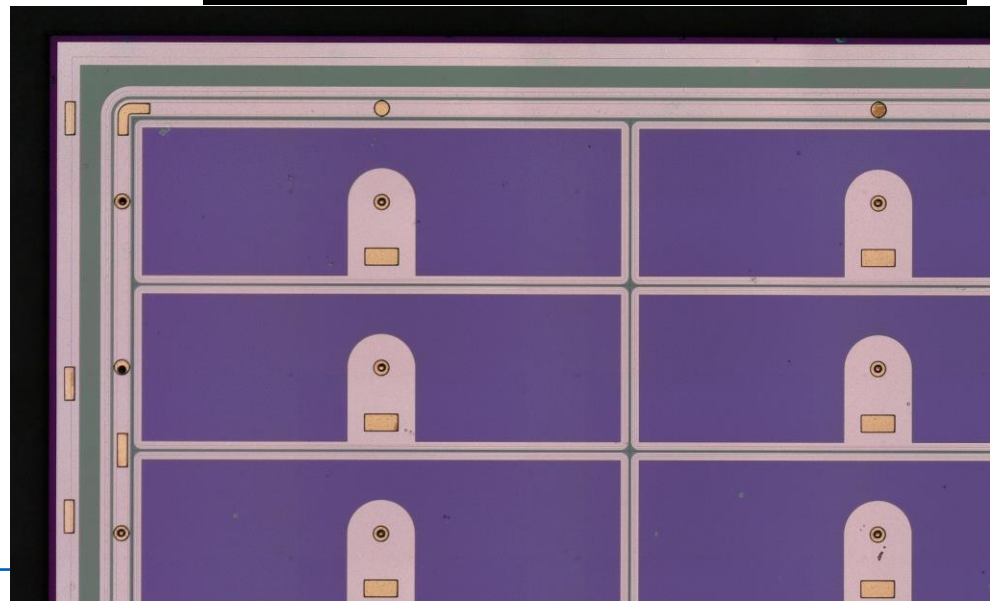
First attempts at bump-bonding and reading out large LGAD sensor prototypes

- Fabrication of interposer PCB
- Gold stud bump deposition on FBK and CNM sensors, flip-chip bonding of sensors to PCB at KIT



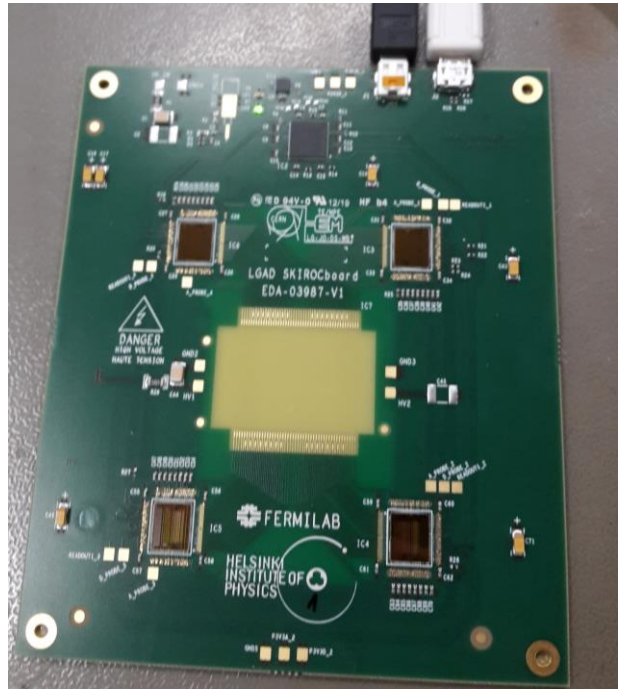


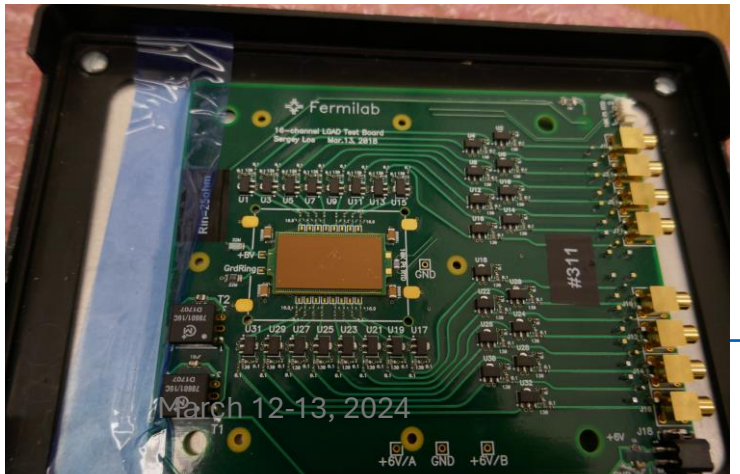


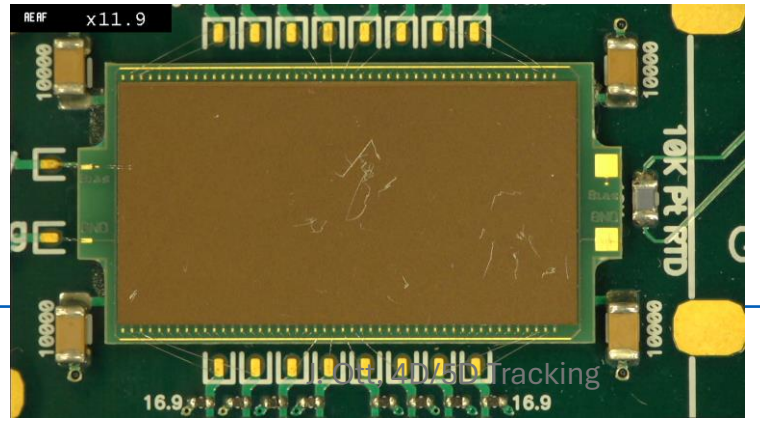


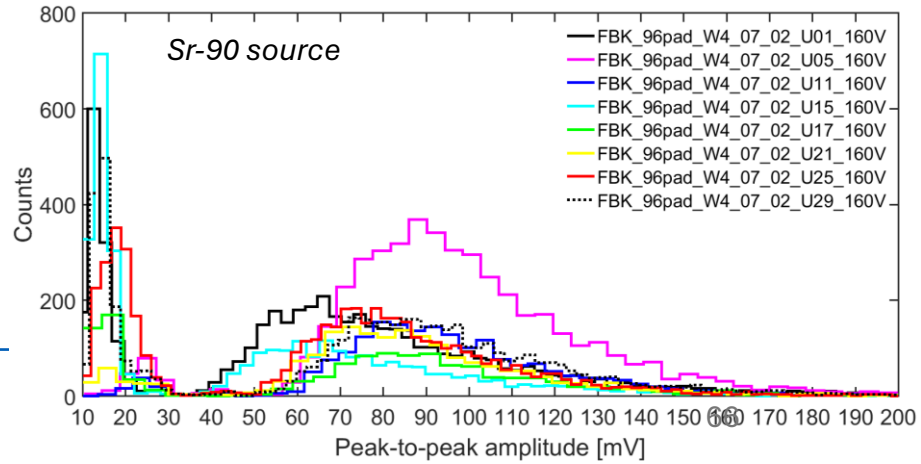
First attempts at bump-bonding and reading out large LGAD sensor prototypes

- Fabrication of interposer PCB
- Gold stud bump deposition on FBK and CNM sensors, flip-chip bonding of sensors to PCB at KIT
- Readout with:
  - *Fermilab fast 16-channel board*
  - *Variant of SKIROC2CMS board adapted to serve 96 LGAD pad channels*









Towards 4D (5D) tracking

Challenge: efficiency

Necessity of fast timing in particular depends heavily on collider type and physics case: e+e- collider does not have significant pileup, timing resolution of ~tens of ps not strictly needed

Integration of timing into ATLAS inner tracker pixel detector: considerable improvements, but has not been subjected in a full technical study

Weighing of 'cost' of additional timing resolution: power consumption of electronics → cooling → additional material budget. Additional information → data transmission → memory, transmission rates; trigger latency?

Extreme conditions in future colliders

HL-LHC

- Max. fluence on silicon detectors ~3×10^{16} n_{eq}/cm^2
- Pileup ~200, for mitigation: timing resolution < 50 ps

Future colliders

- Fluence on inner layers up to 7×10^{17} n_{eq}/cm^2 (FCC)
- Similar pileup conditions to HL-LHC
- Desired resolution: 1-3 µm (lepton colliders)
- Material budget: down to 1% X_0

Silicon detectors in future particle physics experiments

Efficient tracking (in 4D)

- **Timing resolution**
  - Silicon sensors with gain
  - 3D detectors
- **Improved spatial resolution**
  - Small pixels
  - 3D detectors
- **Operation at extreme fluences**
  - Radiation tolerance of material
  - Sensor design (incl. thickness)
- **Efficient manufacturing and operation**
  - Low mass
  - Large area, low cost, low power consumption
  - Challenging interconnection technology

CMOS sensors?

Challenge for LGADs: segmentation, spatial resolution

Limitation of traditional LGADs: termination of the electric field at pad edges, interpad gap (cf. above!)

Mitigation, solution:

- insulation with trenches
- **utilizing charge sharing to improve spatial resolution: AC-LGADs**
- bury the high electric field region = the gain layer deeper into the bulk
  - Deep-junction LGAD: UCSC Patent

Low gain avalanche diodes

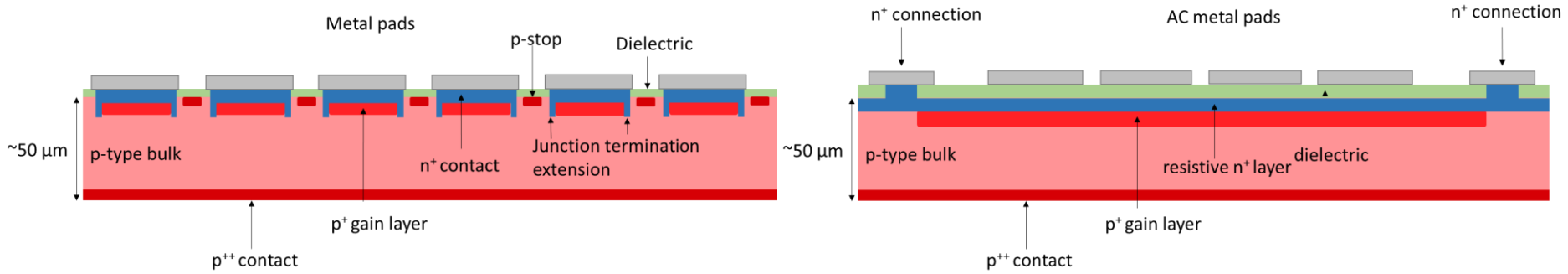
Silicon low-gain avalanche diodes (LGADs) are studied by the CMS and ATLAS experiments for their endcap timing detector upgrades

- Thin sensors, typical thickness 50 µm
- Low to moderate gain (5-50) provided by p^+ multiplication layer

➢ Timing resolution down to ca. 20 ps

➢ Good radiation hardness up to 10^{15} n_{eq}/cm^2

A more recent development: AC-coupled LGAD



H. F.-W. Sadrozinski et al, *4D tracking with ultra-fast silicon detectors*, Reports on Progress in Physics 2018, 81, 026101

CMS Collaboration, *A MIP Timing Detector for the CMS Phase-2 Upgrade*, CERN-LHCC-2019-003, 2019

ATLAS Collaboration, *A High-Granularity Timing Detector for the ATLAS Phase-II Upgrade*, CERN-LHCC-2018-023, 2018

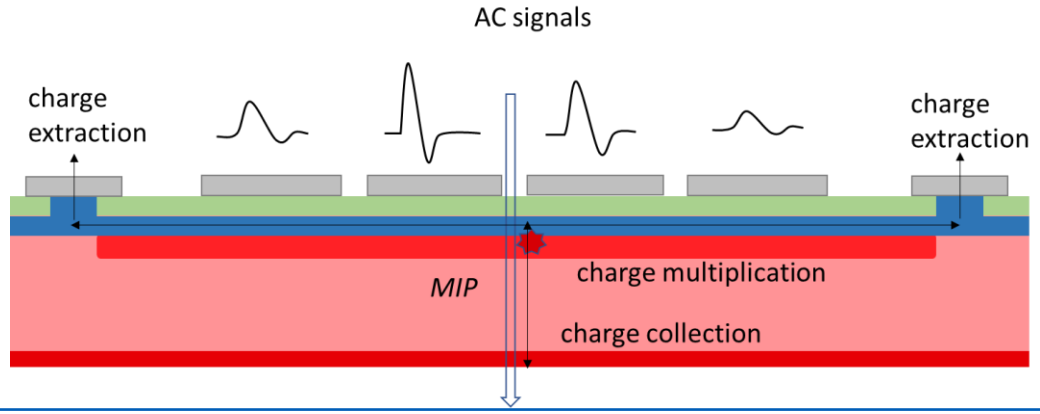
AC-coupled low gain avalanche diodes

In AC-coupled LGADs, also referred to as Resistive Silicon Detectors (RSD), the multiplication layer and n^+ contact are continuous, only the metal is patterned:

- The signal is read out from metal pads on top of a continuous layer of dielectric
- The underlying resistive n^+ implant is contacted only by a separate grounding contact
- No junction termination extension: fill factor ~100

The continuous n^+ layer is resistive, i.e. extraction of charges is not direct

- Mirroring of charge at the n^+ layer on the metal pads: AC-coupling
- Strong sharing of charge between metal pads
- **Extrapolation of position based on signal sharing – finer position resolution for larger pitch, also allowing for more sparse readout channels**



G. Giacomini *et al.,* Fabrication and performance of AC-coupled LGADs, *JINST* **2019**, 14, P09004

A. Apresyan *et al.,* Measurements of an AC-LGAD strip sensor with a 120 GeV proton beam**,** *JINST* **2020**, 15, P09038

S. M. Mazza, An LGAD-Based Full Active Target for the PIONEER Experiment, *Instruments* **2021**, *5*(4), 40

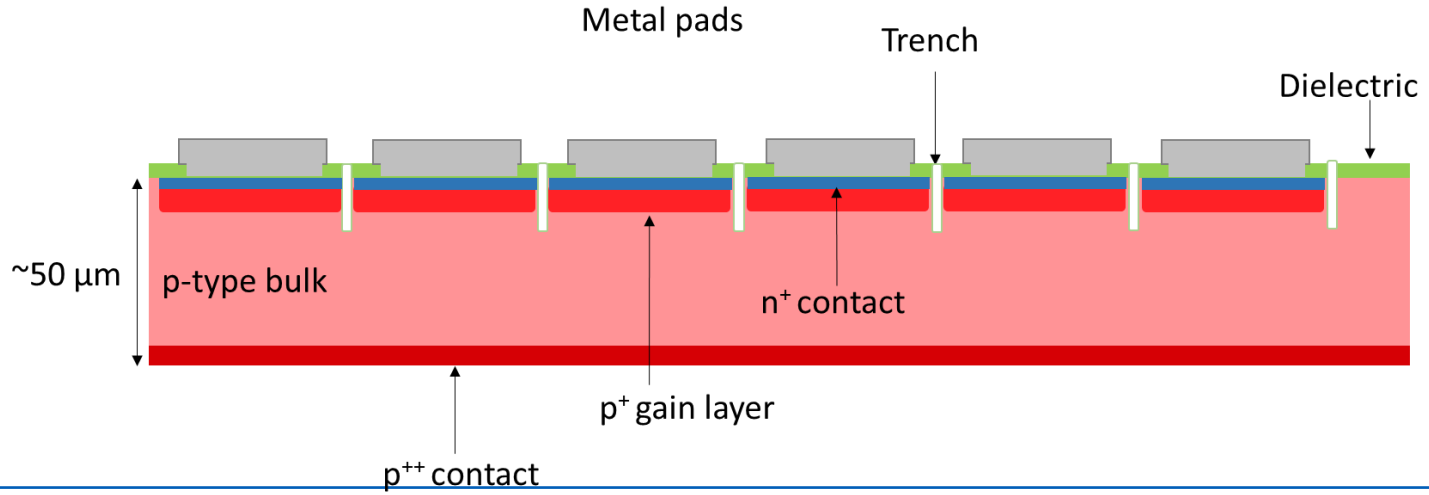
Trench-insulated LGADs

Rely on direct readout from metal pads and segmented gain layer in the same way as standard LGADs

Gain layer is not terminated electrically by an implant, but with etched trenches (fabricated e.g. by Reactive Ion Etching)

- Very high fill factor, 99-100%
- No charge sharing

Relatively early stage of prototyping: focused on small pad arrays, no long strip sensor prototypes yet

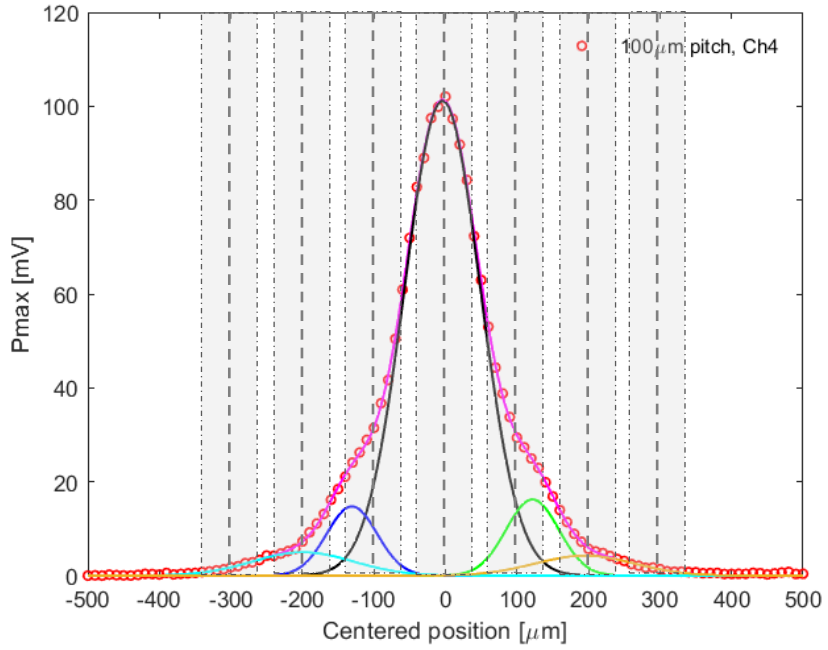


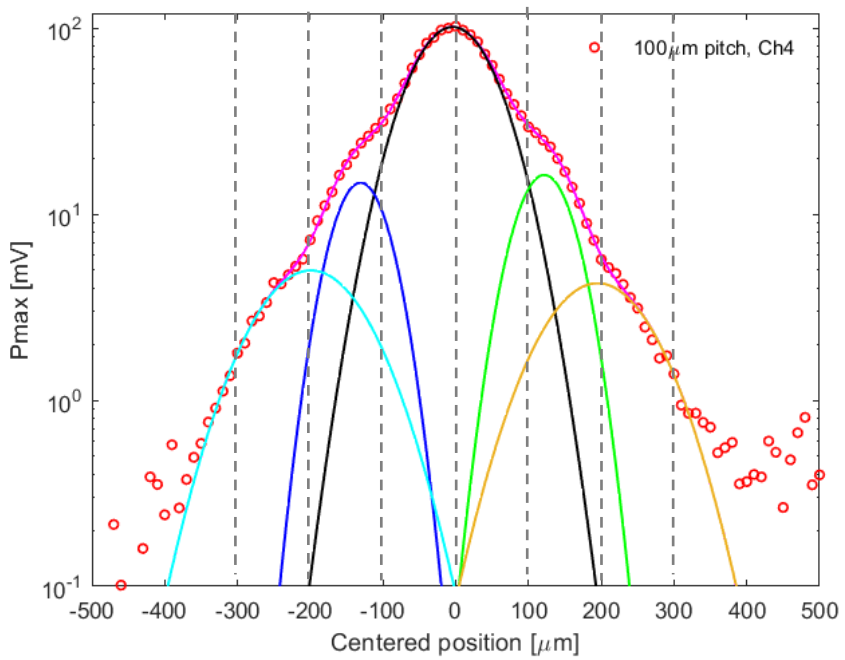
Charge on neighboring strips

Closer examination of the individual strips' pmax profiles reveals contribution from next and even second neighboring strip

Actual sharing extends from the central strip almost to the far edge of the next neighbor

- Localization indicates **induced** charge on the neighboring strips, not purely conduction through the resistive n^+ layer





Narrow, 100 μm pitch

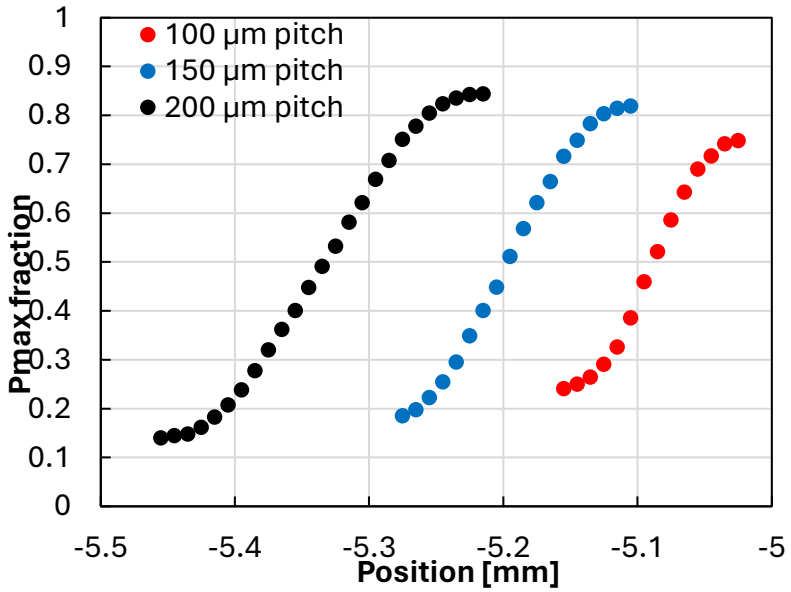
Position resolution in BNL 2021 AC-LGAD strips

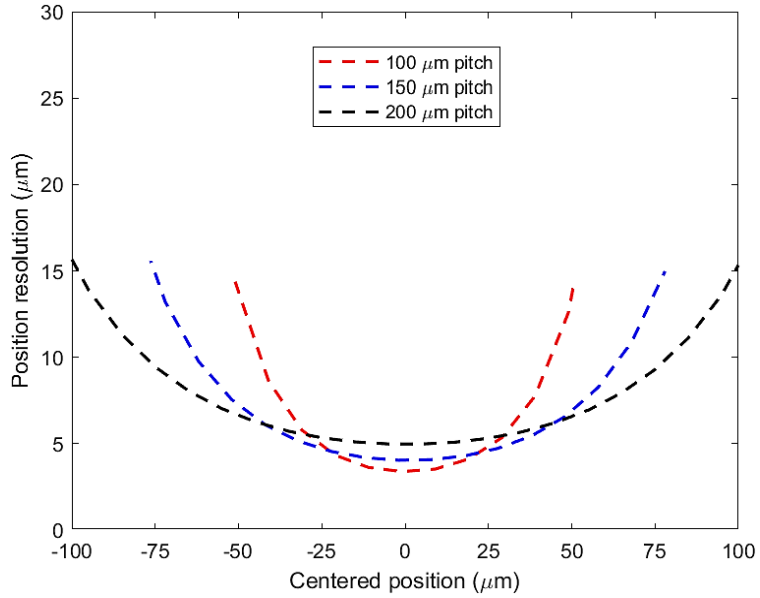
Strip pitch is expected to - and appears to - have a large impact on charge sharing as seen in the pmax fraction profile …

… position resolution of ca. 15 µm at the respective strip metal centers (end of the data points in the plot): in fact very similar for all three pitches

Between strips, a position resolution of ~6 µm or less is reached; slightly better for smaller pitch

- **At best, < 1/20 of the pitch**





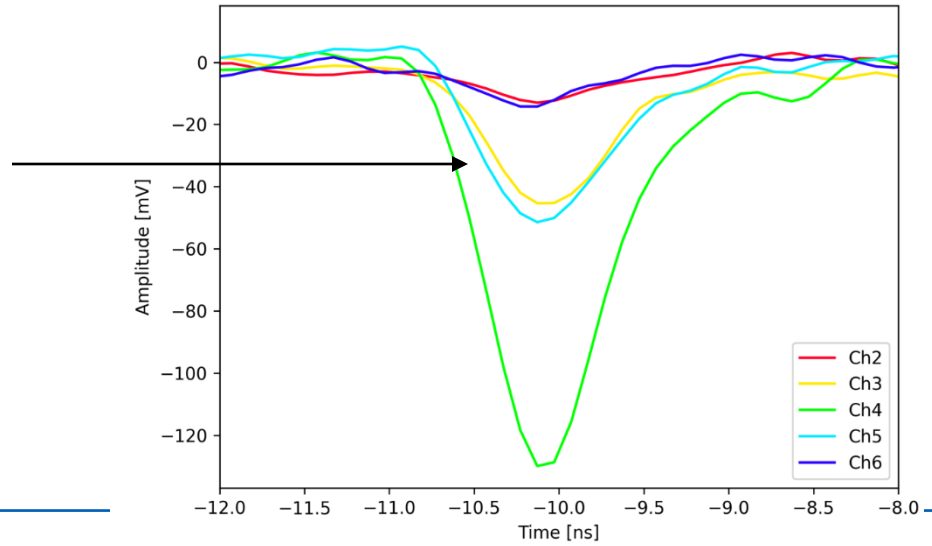
Timing resolution

$$\sigma_t^2 = \sigma_{Landau}^2 + \sigma_{Jitter}^2 + \sigma_{TimeWalk}^2 + \sigma_{TDC}^2 + \sigma_{Distortion}^2$$

AC-LGADs provide comparable performance to conventional LGADs, determined by largely by the gain layer: < 40 ps established, 20 ps reachable

Impact of signal sharing on timing resolution:

- Weighted reconstruction of several contributions can improve timing resolution
- But: lower signal in individual segment increases rise time and reduces signal-to-noise ratio (and thus timing resolution through the jitter component)

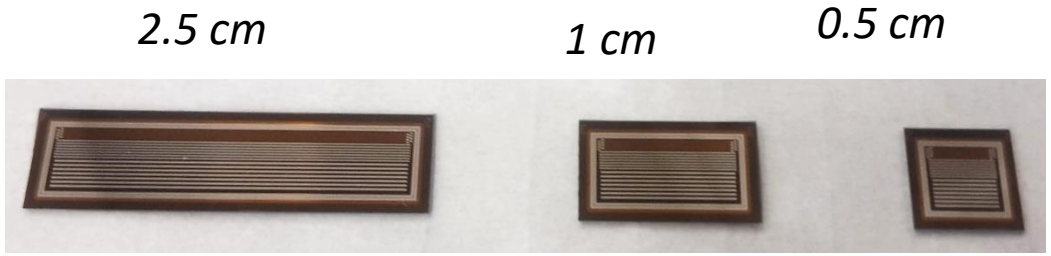


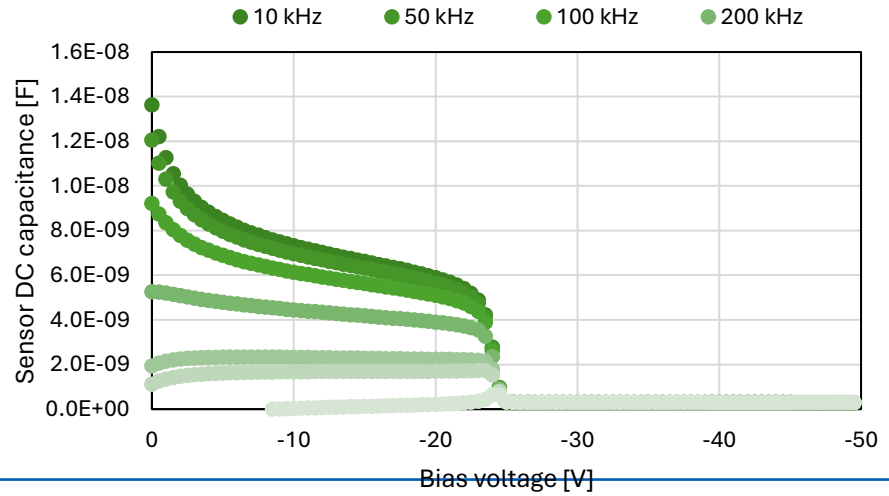
J. Ott et al, AC-LGAD 4D tracking and electrode geometry, Pixel2022

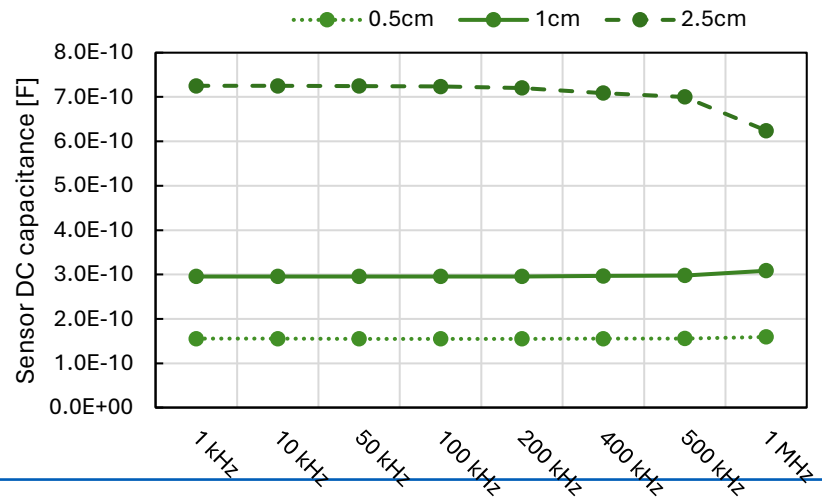
Multipitch strips: sensor capacitance

For reference: capacitance of the full sensor, n^+ to backplane ('DC configuration')

- No dependence on measurement frequency after bulk has been depleted of charge carriers



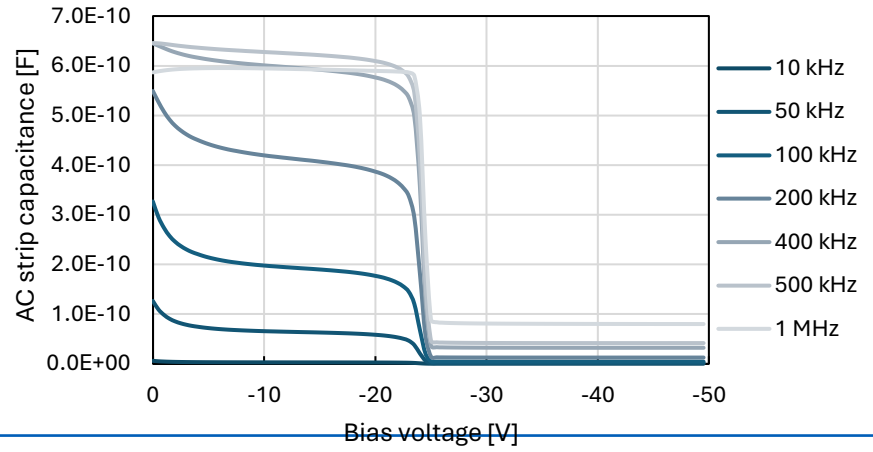


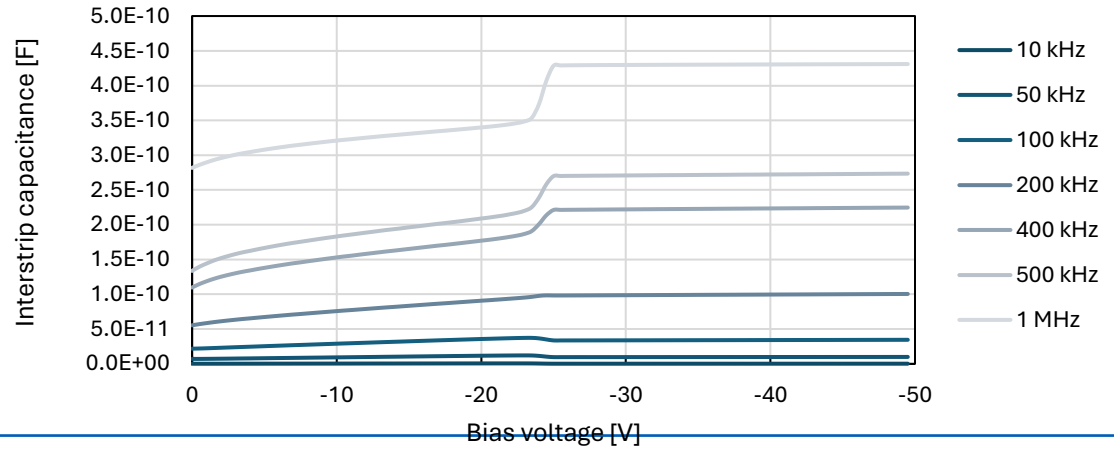


AC strip and interstrip capacitances

- Very different picture when measuring AC component(s): AC strip electrode to backplane, or between AC strips
  - ➢ Frequency dependence, and inverse correlation of frequency and capacitance

- Depletion is still observed: contribution to these capacitances not only by surface, metal or dielectric
- Interstrip capacitance is larger than strip capacitance itself





J. Ott et al, AC-LGAD 4D tracking and electrode geometry, ...

1 cm strip length; 200 um pitch = 100 um metal

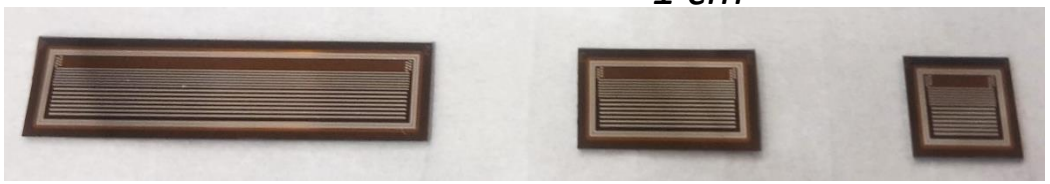
Capacitances as function of strip length and width

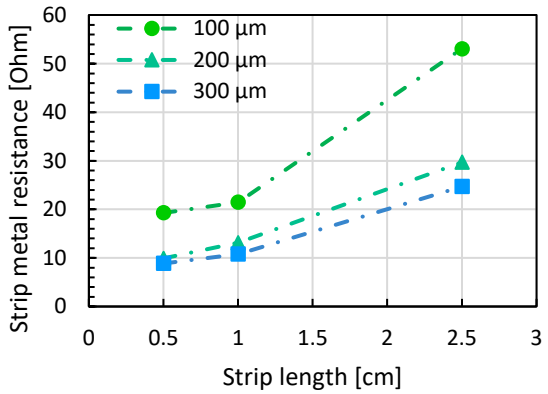
100 kHz

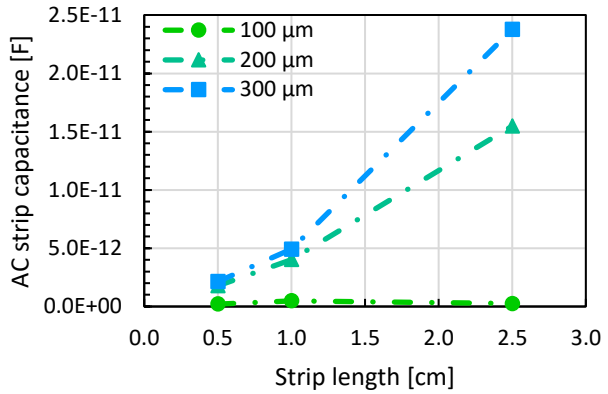
300-150

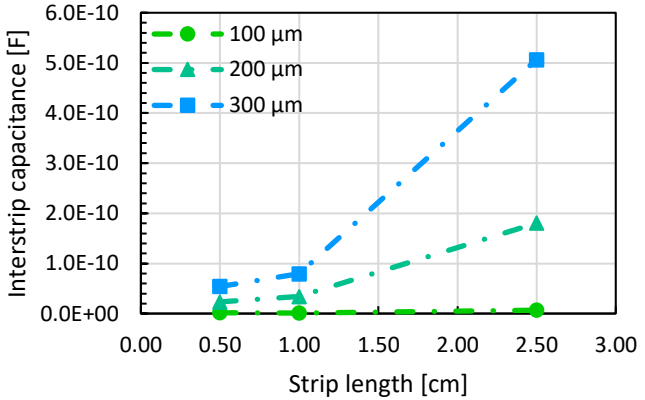
200-100

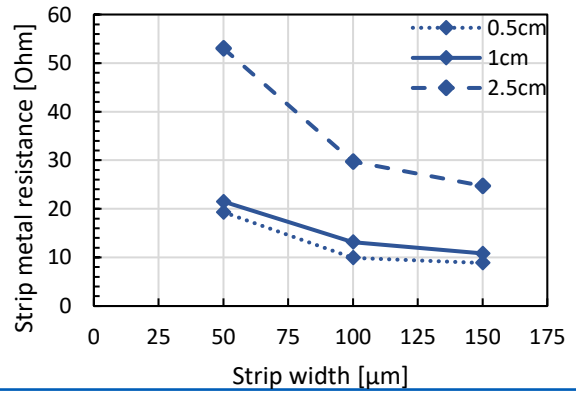
100-50

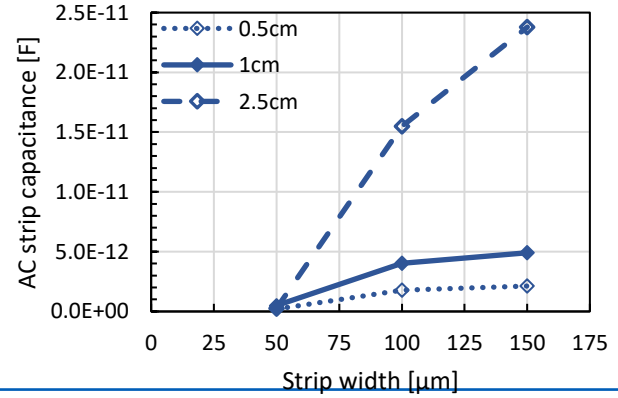


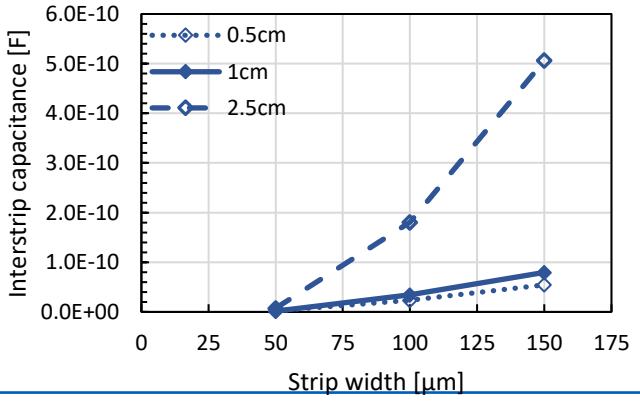












Laser studies on charge sharing in AC-LGADs

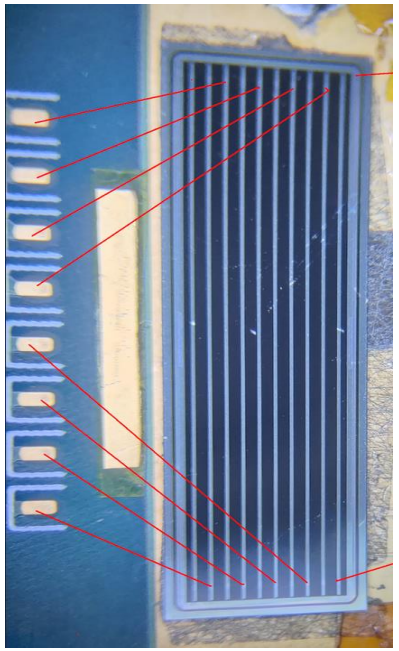
Set of HPK sensor prototypes for the EIC: measured by infrared laser scanning TCT

- Focus on 50 μm strip width

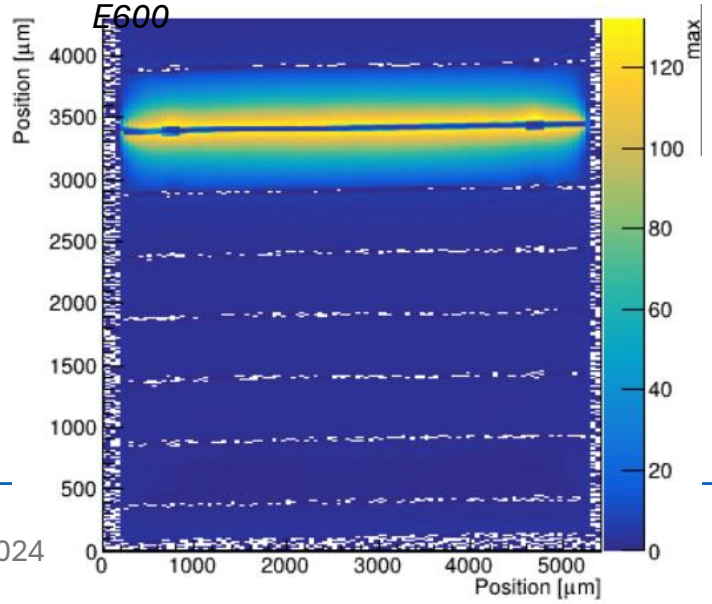
Averaged waveform at each x-y point

Time-of-arrival information and jitter based on laser reference

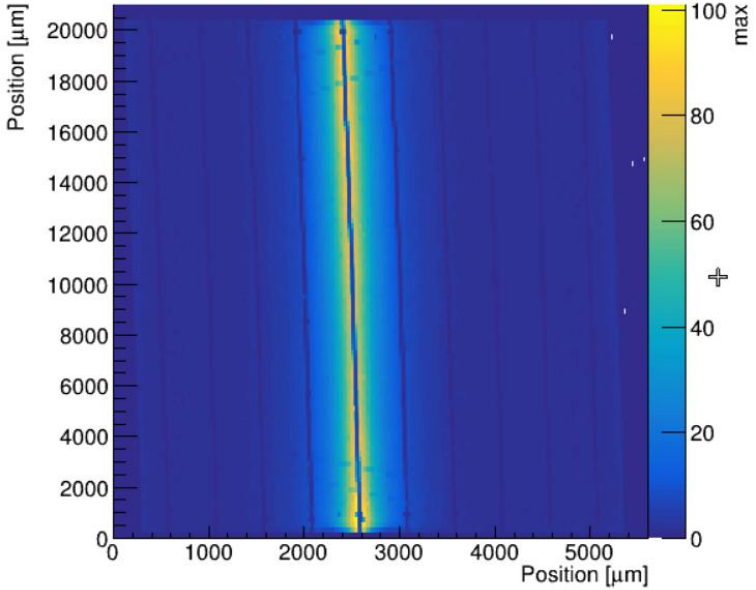
Monitoring of sensor response uniformity, gain 'hotspots'



5 mm length, 50 μm thickness, E600



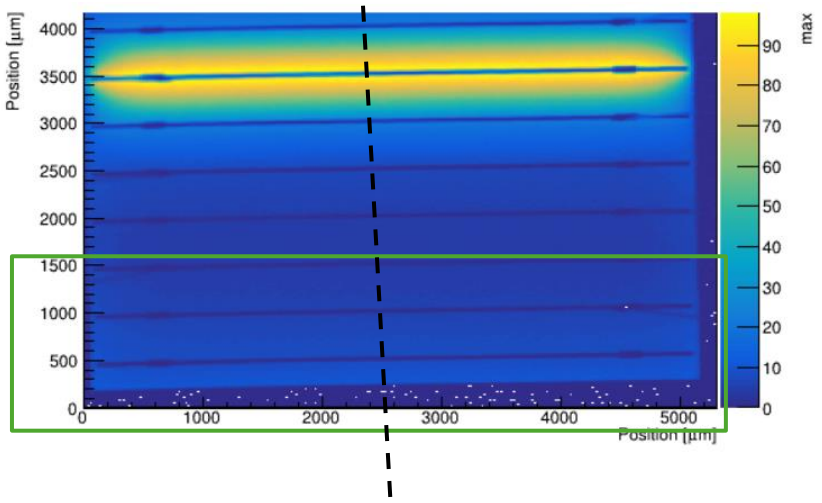
20 mm length, 20 μm thickness, E600

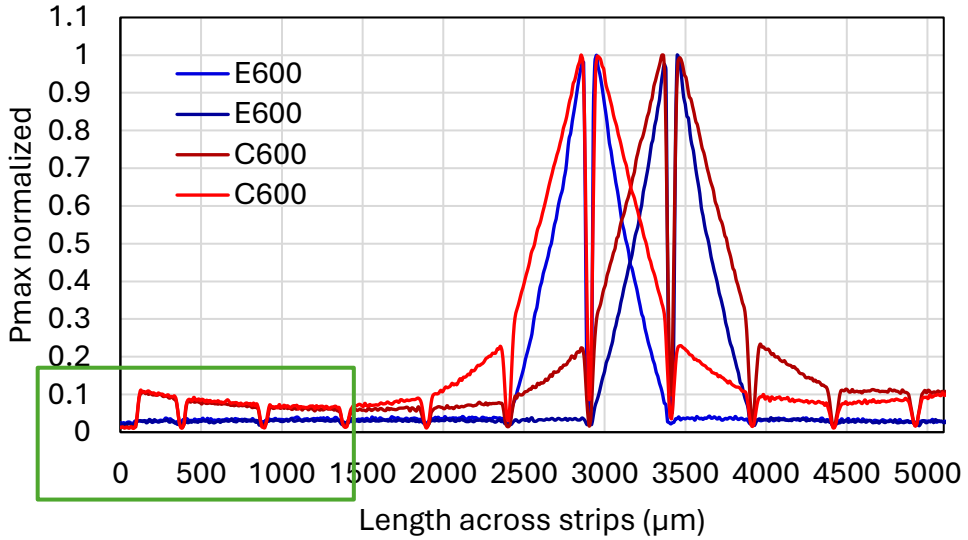


HPK strip sensors: n-layer resistivity

- **Expected to be one of the most important parameters in AC-LGADs**
- **Not fully conclusive results in earlier sensors**

- Effect very clearly visible in the HPK production: show-stopper for strip sensors, however increased sharing may be needed in small pad sensors in order to not lose efficiency at the relatively large 500 µm pitch
- Significant long-distance sharing in the “C” type sensor, increasing towards the edge n-layer contact: how would this affect larger – in this case wider – sensors even if strip length is restricted?





Challenge: radiation damage

LGADs (regardless of what structural variant) suffer from degradation of the gain due to deactivation of acceptors

Can be addressed to some extent by gain layer and defect engineering:

- **Different dopant: e.g. Ga instead of B**
  - Not successful
- **Carbon co-doping**
  - Successful at reducing gain layer deactivation
- **Partially activated boron**
  - More recent; very mixed results for different vendors

Challenge: timing resolution, fabrication

Thin sensors

- Recent productions from several vendors with 20 µm thickness
- Balance: reduction of Landau fluctuation floor in timing resolution, higher electric field, vs gain curve is steeper than thicker substrates, finding suitable (stable) operating point is more sensitive

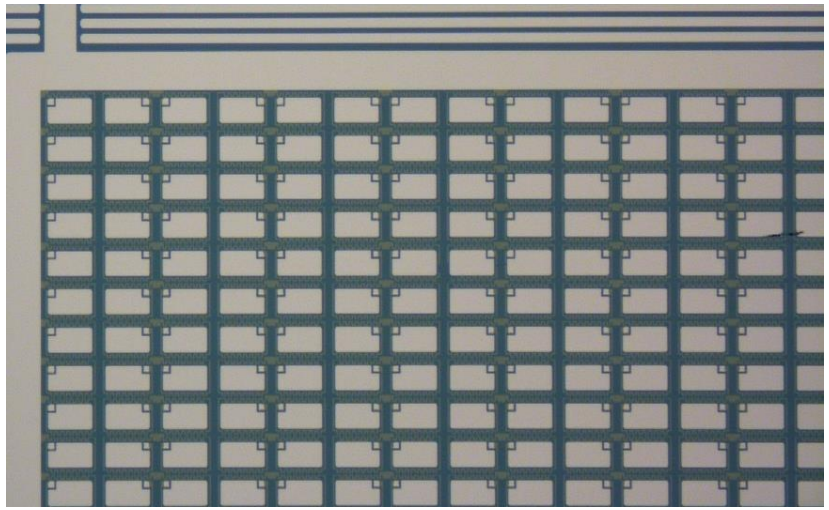
Reduction of interconnect: 3D integration (wafer-wafer bonding) or integrating gain layer into CMOS process

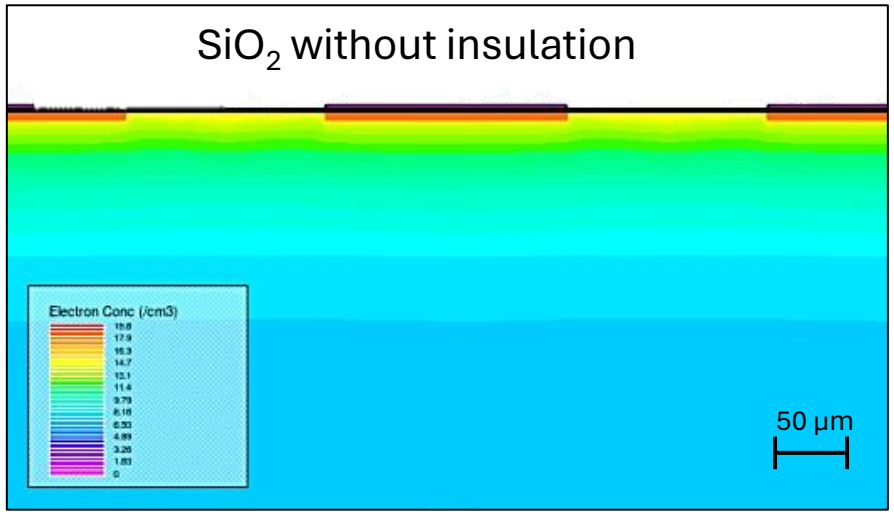
- Strong consensus among US groups, active interest in DRD 3 on these technologies

Thin films in semiconductor detectors

Why aluminium oxide?

- Increased use of p-type Si in detectors for high-luminosity environments
- Higher mobility of electrons in Si → segmentation of n^+ implants
- SiO_2 with its positive oxide charge does not insulate the segments without additional p-spray/p-stop implant

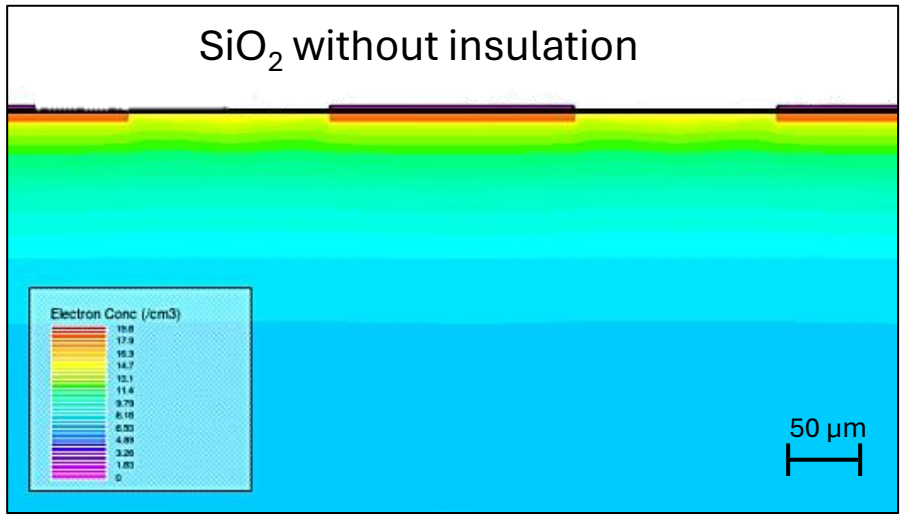


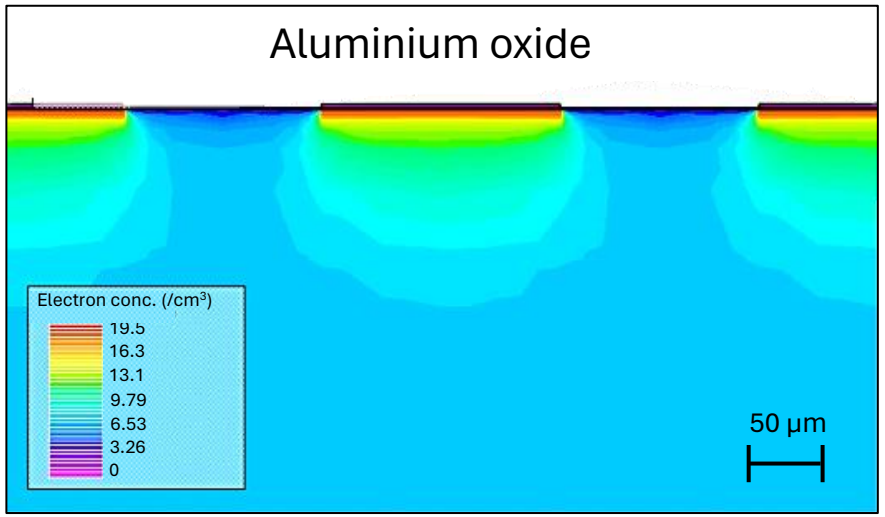


Why aluminium oxide?

Aluminium oxide (Al_2O_3)

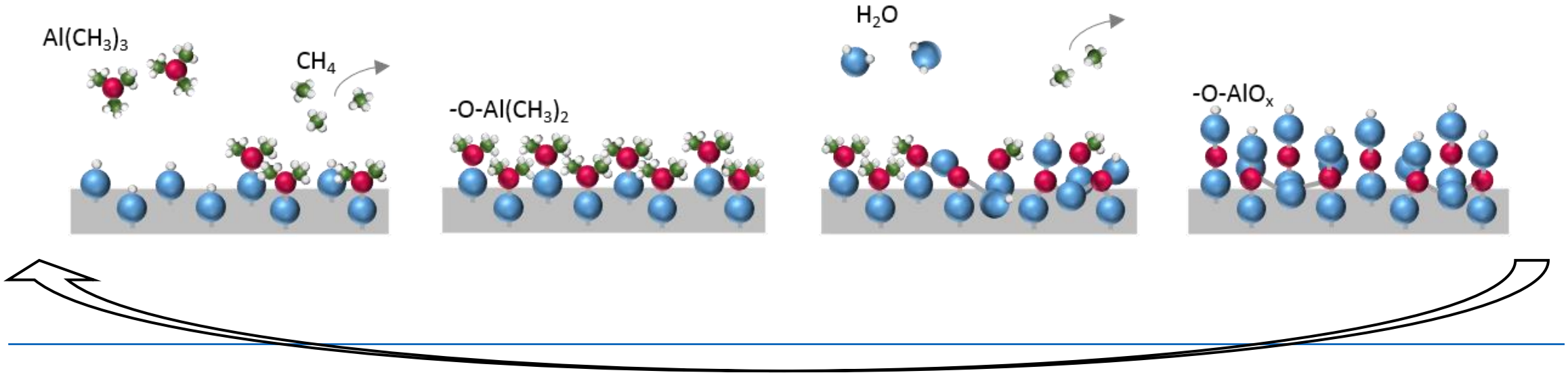
- High **negative** charge (~ 10^{12} cm^{-2})
- Can be deposited at low temperature
- Good dielectric properties - allows for higher oxide capacitances





Atomic layer deposition

- A film is deposited by alternate pulsing of gaseous precursors over a substrate
- No gas-phase reactions, purges between the precursor pulses → self-limiting surface reactions



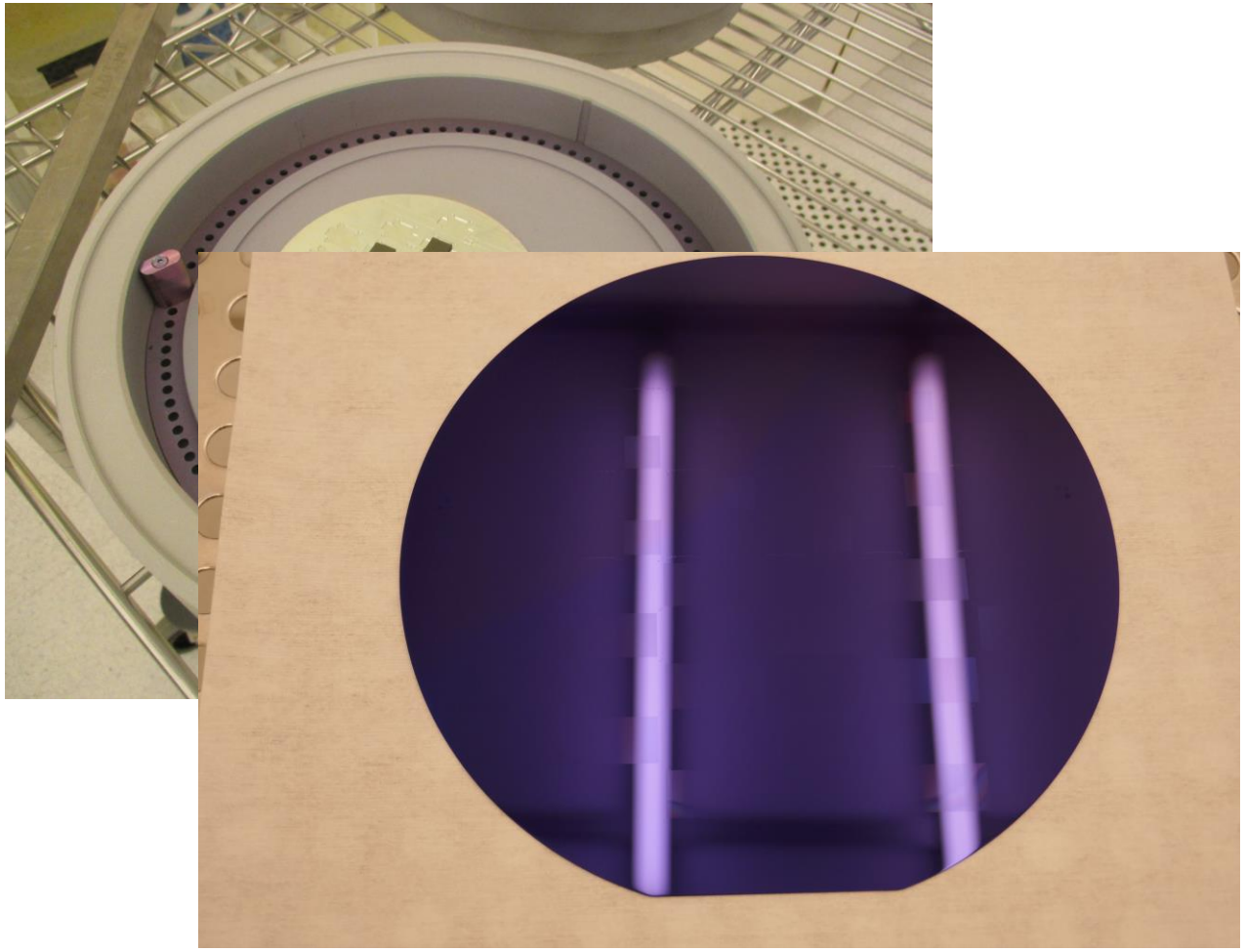
Atomic layer deposition

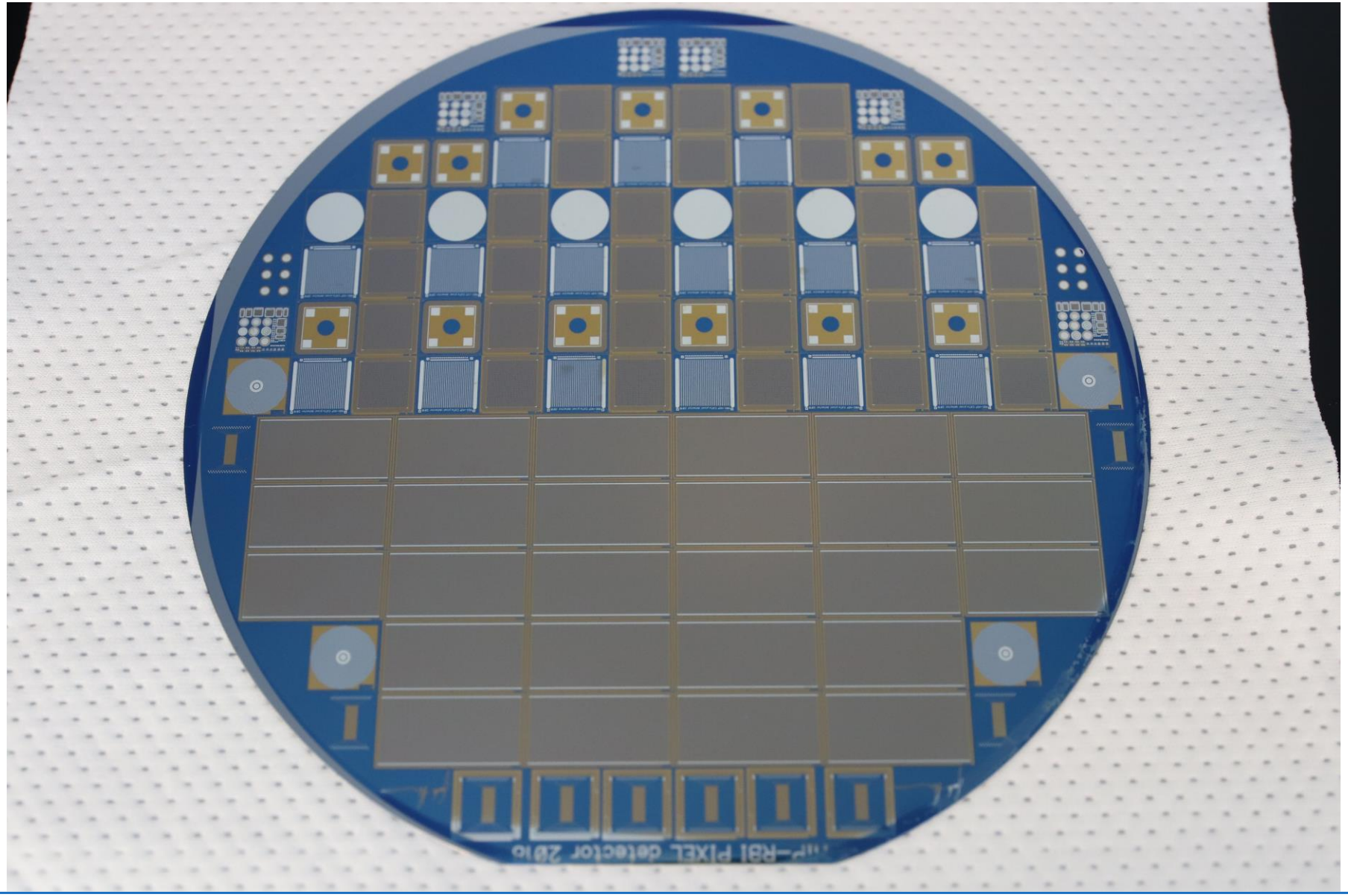
- A film is deposited by alternate pulsing of gaseous precursors over a substrate
- No gas-phase reactions, purges between the precursor pulses → self-limiting surface reactions

- Film growth slow and occuring in cycles → very thin layers can be grown with good precision
- Good film uniformity over relatively large areas, conformal growth

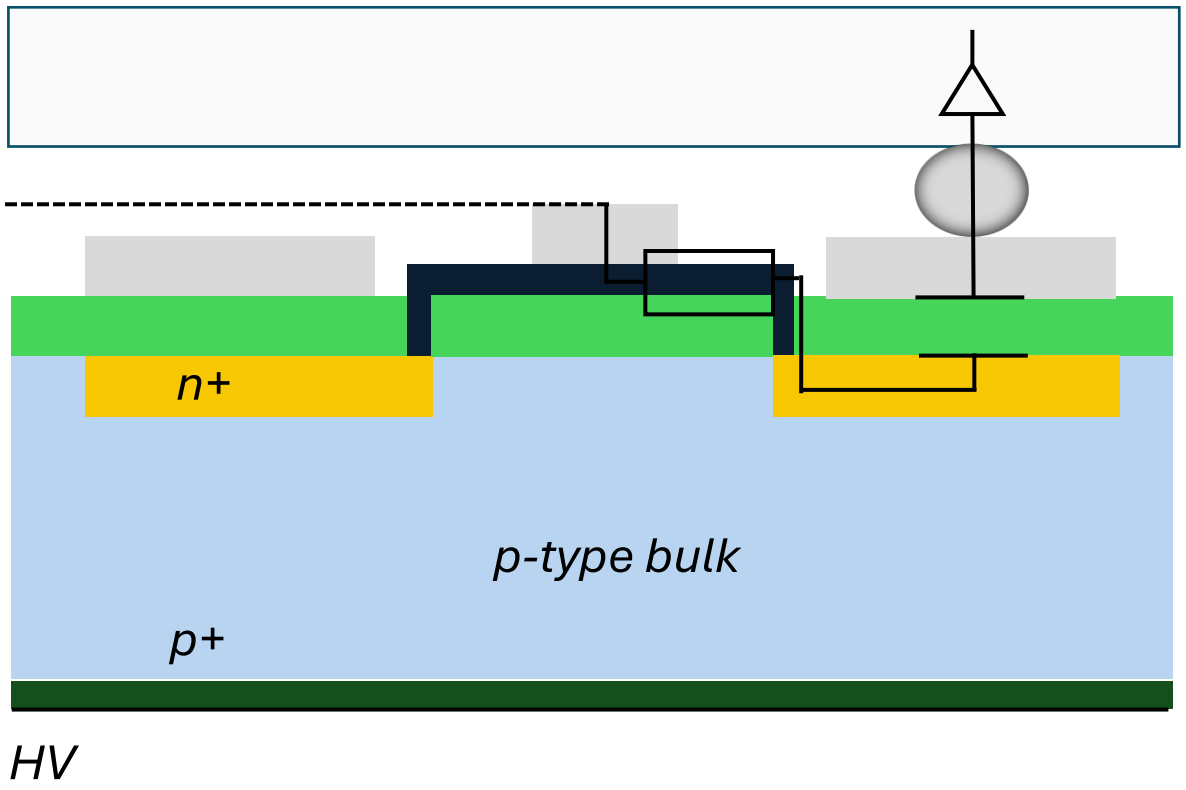
Atomic layer deposition

Beneq.com




HP-R&I PIXEL detector 2016

AC-coupled pixel sensor



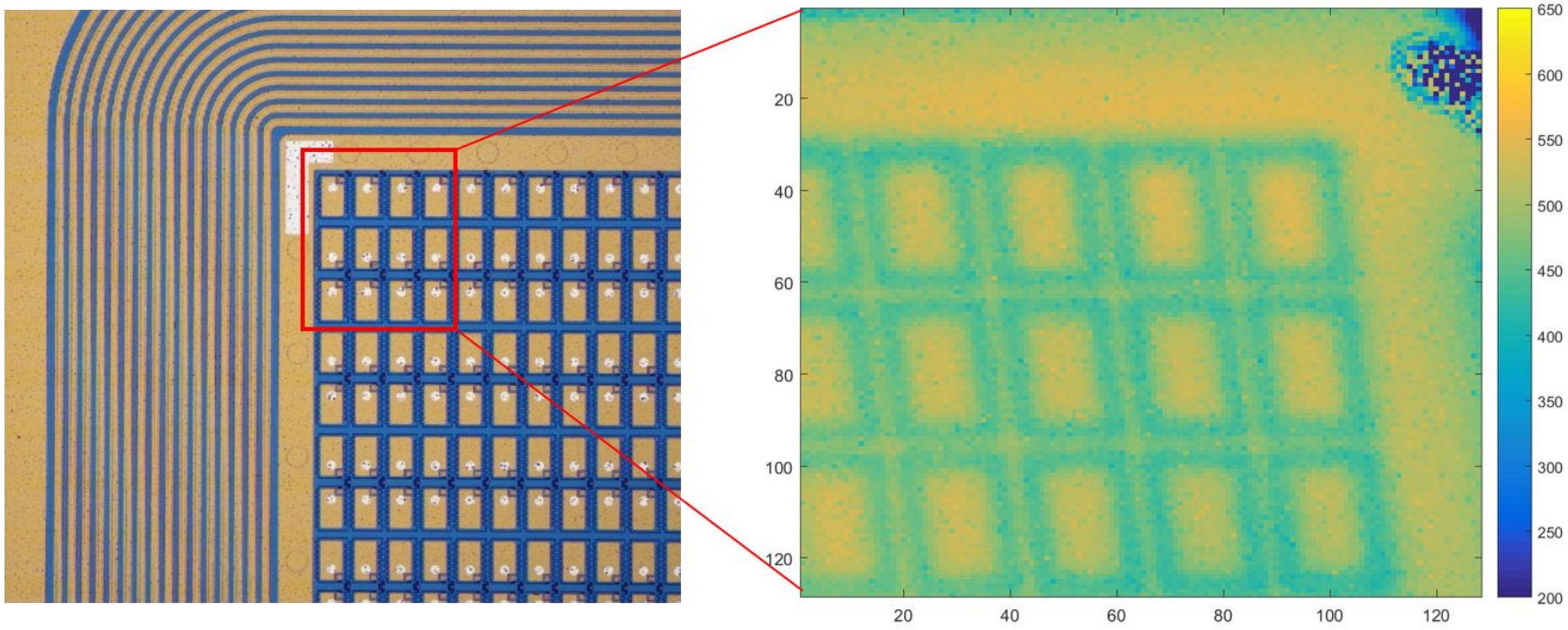
For 100×150 µm area:

C_{ox}: 12.3 pF

Drawing not to scale

C_{Si}: 6 fF

AC-coupled pixel sensors



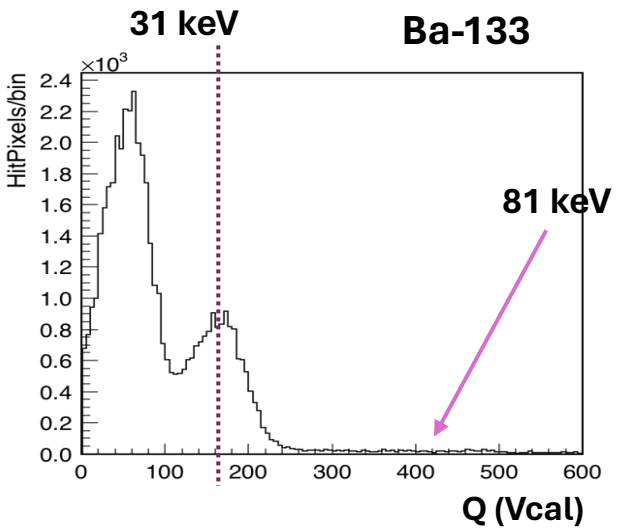
Proton microbeam image of a PSI46dig-geometry AC-coupled pixel sensor with Al_2O_3 insulator

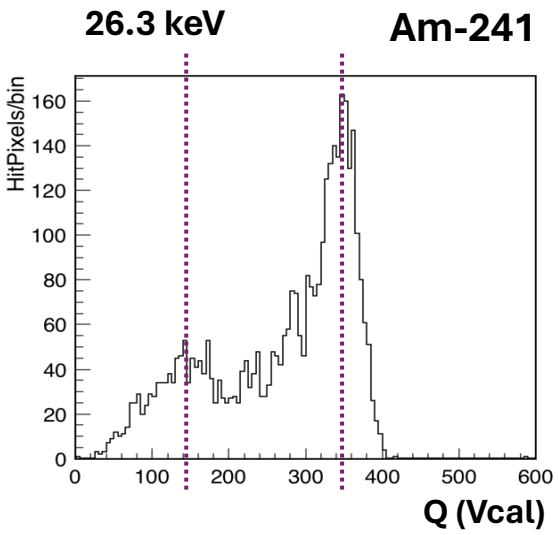
J. Ott et al, *Processing of AC-coupled n-in-p pixel detectors on MCz silicon using atomic layer deposition (ALD) grown aluminium oxide*, Nuclear Instruments and Methods in Physics Research A (2020), 958, 162547

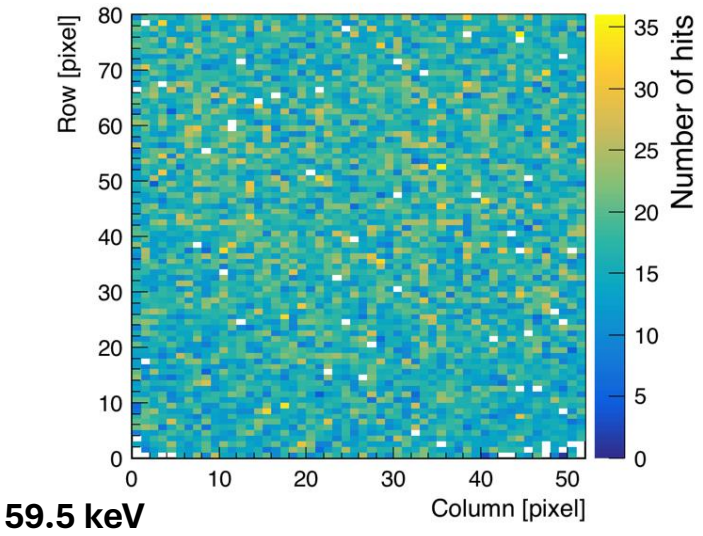
AC-coupled pixel detectors

Testing with radioactive sources

- Typically 10-20 dead pixels / assembly: < 0.5 %
- Similar number of hot or noisy pixels masked







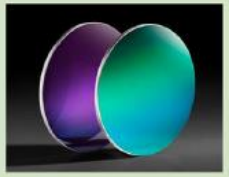
A. Gädda, **J. Ott** et al, *AC-coupled n-in-p pixel detectors on MCz silicon with atomic layer deposition (ALD) grown thin films*, Nuclear Instruments and Methods in Physics Research A (2021), 986, 164714

Thin film materials as charged particle detectors?

Summary & Our Vision

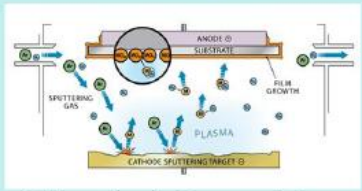
14/15

Completed



Single Crystal Substrates

Chemical Deposition



Physical Deposition

Ultimate Goal

Roll-to-roll Technology

Pilot Study

- Screen/test candidate crystalline materials
- Test and analyze detector performance (source/test beam)

Phase-II

- In-house thin film InP
- Optimize deposition process
- Fabricate detectors, repeat testing and analysis

The Vision & Goal

- **Quick & easy** to manufacture
- **Inexpensive**
- **Easy assembly** into large-scale detector
- Similar 'sensor' performance to **Silicon technologies**

R&D Direction

- *Different materials*
- *Monolithic detector design*
- *Large-area production*

⇒ ***US groups are in a position*** *to* ***lead the solid-state detector R&D efforts***

CPAD Workshop 2023 – Sungjoon Kim

https://www.mks.com/n/cvd-physics

S. Kim et al, CPAD 2023, https://indico.slac.stanford.edu/event/8288/contributions/7503/

S. Kim, V. Berry, J. Metcalfe, A.V. Sumant, Thin film charged particle detectors. *JINST* **18**, (2023)

Thin film materials as charged particle detectors?

InP has favorable properties: especially electron mobility, which is higher than in Si

Chosen as a commercially available small wafer material and crystalline reference to (amorphous) future thin film devices

TABLE I

PROPERTIES OF SEMICONDUCTOR MATERIALS AT 25°C

Material	Atomic Number	Density g/cm³	Band-gap eV	Melting Point °C	Knoop Hardness	Crystal Structure	Ionicity	Dielectric Constant
Ge	32	5.33	0.67	958	692	Cubic	0	16
Si	14	2.33	1.12	1412	1150	Cubic	0	11.7
CdTe	48, 52	6.2	1.44	1092	45	Hexagonal	0.61	11
CdZnTe	48, 30, 52	≈ 6	1.5–2.2	1092–1295				
CdSe	48, 34	5.81	1.73	>1350		Hexagonal	0.6	10.6
CdZnSe	48, 30, 34	≈ 5.5	1.7–2.7	1239–1520				
HgI_2	80, 53	6.4	2.13	250 (127†)	<10	Tetragonal	0.67	8.8
TlBrI	81, 35, 53	7.5	2.2–2.8	405–480	40	Cubic		
GaAs	31, 33	5.32	1.43	1238	750	Cubic	0.23	12.8
InI	49, 53	5.31	2.01	351	27	Orthorhombic	0.8	26
GaSe	31, 34	4.55	2.03	960		Hexagonal	0.53	8
diamond	6	3.51	5.4	4027	10^4	Cubic	0	5.5
TlBr	81, 35	7.56	2.68	480	12	Cubic	0.81	29.8
PbI_2	82, 53	6.2	2.32	402	<10	Hexagonal	0.8	
InP	49, 15	4.78	1.35	1057	535	Cubic	0.38	12.5
ZnTe	30, 52	5.72	2.26	1295		Cubic	0.62	9.7
HgBrI	80, 35, 53	6.2	2.4–3.4	229–259	14	Orthorhombic		
a-Si	14	2.3	1.8				0	11.7
a-Se	34	4.3	2.3				0	6.6
BP	5, 15	2.9	2	dl400	4700	Cubic	0.01	11
GaP	31, 15	4.13	2.24	1750		Cubic		
CdS	48, 16	4.82	2.5	1477		Hexagonal	0.58	11.6
SiC	14, 6	3.2	2.2			Cubic		
AlSb	13, 51	4.26	1.62			Cubic		
PbO	82, 8	9.8	1.9	886				
BiI_3	83, 53	5.78	1.73	408		Hexagonal		
ZnSe	30, 34	5.42	2.58			Cubic		8.1

TABLE I (*Continued*)

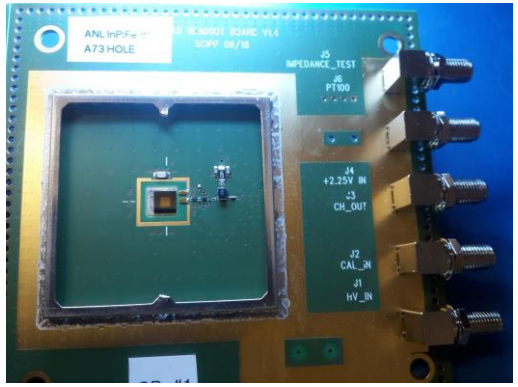
Material	E_{pair} eV	Resistivity (25°C) Ω-cm	Electron Mobility cm²/V · sec	Electron Lifetime sec.	Hole Mobility cm²/V · sec	Hole Lifetime sec.	$\mu\tau(e)$ Product cm²/V	$\mu\tau(h)$ Product cm²/V
Ge	2.96	50	3900	$>10^{-3}$	1900	1×10^{-3}	>1	>1
Si	3.62	up to 10^4	1400	$>10^{-3}$	480	2×10^{-3}	>1	≈1
CdTe	4.43	10^9	1100	3×10^{-6}	100	2×10^{-6}	3.3×10^{-3}	2×10^{-4}
CdZnTe	5.0*	10^{11}	1350	10^{-6}	120	5×10^{-8}	1×10^{-3}	6×10^{-6}
CdSe	5.5**	10^8	720	10^{-6}	75	10^{-6}	7.2×10^{-4}	7.5×10^{-5}
CdZnSe							$\approx 10^{-4}$	
HgI_2	4.2	10^{13}	100	10^{-6}	4	10^{-5}	10^{-4}	4×10^{-5}
TlBrI		10^{10}					9×10^{-5}	
GaAs	4.2	10^7	8000	10^{-8}	400	10^{-7}	8×10^{-5}	4×10^{-6}
InI		10^{11}					7×10^{-5}	
GaSe	4.5		75	5×10^{-7}	45	2×10^{-7}	3.5×10^{-5}	9×10^{-5}
diamond	13.25		2000	10^{-8}	1600	$<10^{-8}$	2×10^{-5}	$<1.6 \times 10^{-5}$
TlBr	6.5	10^{12}	6	2.5×10^{-6}			1.6×10^{-5}	1.5×10^{-6}
PbI_2	4.9	10^{12}	8	10^{-6}	2		8×10^{-6}	
InP	4.2	10^7	4600	1.5×10^{-9}	150	$<10^{-7}$	4.8×10^{-6}	$<1.5 \times 10^{-5}$
ZnTe	7.0**	10^{10}	340	4×10^{-9}	100	7×10^{-7}	1.4×10^{-6}	7×10^{-5}
HgBrI		5×10^{13}					1×10^{-6}	$<1 \times 10^{-7}$
a-Si	4	10^{12}	1	6.8×10^{-9}	.005	4×10^{-6}	6.8×10^{-8}	2×10^{-8}
a-Se	7	10^{12}	.005	10^{-6}	.14	10^{-6}	5×10^{-9}	1.4×10^{-7}
BP	6.5**	1	10	10^{-9}				
GaP	7.0**		120		120			
CdS	7.8**		300		50			
SiC	9.0**		400(α)					
AlSb	5.05	$<10^4$	300		400			
PbO	6.47							
BiI_3	5.5**	10^{12}						
ZnSe	8.0**		100					

Note: Materials are listed in order of decreasing $\mu\tau(e)$ at room temperature.
*Estimated for 20% Zn.
**Estimated.
†Solid/solid phase transition.

Semiconductors for Room Temperature Nuclear Detector Applications

SEMICONDUCTORS AND SEMIMETALS
Volume 43

Crystalline InP sensors

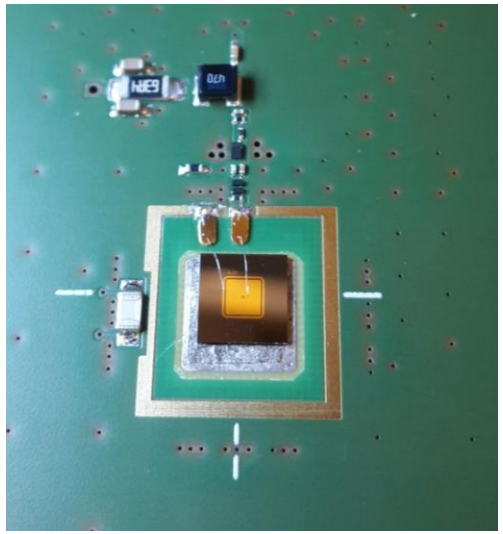


Sensor bonded to 1-ch UCSC fast readout board with 470 Ω transimpedance amplifier, plus external 20dB RF amplifier

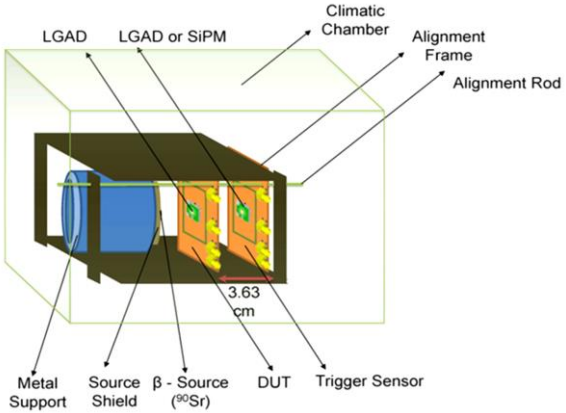
638 nm red laser, x-y scanning stage (Particulars)

Laser intensity adjusted manually to obtain 20 – 30 mV signal

No signal from the IR laser even at high intensities



- Beta source: Sr-90
- Known HPK Silicon LGAD as trigger and reference



Z. Galloway et al 2019

J. Ott, oral presentation, *Characterization of InP sensors for future thin film detectors*, 42nd RD50 Workshop

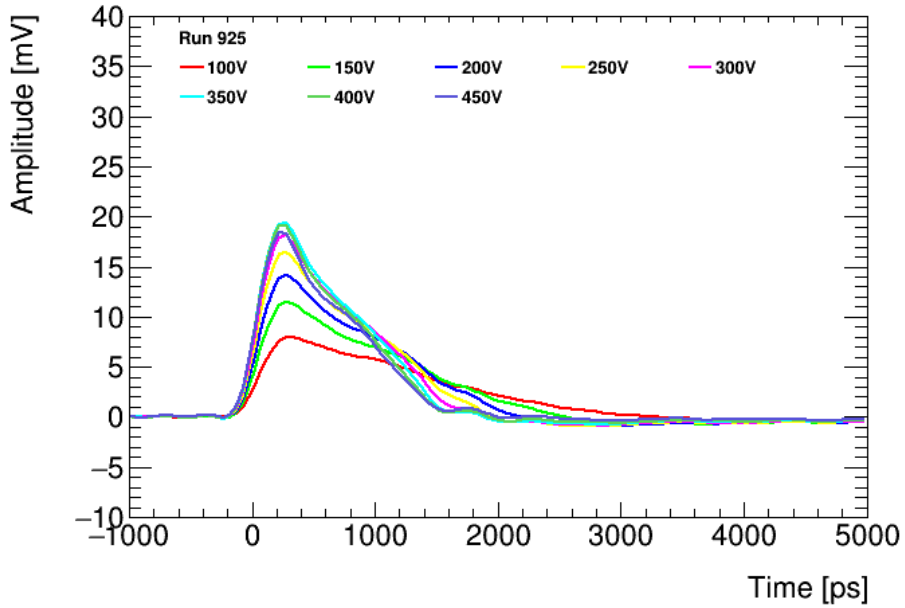
Manuscript in preparation

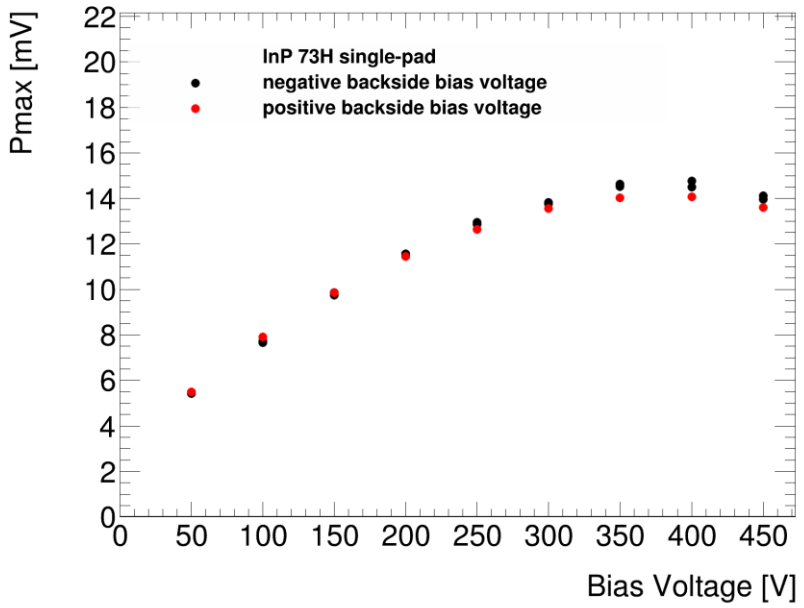
InP tested with Sr-90 beta electrons: signals

Practically independent of bias voltage polarity
- ➢ Expected for homogeneous bulk and unsegmented single-pad electrode

Comparatively small signal, around 15 mV, but fast
- ➢ Similar, to laser signal from assumed hole drift, although a bit lower

Decline after ca. 400 V
- ➢ Similar to laser signal



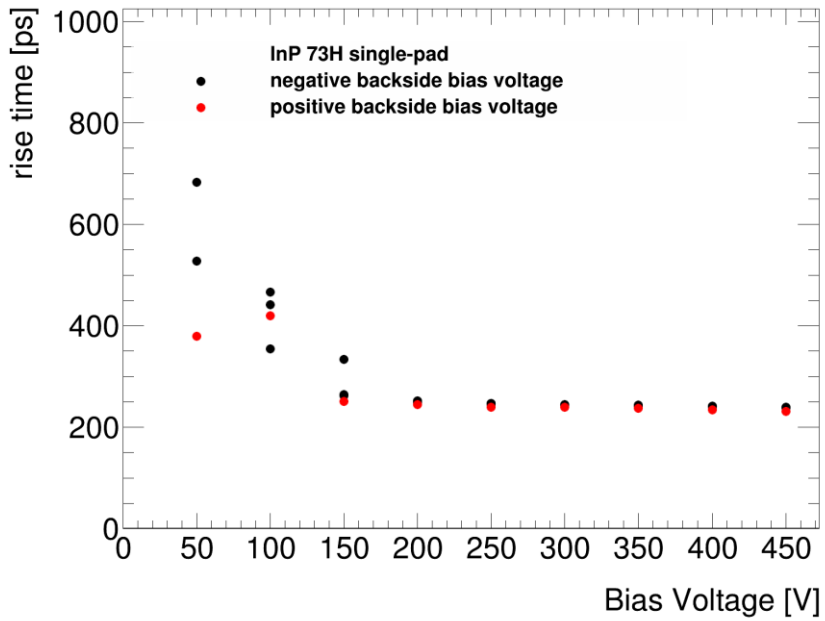


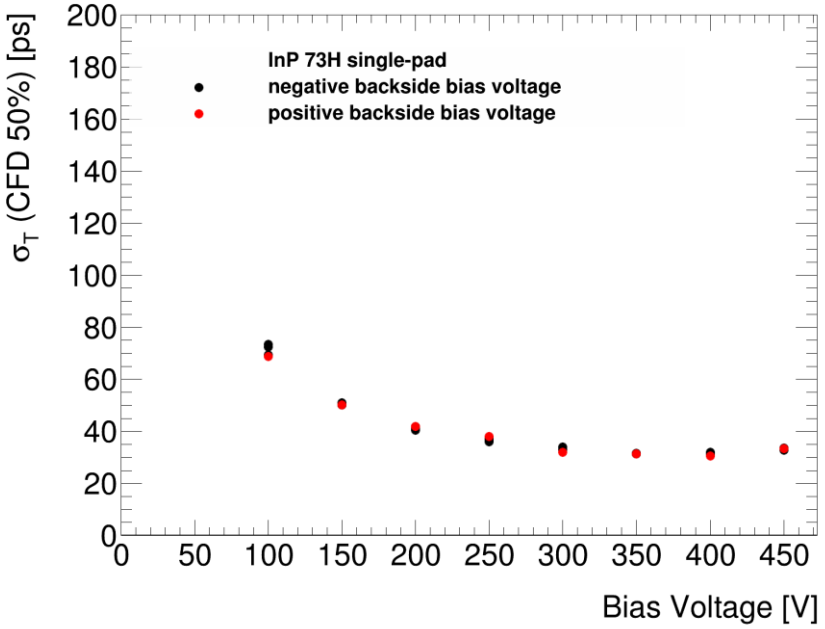
InP tested with Sr-90 beta electrons: rise time and timing resolution

Rise time independent of bias voltage, down to 250 ps after 150 V

Excellent timing resolution: 33 ps reached between 300 and 400 V

- Despite 350 µm-thick device, no special gain layer, relatively small signal!



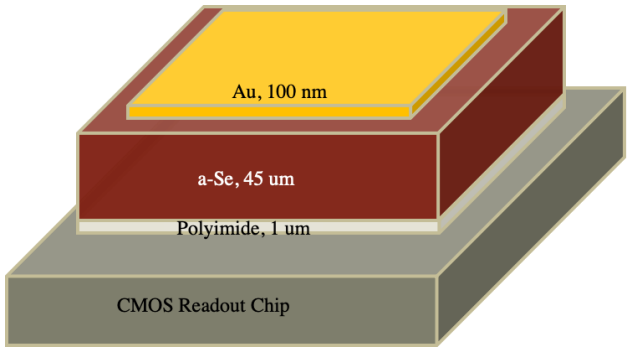


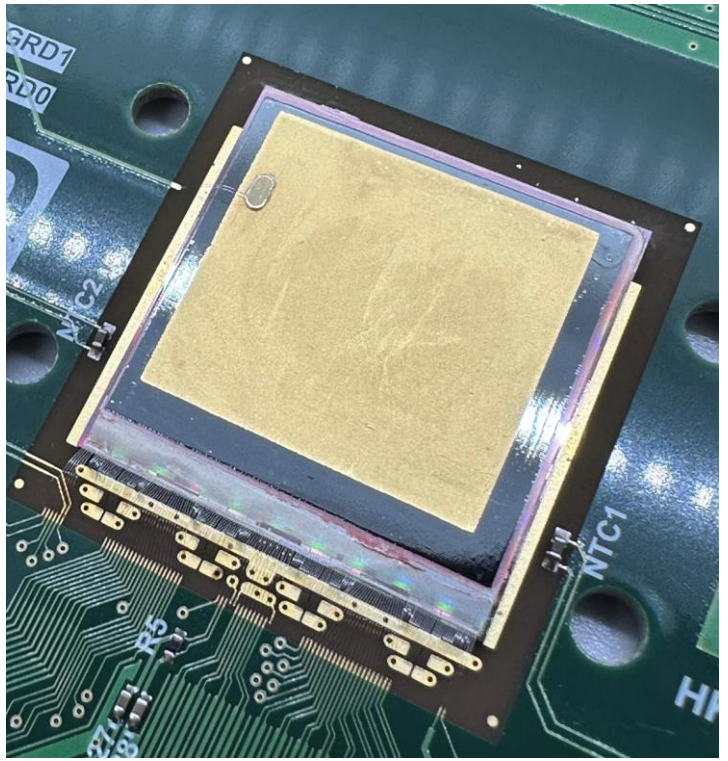
Amorphous Selenium; deposition on ASIC (ITkPix)

aSe is most established as x-ray detector for e.g. mammography panels

Approach here: utilize pixelated ASIC developed for HEP, deposit active sensor material directly on top by relatively low-temperature thermal evaporation

- **Using ITkpixV1.0 (RD53B), V2.0 (sample fabricated, to be measured)**
- **Leveraging expertise with ATLAS pixel modules to set up DAQ, perform chip calibrations and tuning before scans with radioactive source**





A. Swaby, **J. Ott**, K. Hellier, M. Garcia-Sciveres, S. Abbaszadeh, *Hybrid a-Se/RD53B CMOS Detector: Initial Results*, Proceedings of SPIE Medical Imaging (2023), 12463, https://doi.org/10.1117/12.2654519

Backup

Motivation

Precision timing – and 4D tracking – is increasingl**y important for high-energy and nuclear physics experiments**

Large-scale **detector applications require large numbers of segments: depending on the experiment and detector layout, the density of readout channels is high**

Design of fast readout electronics with an acceptable power consumption and cost level is an ongoing challenge

Time-to-Digital Converter (TDC) and time-over-threshold solutions provide only an indirect estimate of integrated charge and are adversely impacted by effects such as time walk, baseline wander, which need to be corrected

➢ **Implementation of on-chip waveform digitization at the GSample level could address these concerns**

Key developments to HP-SoC v2

Assuming 0.4 pF input capacitance

Simulation before any parasitics

In order to achieve timing resolution below 30 ps, it is likely necessary to go to thinner sensors (Landau distribution of charge deposition can only be reduced in this way)

	TIAv1+Gain v1	TIAv2 + follower	TIAv2 + Gain
Gain (signal/ freq=0)	6.48/13 (kOhm)	6.50/9.9(kOhm)	11.9/43(kOhm)
Rin (signal/freq=0)	872/1.4k (Ohm)	177/246 (Ohm)	63/254 (ohm)
Bandwidth	228Mhz	356MHz	129MHz
Rise time	649ps	627ps	691ps
Output bias	357mV	359mV	249mV
Noise (5 GHz)	0.093mV	0.162mV	0.14mV
Current	1.63mA	2.4mA	3.15mA (2.24mA final)
Vpeak (from Base)	92mV	92.3mV	169mV
Estimated jitter (assuming 1 mV total noise)	8.8ps	8.5ps	5.1ps

50 µm (~10 fC signal)

	TIAv1+Gain v1	TIAv2 + follower	TIAv2 + Gain
Gain (signal/ freq=0)	3.05/13 (kOhm)	3.16/9.9(kOhm)	5.15/43(kOhm)
Rin (signal/freq=0)	503/1.4k (Ohm)	117/246 (Ohm)	29.5/254 (ohm)
Bandwidth	228Mhz	356MHz	129MHz
Rise time	348ps	332ps	368ps
Output bias	357mV	359mV	249mV
Noise (5 GHz)	0.093mV	0.162mV	0.14mV
Current	1.63mA	2.4mA	3.15mA (2.24mA final)
Vpeak (from Base)	43.3mV	44.9mV	73.6mV
Estimated jitter (assuming 1 mV total noise)	10ps	9.24ps	6.24ps

20 µm (~4 fC signal)

Power consumption estimate

TIA (with gain): 2.24 mA

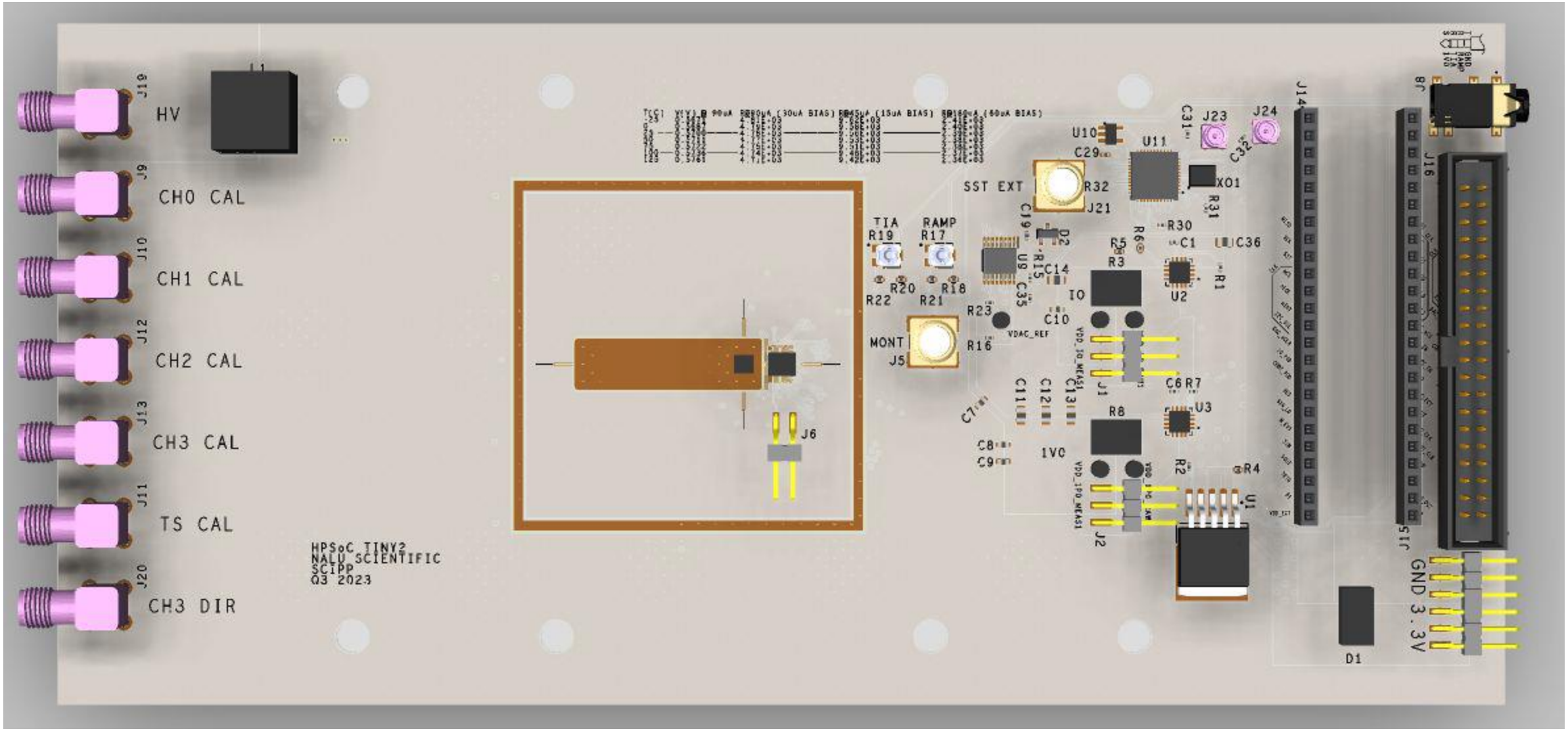
Trigger: 0.720 mA

Ramp: ~30 µA

Comparator: 256x1 µA = 0.256 mA

Total w/out clock and counter distribution: 3.25 mA

- Ca. 3.3 mW (1 V op)


HV
CH0 CAL
CH1 CAL
CH2 CAL
CH3 CAL
TS CAL
CH3 DIR
HPSoC TINY2
NALU SCIENTIFIC
SCIPP
Q3 2023
SST EXT
TIA
RAMP
MONT
GND 3.3V

Fabricated chip

Initial shorting of wirebond heels to chip seal (metal frame) required adjustments to bonding wire and parameters!