ALPHA ASIC Evaluation Board

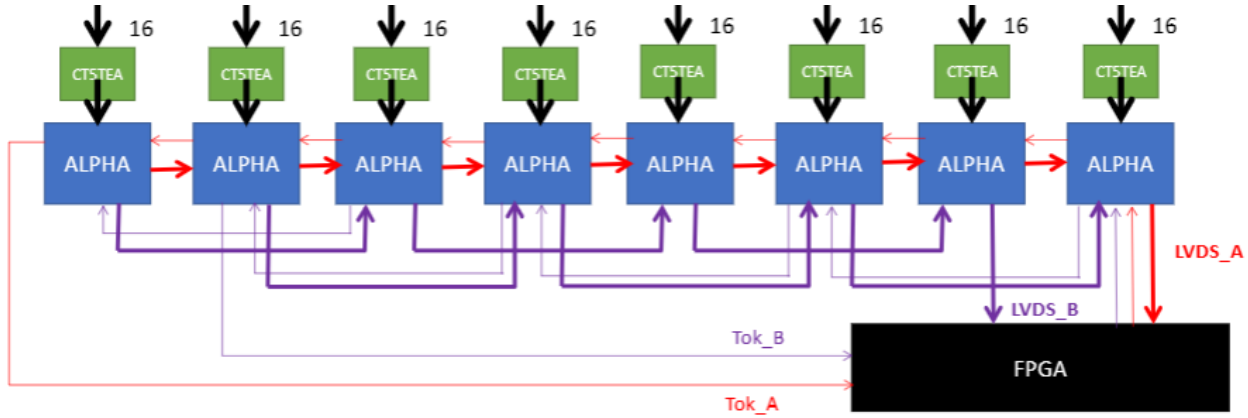
Makiko Kuwahara

PHYS475 Fall 2021

Professor: Dr. Gary Varner

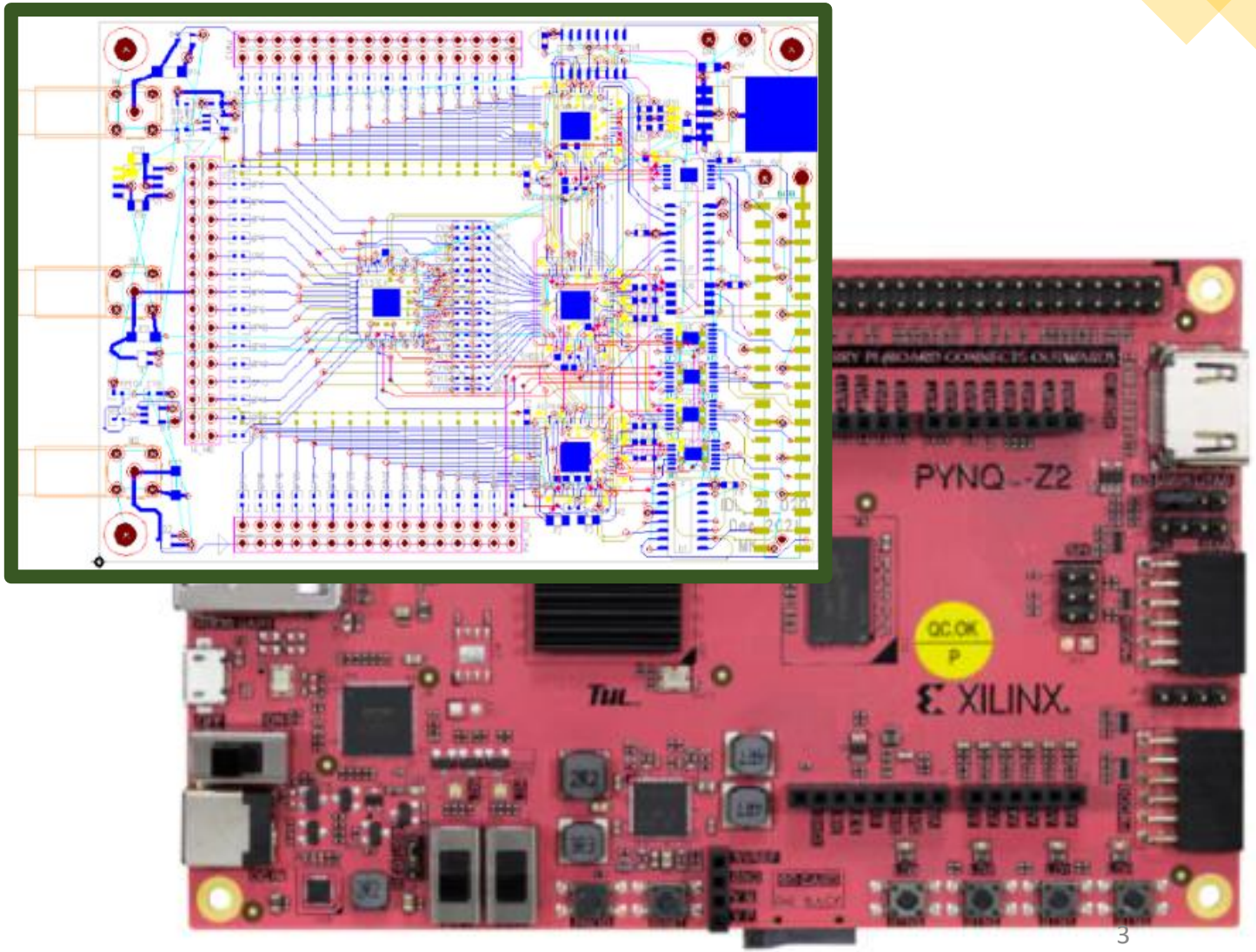
ALPHA ASIC

- Advanced Low Power Hybrid Acquisition [ALPHA] ASIC
- Project Title: The **Antarctic Demonstrator** for the Advanced Particle-astrophysics Telescope (APT)
- ALPHA_v1 ASIC designed in our IDLab and manufactured by TSMC
- Multiple ASICs are daisy chained with one FPGA to lower power consumption
- CT5TEA sends trigger to ALPHA for capturing samples of interest
- There are two paths for data and token so that the chain can detour defective ASIC

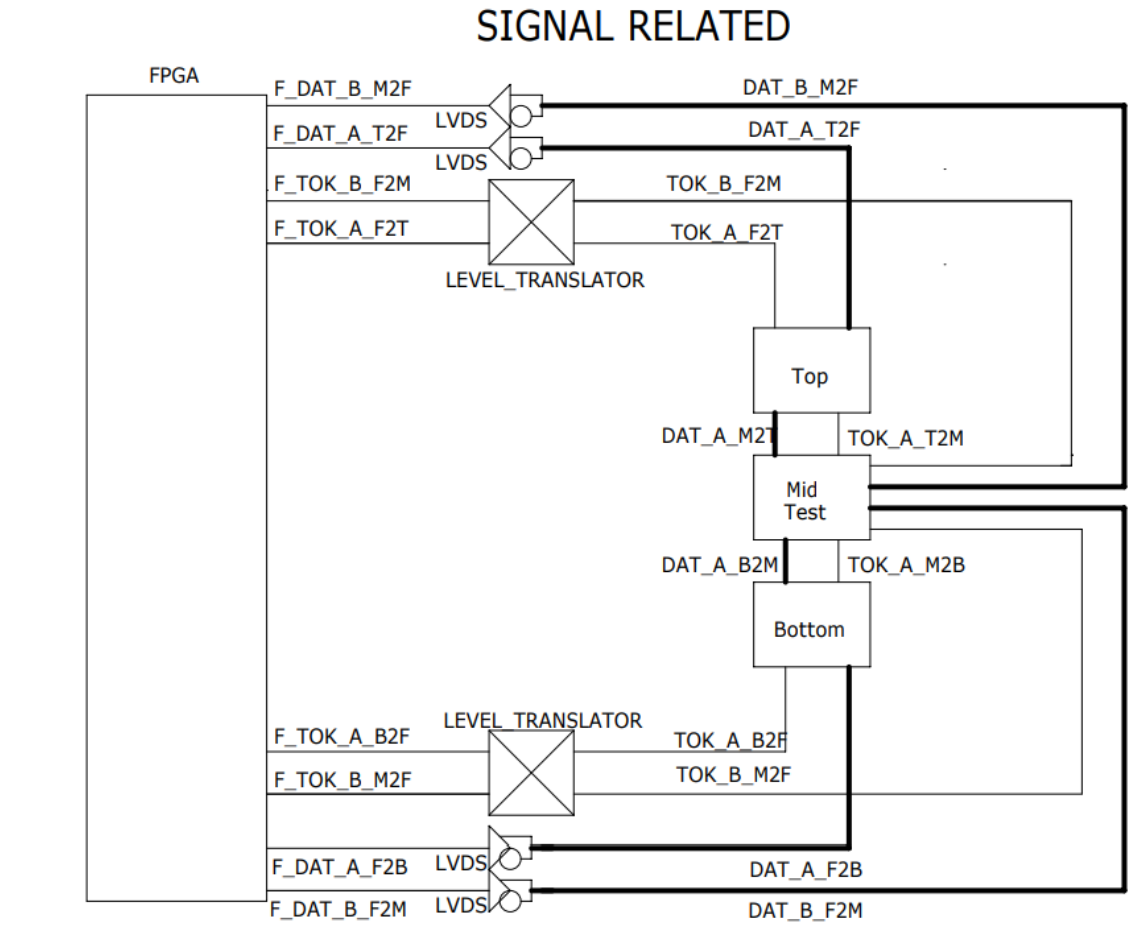


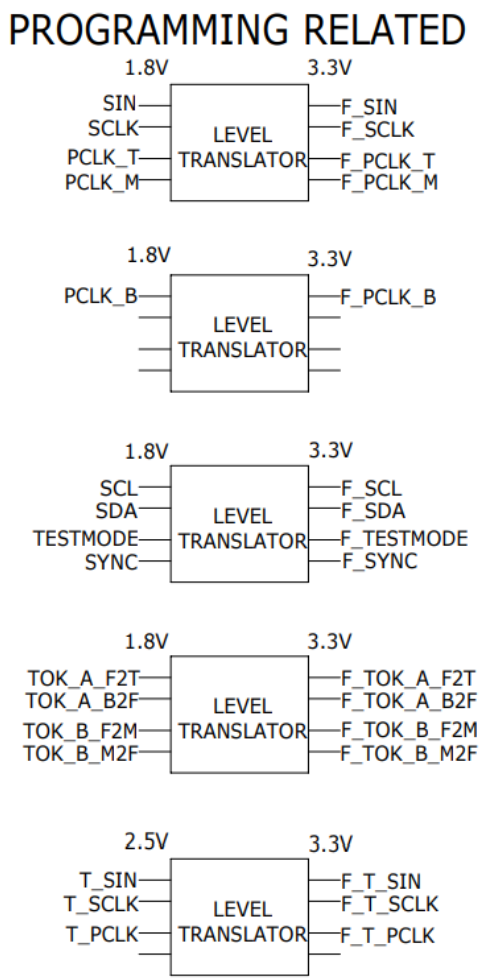
Evaluation Board Features

- Evaluation board PCB on PYNQ
- Test with one ALPHA to characterize chip by itself
- Test with 2 other ALPHAs (total 3) to test the communication
- 1 CT5TEA to emulate the performance
- Power 1.8V(ALPHA) 2.5V(CT5TEA) 3.3V(PYNQ)
- Schematic and Layout creation using Mentor PADS software
- PCB size 3 x 4 inches



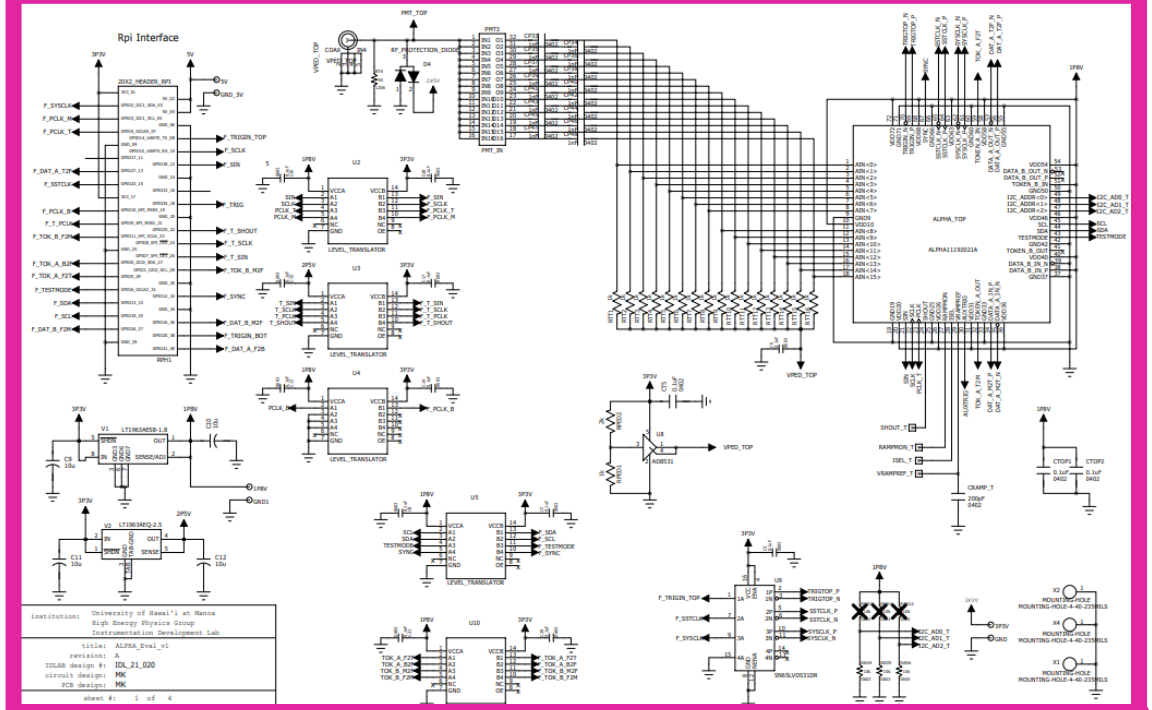
PADS Logic (Wiring Documentation)

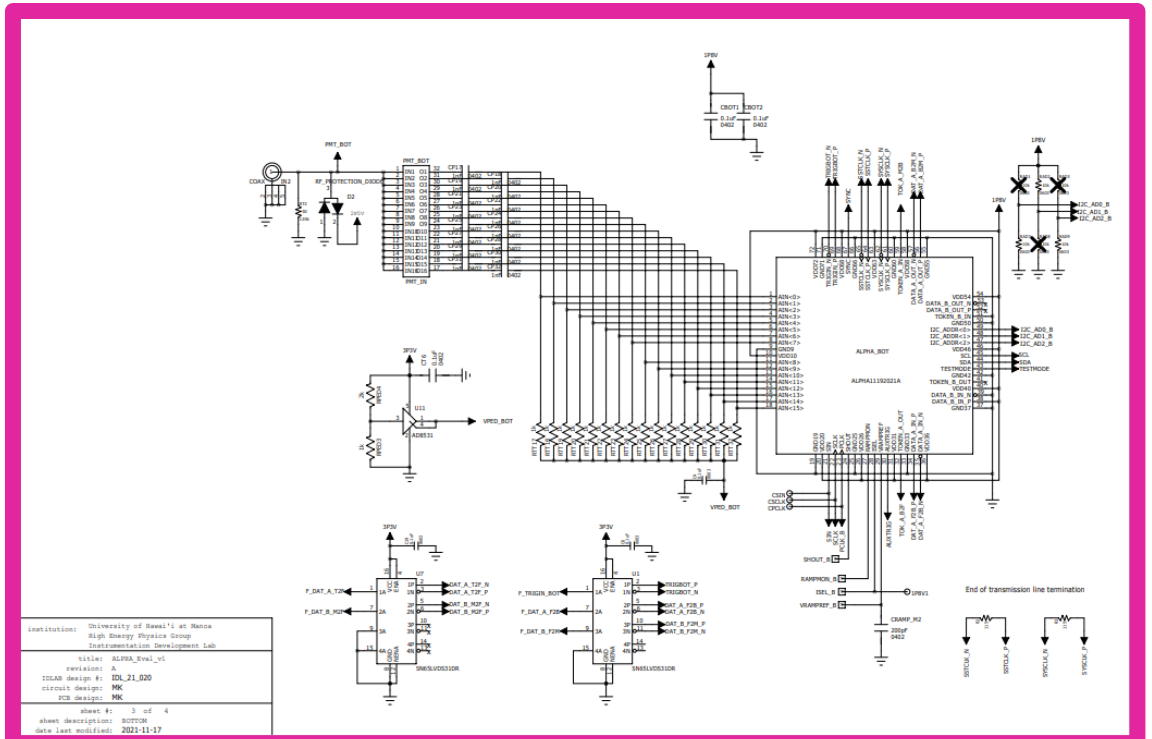


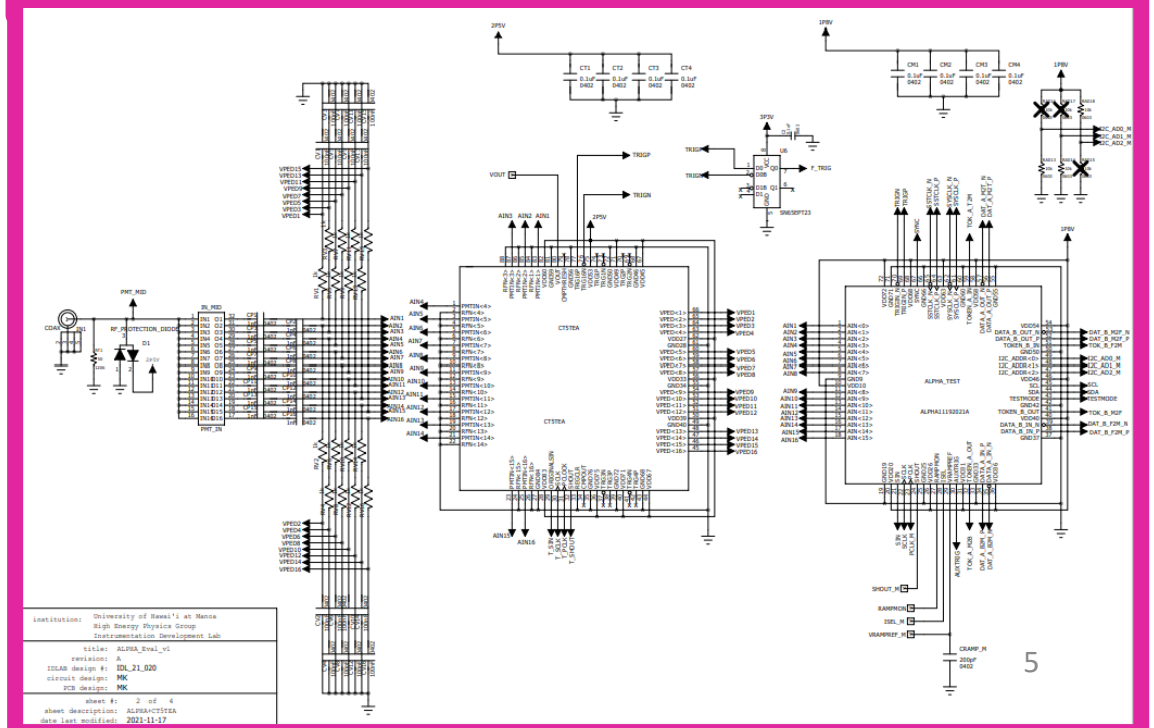


PADS Logic Schematic

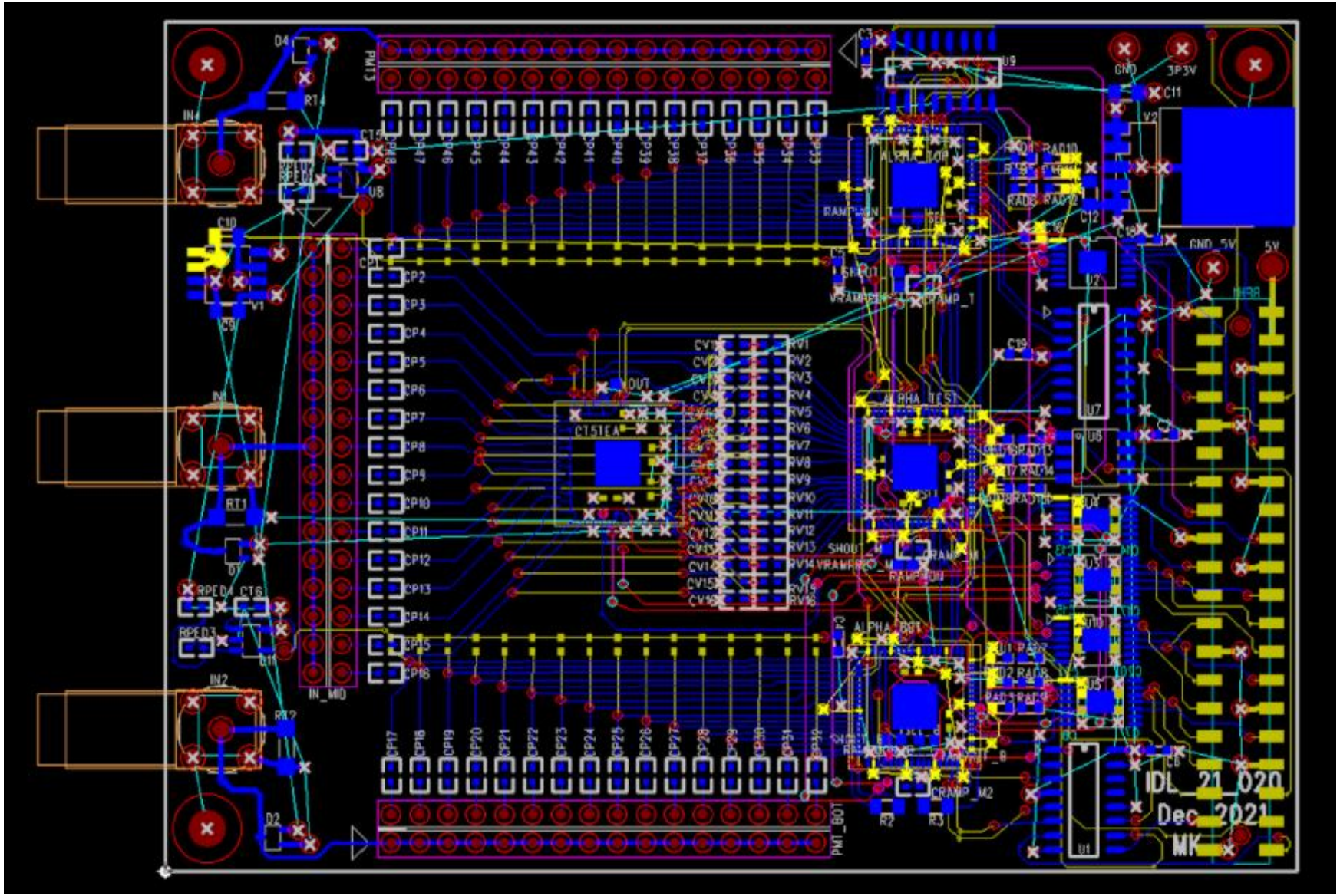
Blueprint of the parts and connections.







PADS Layout



Evaluation board production process flow diagram

Mentor PADS

Mentor Graphics pads personal automated design system

Symbol Creation **PADS Logic** → Decal Creation **PADS Layout** → Wiring Documentation **PADS Logic** → Schematic Creation **PADS Logic** → PCB Layout **PADS Layout** → Artwork Generation **PADS Layout**

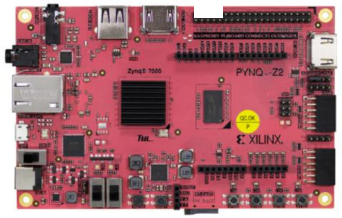
Future Work

PCB Design Submit for Manufacturing → Stencil Making for Assembling → Soldering Parts on PCB → Testing ALPHA_v1 → ALPHA_v2

ADVANCED CIRCUITS
Leading the PCB Industry in Quality & Innovation

Completed on Dec 08, 2021
Estimated delivery on Dec 20, 2021

rayjet Laser Engraver



PYNQ

Questions?