Report from LAL visit

S. Yamada (KEK)

Meeting at LAL

- Itoh-san and I visited LAL last week and have meetings with LAL people.
- Dec. 7th : meeting w/ LAL SERDI people
- Dec. 8th : François Le Diberder-san joined.

SERDI
Service d'Electronique, Recherche en Détecteurs et Instrumentation

Head: **Dominique Breton** (IPP1)
Deputy: Véronique Puill (IR1)

April 2017
42 persons

Secretary: Vanessa Bénard (TCN)

Driving comity:
Head of department
Head of groups

Instrumentation

F. Wicek (IR1)
Head

C. Cheikali (IE2)
R. Chiche (IR1)
P. Cornebise (AI)
M. Gaspard (IEHC)
J. Jéglot (IE2)
D. Jehanno (AI)
J. Girault (TCN)
S. Trochet # (TCE)
C. Sylvia (AI)

Systems

C. Beigbeder (IR1)
Head

T. Cacérès (IEHC)
D. Charlet (IR2)
B.Y Ky (ASI)
J. Maalmi (IR2)
E. Plaige (IE1)
S. Simion (IR1)
V. Truong Canh (Apprenti)

Research on Detectors

V. Puill (IR1)
Head

P. Barrillon (IR1)
L. Burmistrov (IR2)
S. Dubos (IR)
V. Chaumat (AI)
P. Halin (TCS)
P. Loaiza (IR2)
A. Natochii (Doctorant)

Microelectronics

P. Vallerand (IR1)
Head

M. Cohen Solal (IR2)
M. El Berni Δ (IE2)
O. Lemaire (IR2)

CAD/Fabrication

O. Duarte (IR1)
Head

CAD

P. Rusquart ◊ (AI)
C. De Andrade (AI)
J-Ch. Hernandez (TCN)
C. Mendy (TCN)
J-L Socha (TCS)

Fabrication

P. Favre (TCE)
F. Campos (TCN)
B. Debennerot (TCS)
M. Fernandez (TCS)

 # support machine CMS
Responsable plateforme Captinnov

Δ support outils VLSI

◊ support outils CAO PCB

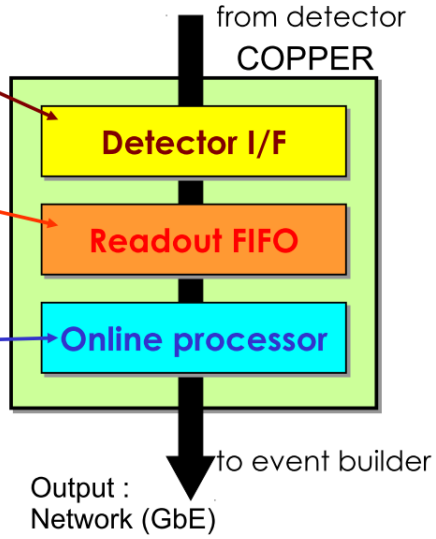
Itoh-san explained the motivation and timeline etc..

What is COPPER?

COPPER is a unified "pipeline read-out platform" module.

(Common Pipelined Platform for Electronics Readout)

- Detector I/F
  - Signal digitization.
    -> Belle2link receiver (Belle II DAQ)
  - L1 pipeline.
- Readout FIFO
  - Event buffers for asynchronous readout.
- Online processor
  - Data size reduction.
  - Data link management to event builder.
  - Linux operated



Why is the maintenance of COPPER system difficult?

1. The design of COPPER is based on the old PC technology, such as PCI-bus, which is already obsolete.

2. The production of many components used in COPPER is already discontinued.
   * Network controller chip
   * Chipset used in the CPU card (PrPMC)
   * Various control chips used in COPPER (FIFO.....)
   .....

3. The production company of COPPER says they cannot support COPPERs any more.
   - *We still have a number of backup COPPER modules, but it is limited (especially COPPER III, majority of COPPERs in our DAQ).*

4. Cannot keep up with the evolution of Belle II software.
   * COPPER CPU has the 32bit architecture, but recent Belle II software, which is heavily utilized in COPPER CPU, is now all 64bit based while abandoning the support for 32bit.....

Further concern:

- There could be a chance that the accelerator luminosity goes up beyond the design value.
  <- Remember the fact that KEKB achieved twice luminosity of the design value!

- In this case, the processing power of COPPER becomes the bottleneck of DAQ, which was designed for the luminosity up to $L=8x10^{35}$
  * PCI bus speed cannot manage the expected data flow.
  * Lack of processing power of CPU card.

Replacement of old COPPERs is required.

Readout Upgrade : Short Overview

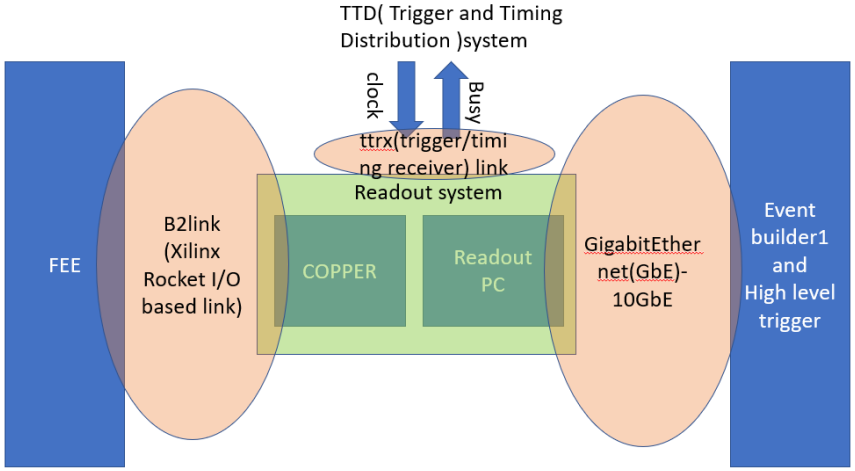
- COPPERs are already obsolete and we agreed to start R&D on the new readout system last year.

- In the DAQ meeting in March, it was decided to keep the current implementation schedule unchanged although Belle II commissioning was deferred:
  * Start prototyping in late JFY2018 and two years for R&D.
  * Start mass-production in JFY2020 and complete in 3 years.
  * Start partial replacement of COPPERs from JFY2021 and complete replacement by the end of JFY2023.

- To keep up with the schedule, we need to fix the prototype design by Oct.2018.

I explained the boundary condition and upgrade ideas at the October workshop

Boundary condition for new readout



Basic framework of belle2link (Xilinx rocket-IO based serial link) should be the same. Otherwise FEE's FW/HW update might be needed.

Upgrade like GbE -> 10GbE will be possible, if we upgrade switches.

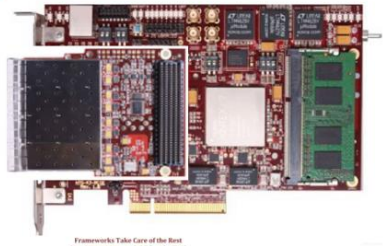
COTS

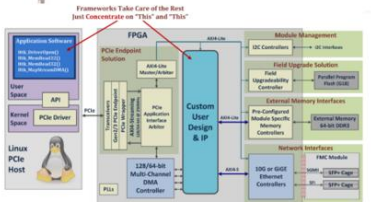
(L.Wood)

COTS Proposal #2: FPGA "Network Card"

Pacific Northwest NATIONAL LABORATORY

- **4xHSLB + COPPER replaced by single COTS FPGA + FMC carrier**
  - Ex: HTG-K700 + 4xSFP+ FMC: $3900-4200
  - Kintex-7 **XC7K410T** (-2 or -3)
  - x8 PCIe Gen2 (Gen3 req's IP)
  - Up to 8GB DDR3
  - Quad SFP+ FMC
- **Available FW framework** with interfaces for 1/10GbE, DDR3, flash, PCIe DMA and remote programming, Linux device drivers, etc.
- **Improvements:**
  - Zynq and Ultrascale boards available
  - Higher density of network ports on FMC (2 x QFP, 10 x SFP, etc.)



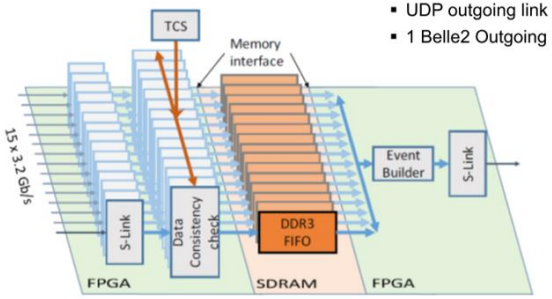


DHCmx

(I. Koronov)

DHQmx

- 60 Belle2 Input links
- MX 60 :1
- IPBUS, B2TT
- UDP outgoing link for Local Run
- 1 Belle2 Outgoing Link



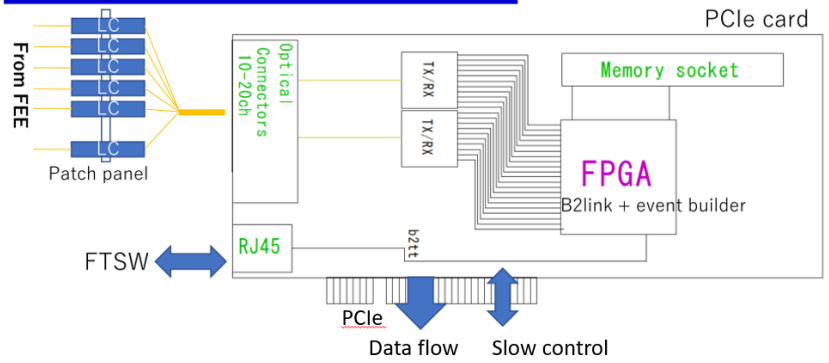
Data Consistency Check:

- Transmission errors detected by S-Link
- Truncation, i.e. mismatch between real and declared data block size
- Inconsistency of event label
- Missing data -> timeout

Error detected

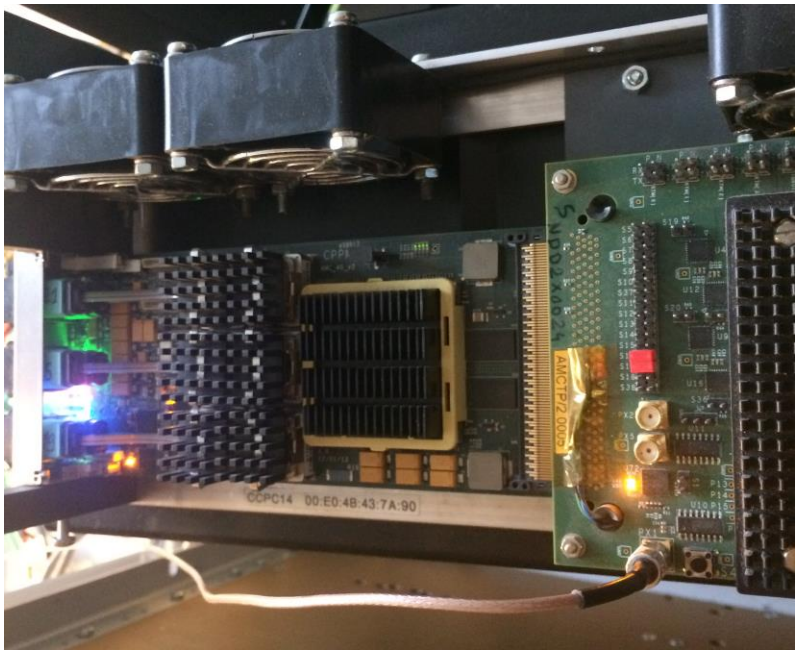
- Discarding/throttling of wrong data
- Adding of specific header
- Setting error flag in local register

Schematic view of a new readout board

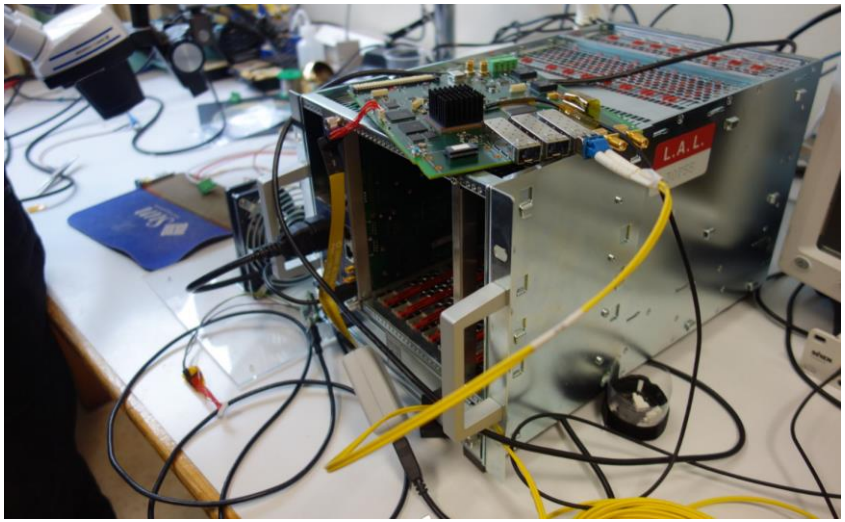


- Compared with COTS, new board development can make a simple solution which fits the Belle II experiment.
- Technology has advanced from COPPER board era
  - High density of input channels -> compact system
- Current preference is PCIe output. If possible, 10GbE output could make a simpler system without intermediate readout PCs.

Workshops at LAL



Tell40 board for LHC experiments was being tested.



AMC Carrier board and FMC as an input card ,which are being developed by Daniel-san.

Summary of the meeting (from my side)

- Enough expertise and resources for the upgrade
- SERDI people looked interested in the Belle II DAQ upgrade. (The internal discussion will be needed for group's decision.)
- They seem to be considering basically the same kind of techniques for a new readout board as we discussed at October Workshop.
- François Le Diberder-san was also interested in the cooperation in this upgrade for Belle II.
- Itoh-san proposed to apply for *France Japan Particle Physics Laboratory fund* (basically travel budget) for LAL-KEK cooperation.
- Cost and timeline of the upgrade were asked but they are not still easy to answer.
  - As for a KEK idea, I'm going to take an cost estimation from a company.

My thoughts after the LAL visit.

- In my feeling when we had discussion w/ LAL people, the technology for the upgrade will be basically similar as ours(COTS, TUM and KEK), due to the boundary condition for the Belle II readout system.
- So, first, I hope that we can build consensus about what kind of technology should be used.
  - I think that it will take longer time if we start discussion to decide between Group A' board, B's board and C which are not so much different…
- Then, who will/can be responsible for the hardware development/production will become another issue to be discussed. (It will depend on resources, budget, etc… I'm not sure that is inside/outside of the scope of the committee.)