UNIVERSITY of HAWAI'I®
MĀNOA

Muon Tracker Prototype of the Borehole Muon Detector

PHYS 475 - Final Presentation

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Overview / Background

- What
  - Design second version of muon detector using Multi-Pixel Photon Counters (MPPC)
- Why
  - Tomographic reconstruction allows non invasive 3D imaging
  - Muons have greater penetration, allowing deeper scanning than x-rays
  - 1st version was too large for use in boreholes

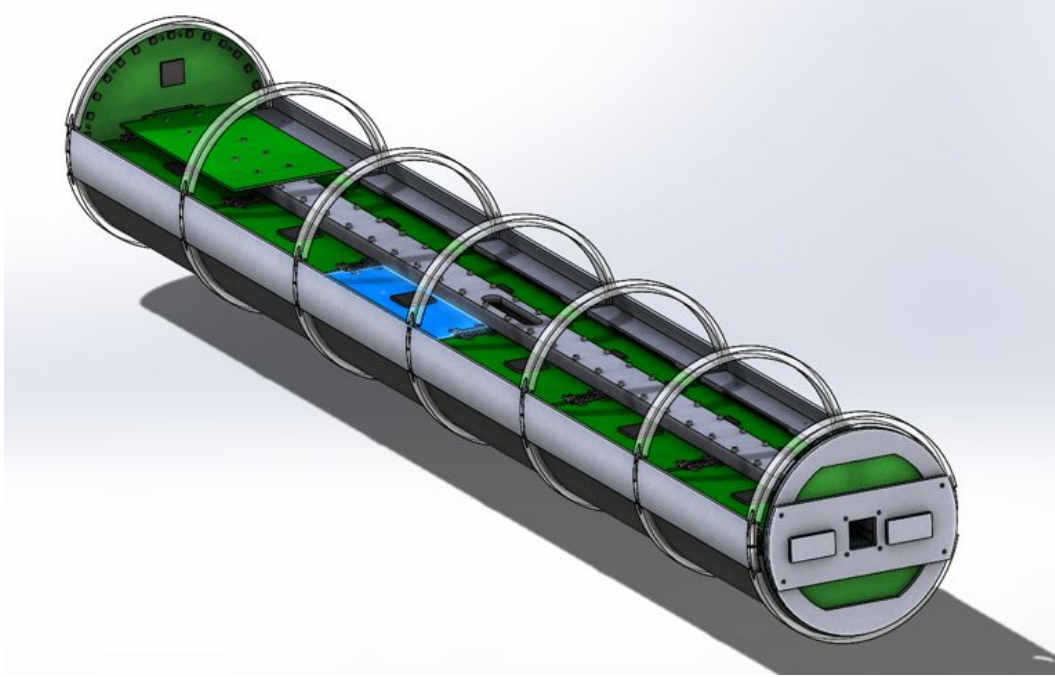


Figure 1. 3D model of Full BMD Detector.

Overview / Background (continued)

- How
  - Remove long CAT 6 cables to reduce signal noise and congestion
  - Redesign MPPC boards to include additional FPGA for localized ASIC readout and initial data reduction
  - Modify scintillators from square rods to round hollow cylinders composed of wavelength shifting fibers

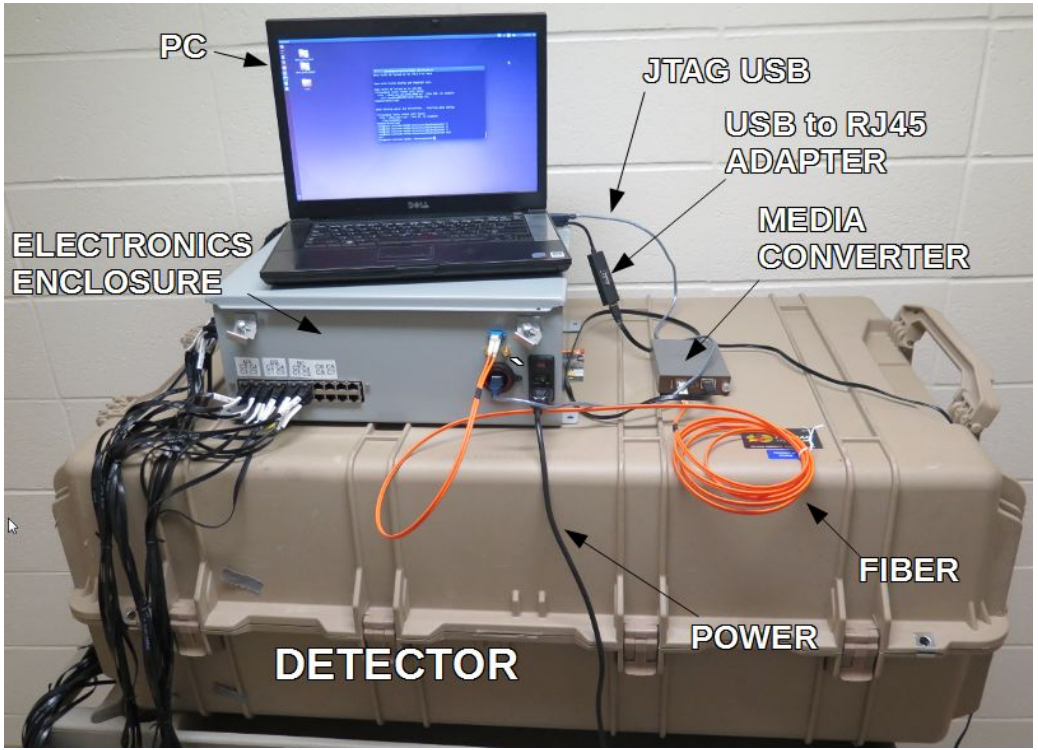


Figure 2. Original BMD setup.

Project Objectives

1. Design, fabricate, populate, and test the BMD daughter cards and interconnection board
2. Design, develop, integrate, and test firmware for subcomponents on daughter card
   a. DAC
   b. Temperature Sensor
   c. SRAM
3. BMD control/configuration firmware
4. Data readout

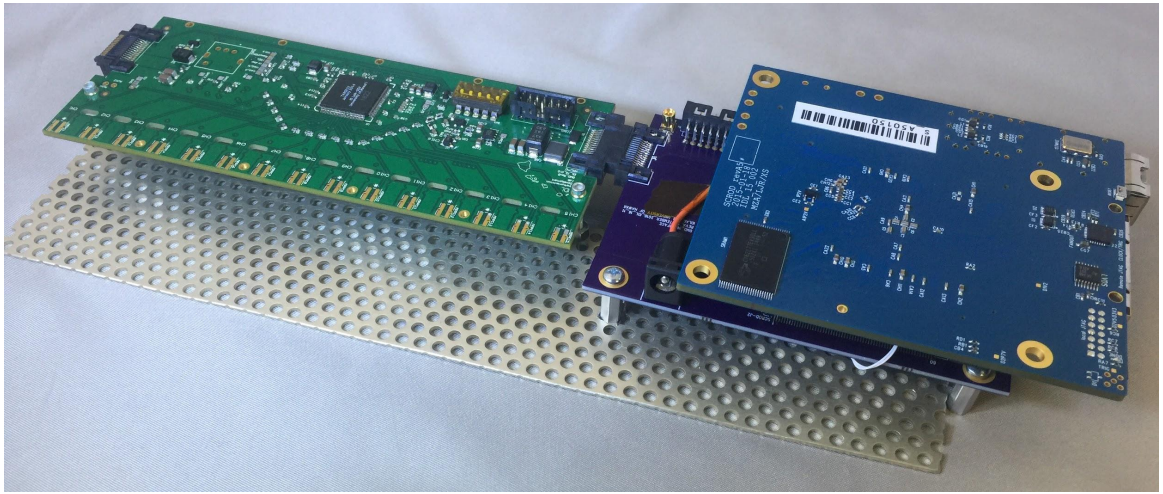


Figure 3. Electronics of the BMD detector.

Specifications

- Dimensions 1m x 15cm cylinder
- Current draw ≈ 10A
- Final BMD system will include
  - 15 channels/daughter card
  - 18 daughter center cards
  - 2 end cap cards
  - 1 power board
  - 1 SCROD
  - Thermo-electric coolers (TEC) along length of system

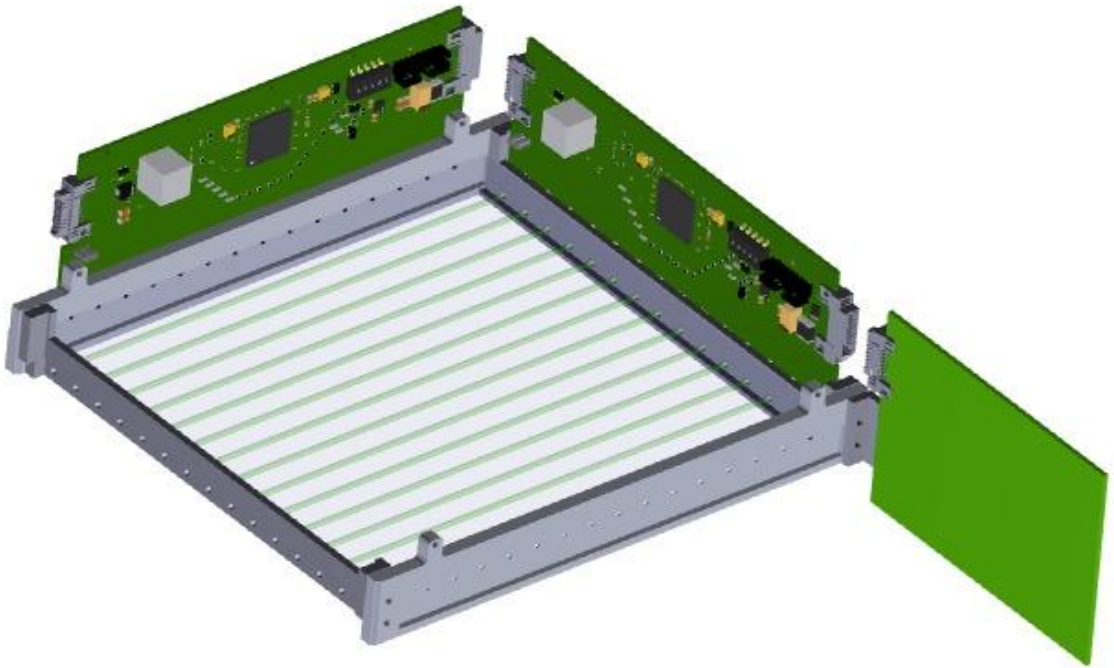
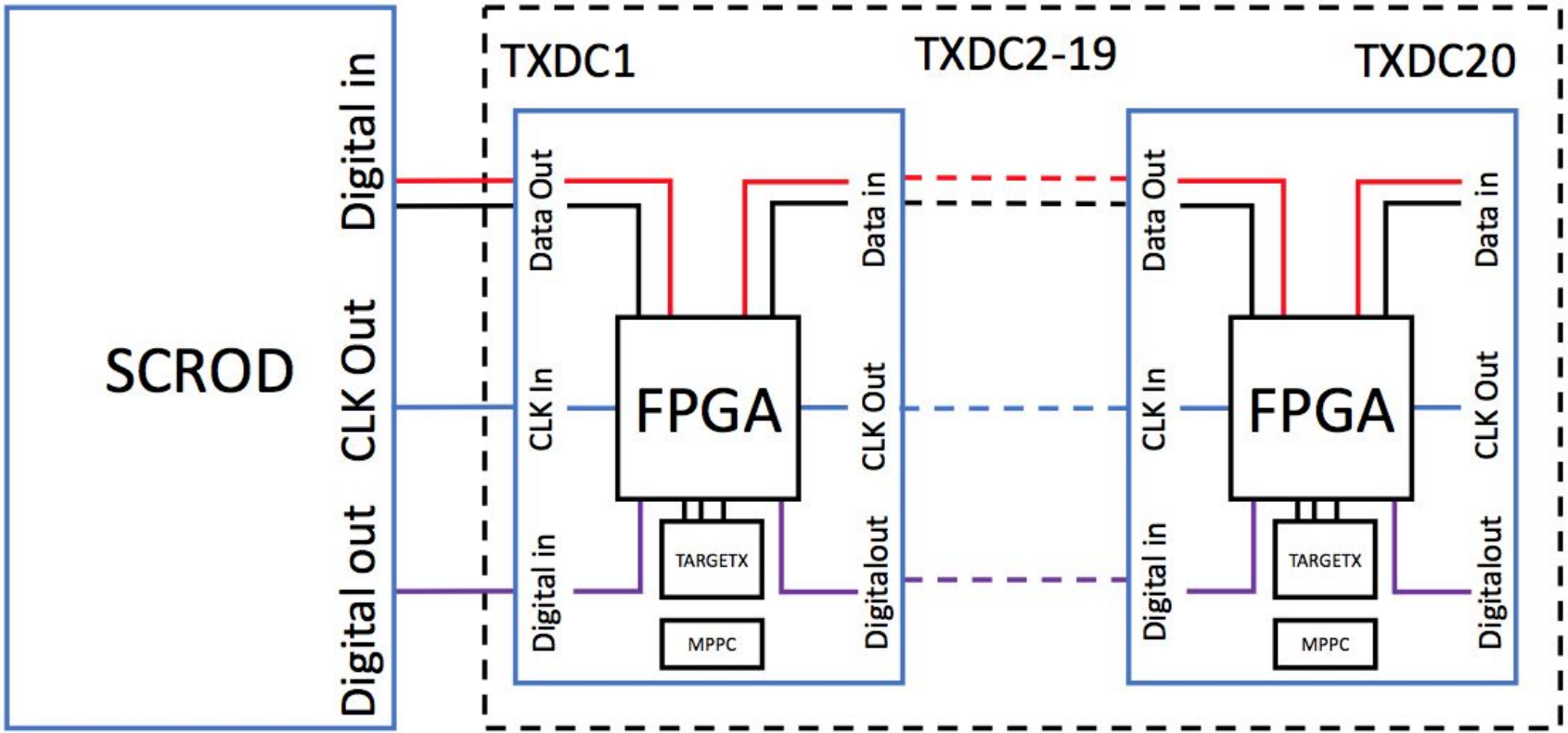
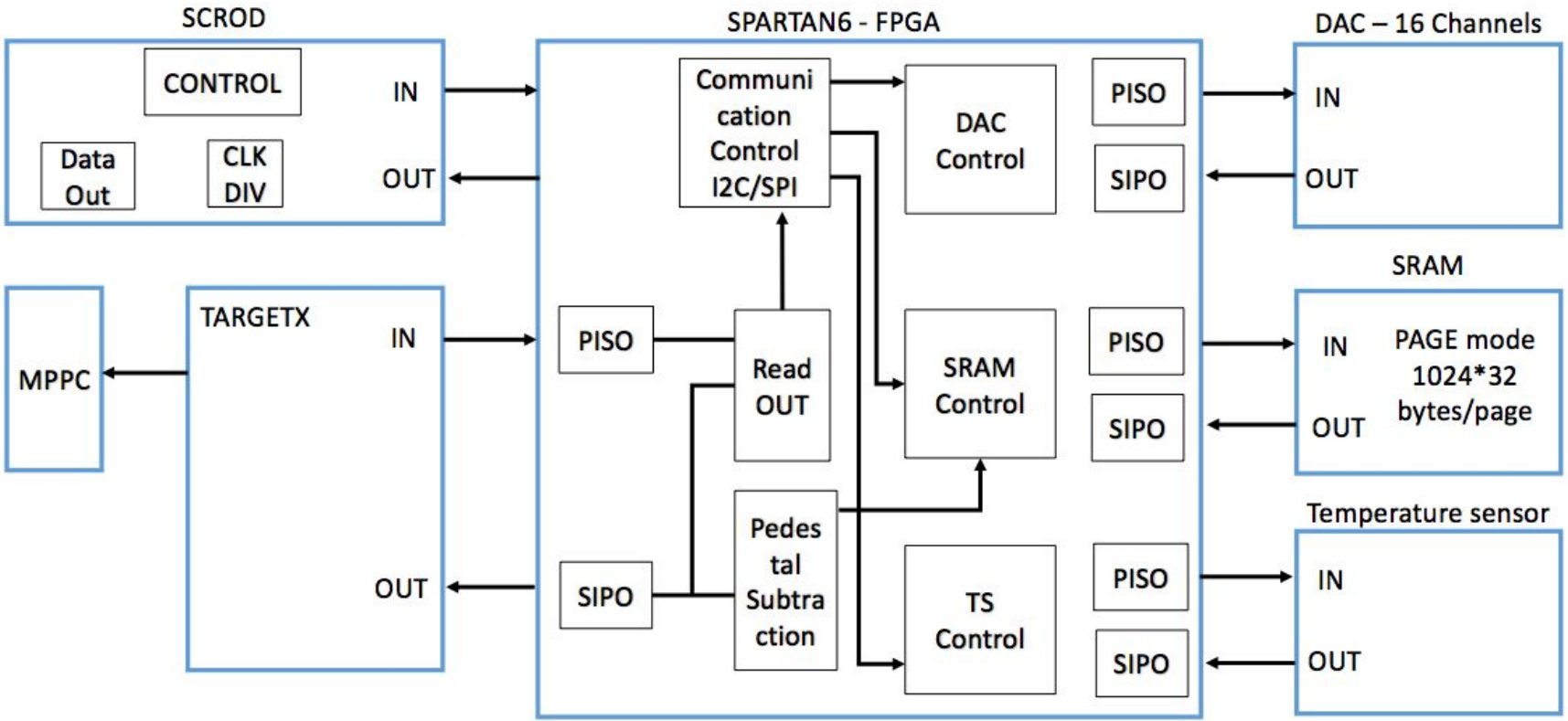


Figure 4. Testing Jig.

Block Diagram (TOP Level)



Block Diagram (Firmware)



Overview of Key Components (SCROD)

- The SCROD is used as system master
  - Controls daughter card readouts
  - Intermediate data processing
  - Communications via Ethernet to PCs for post data processing
  - Monitor system temperature and adjust thermo-electric coolers

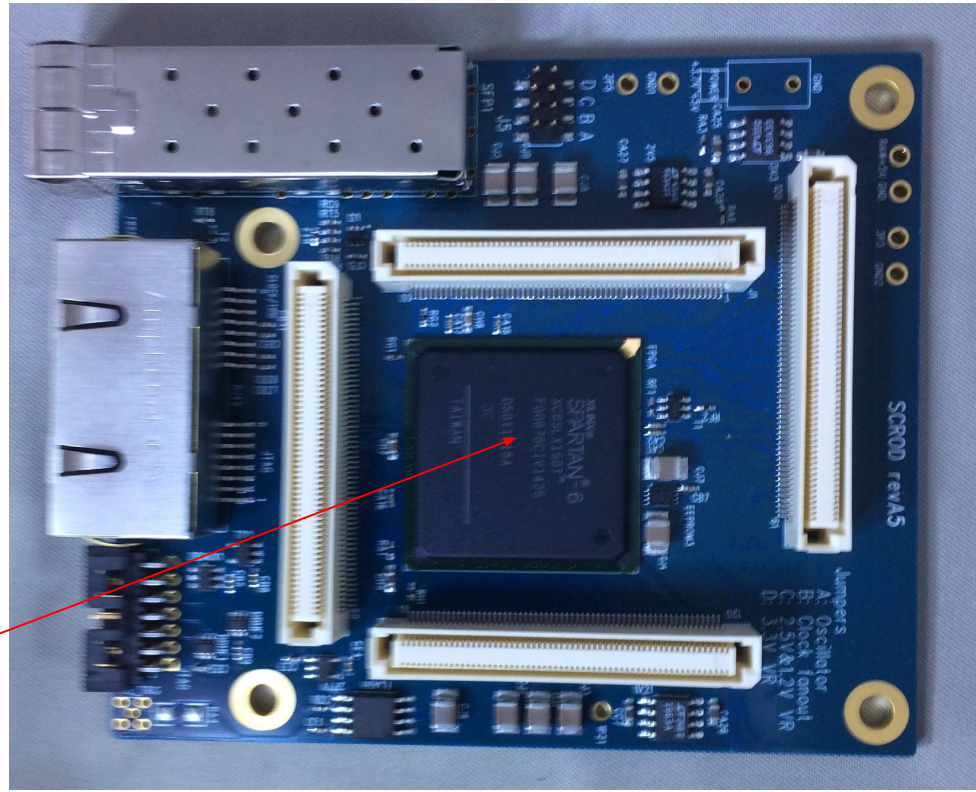


Figure 5. SCROD.

Overview of Key Components (Daughter Card)

- Daughter Cards uses TargetX to sample and digitize MPPC events and does initial data processing
  - 15 MPPC channels
  - Spartan 6 FPGA
  - TargetX

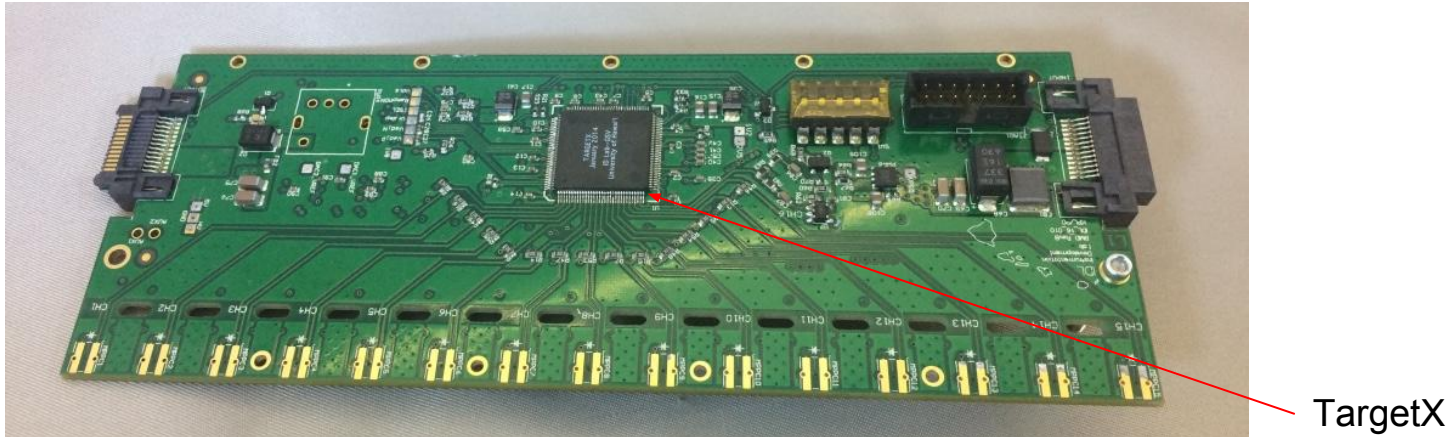


Figure 6. Daughter Card.

Overview of Key Components (Interface Board)

- The interface board connects the SCROD with the daughter cards for initial bench top testing.

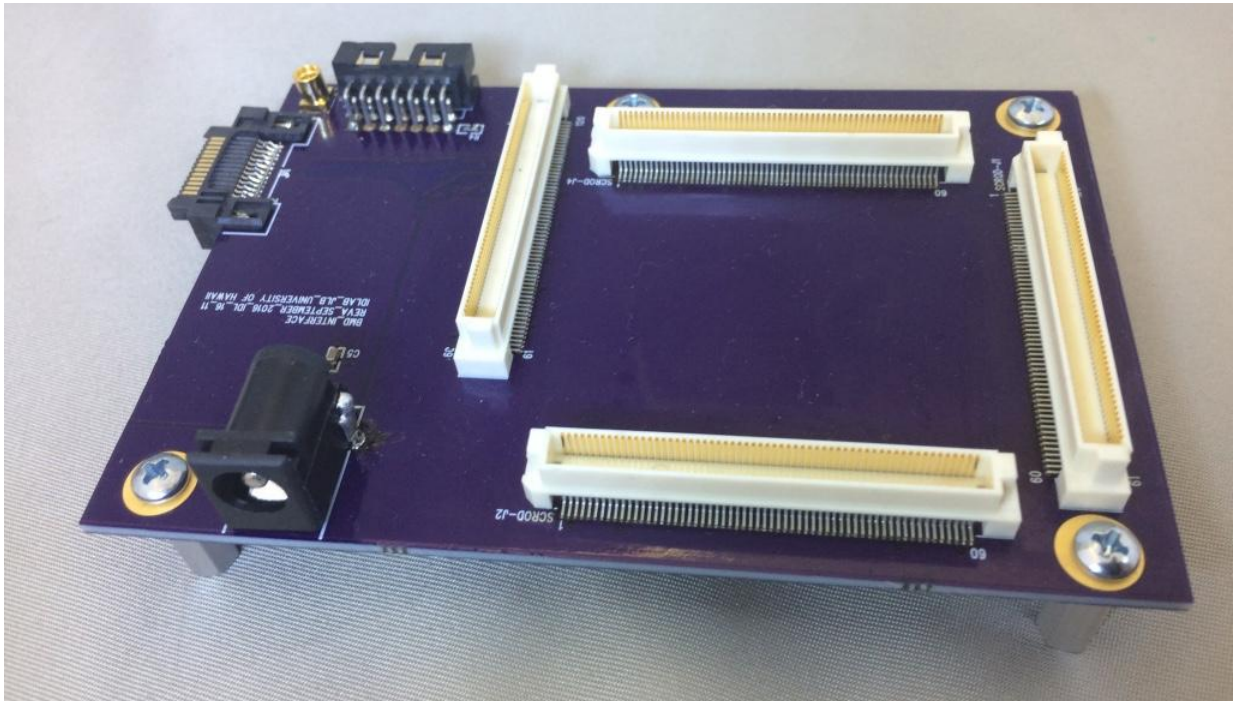


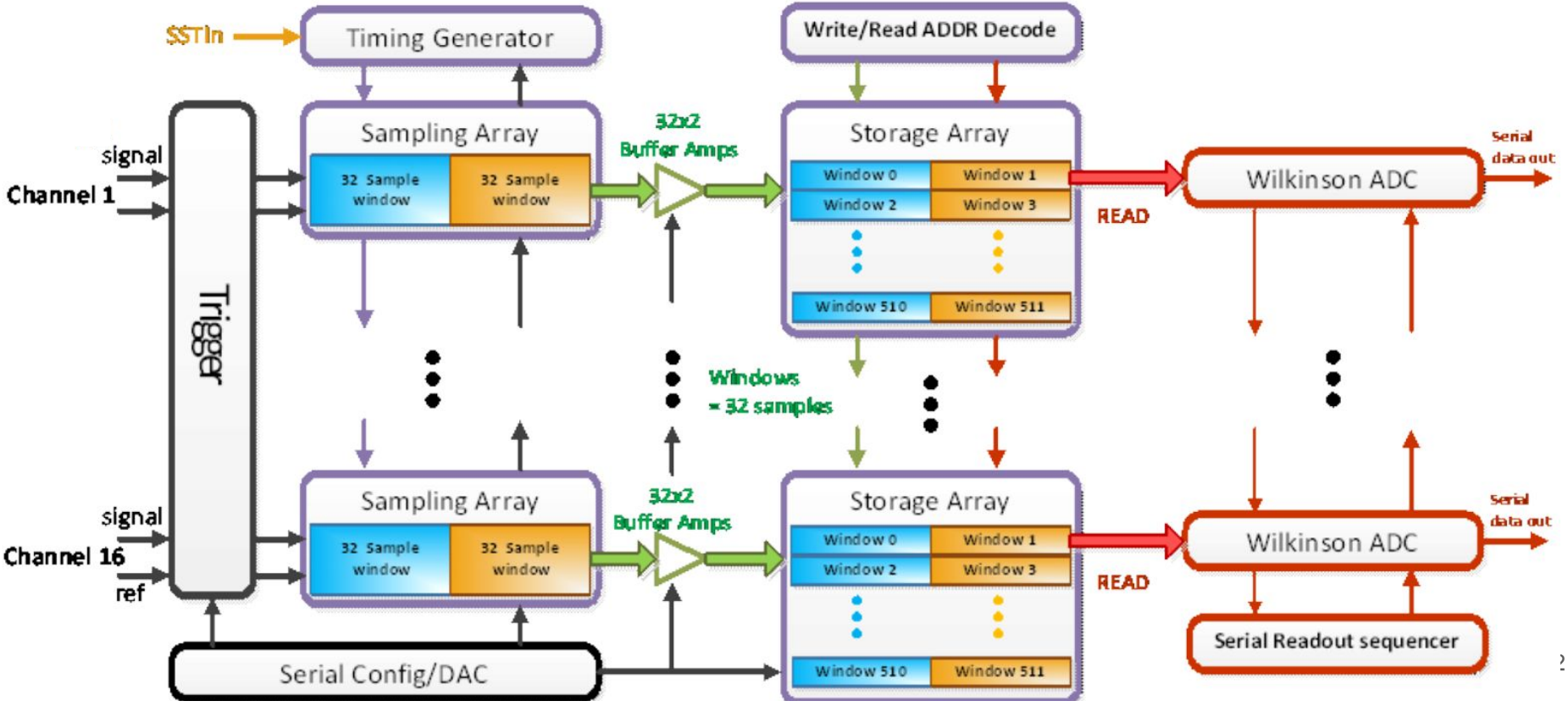
Figure 8. Interface Board.

TargetX

- Sampling rate of 1 GSa/s
- 16 channels with 16,384 storage samples per channel
- Single sample resolution of 9-10 bits
- Random access to individual samples
- Fast conversion < 5 μs / 512 samples
- Low power < 10 mW / channel

Figure 7. TARGETX ASIC.

Detailed Schematics (TargetX)



Detailed Schematics (MPPC)

Hamamatsu S12572-050/P MPPCs, along with the scintillators, are used for capturing and tracing the muons

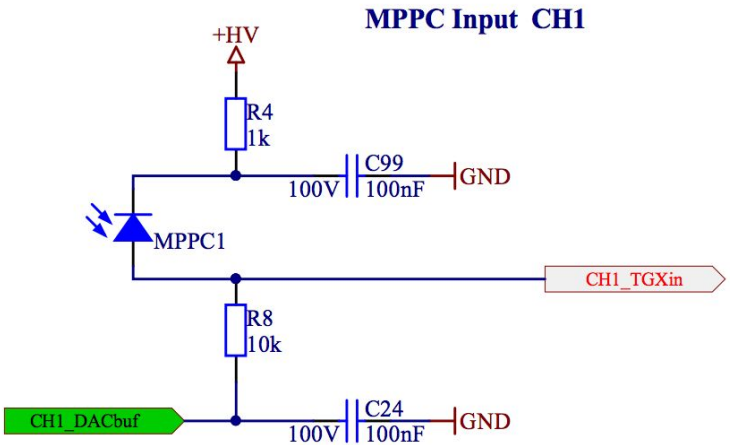


Figure 10. Schematic of the MPPC.

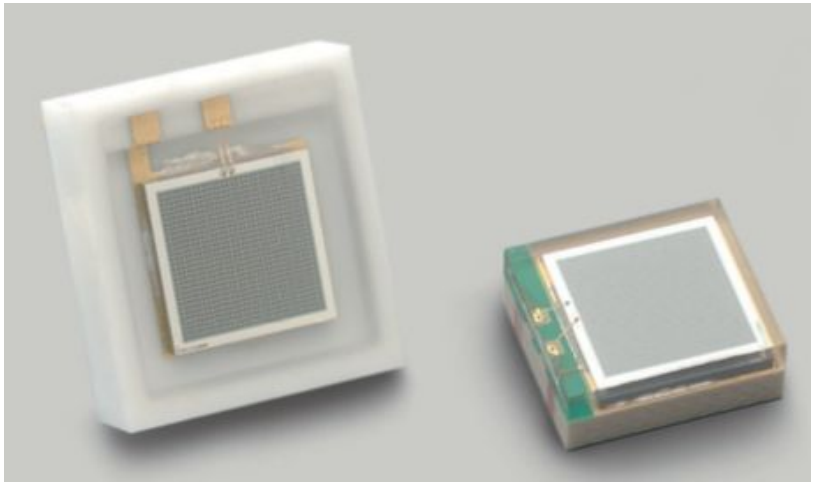
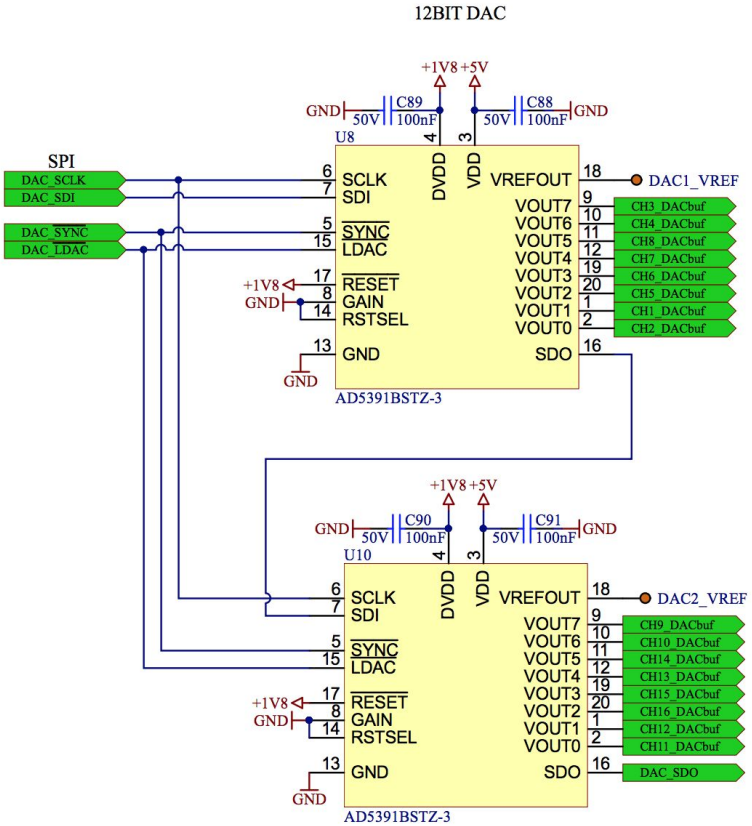


Figure 9. Hamamatsu MPPC.

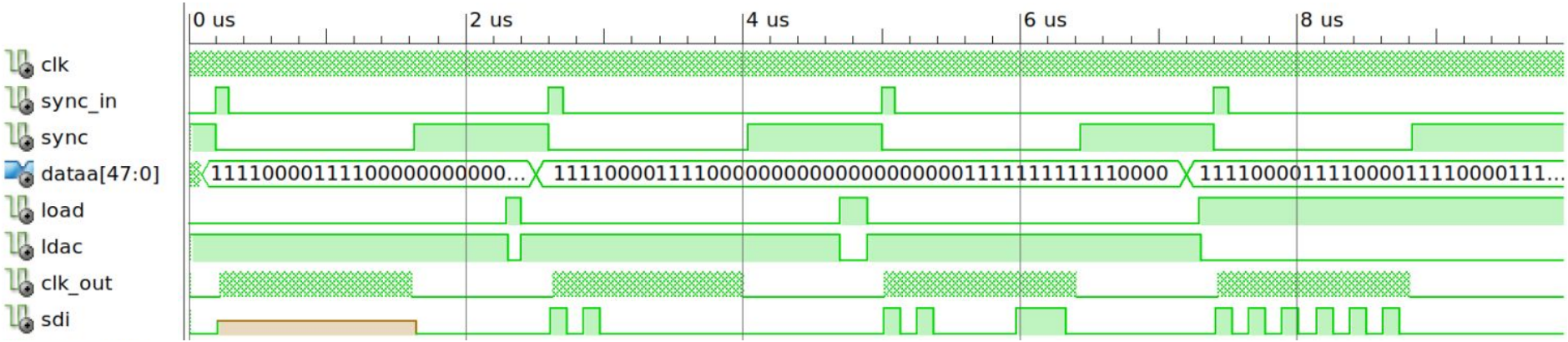
- The MPPC is Reverse biased with high voltage (~70 V)
- As the photon hits the MPPC, an avalanche effect generates an output pulse
- The DAC is used to control the dynamic range of the TargetX readout, ie. biasing the signal from the MPPC

Detailed Schematics (DAC)

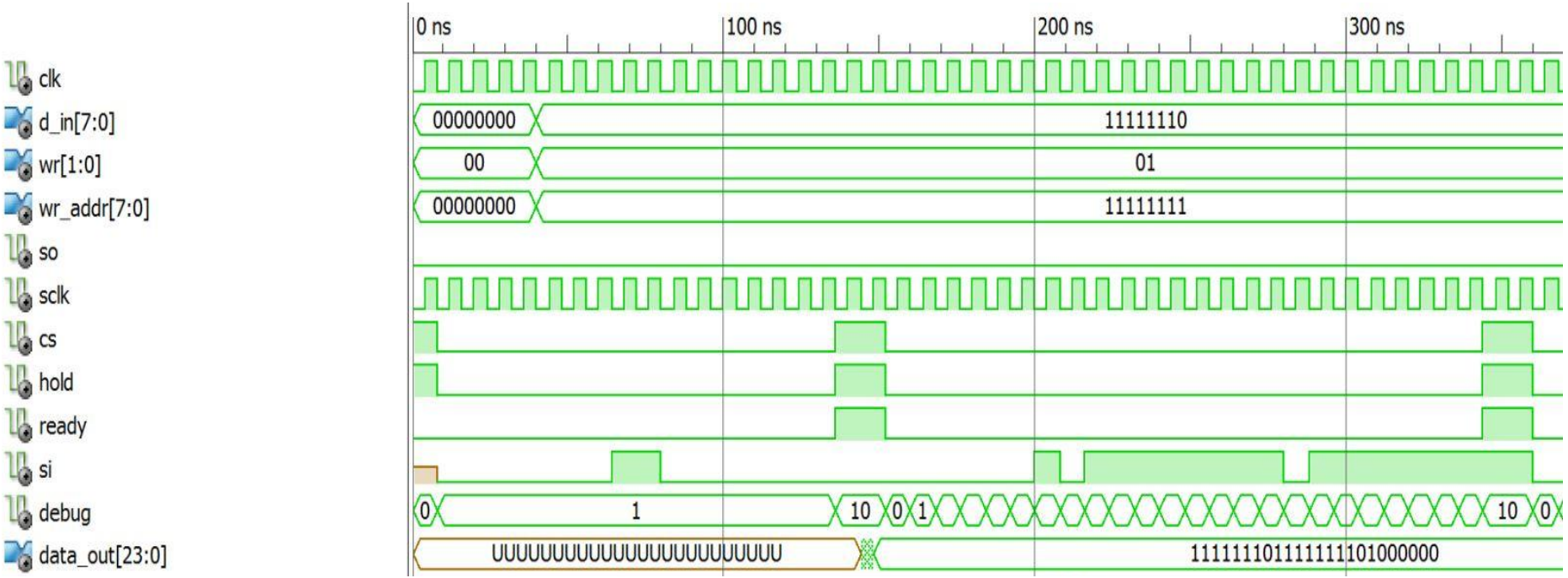


- The DAC is used for biasing the signal from the MPPC
  - Increase the dynamic range of the TARGETX readout
- One daughter card has two daisy chained DAC's to control 16 channels with 12-bit resolution
- Channels 1-15 controls the biasing of the MPPC's
- Channel 16 is used for controlling the high voltage

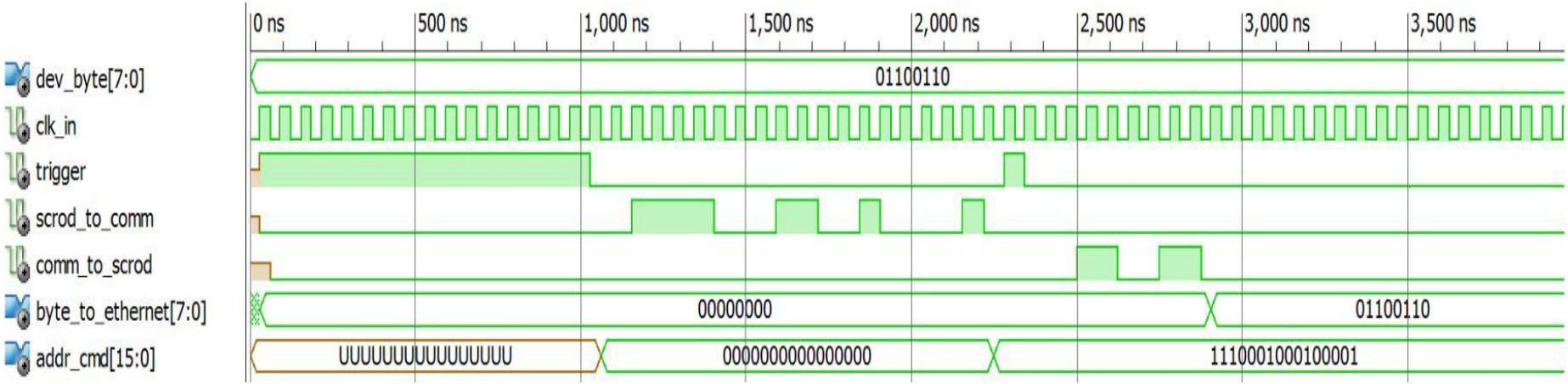
DAC - Firmware Simulation Results



SRAM - Firmware Simulation Results



Communications - Firmware Simulation Results



Elements Completed

- The circuit boards are done
- The firmware for all subcomponents are done and ready for integration

Onward

- SCROD/STRAP signal processing firmware
- Configuration and data taking software
- GUI display/running software
- Make a testing jig for the completed system

Questions?

(please say no)

(please clap)

Back Up Slides

Current Issues / Roadblocks

- Firmware and frontend for control, processing, and communications cannot be completed until existing SCROD/STRAP code is obtained for review.
- Full system cannot be tested until the mechanical components are complete.

Detailed Schematics (FLASH memory and SRAM)

Flash memory: used to store FPGA bit file for auto imaging on boot up

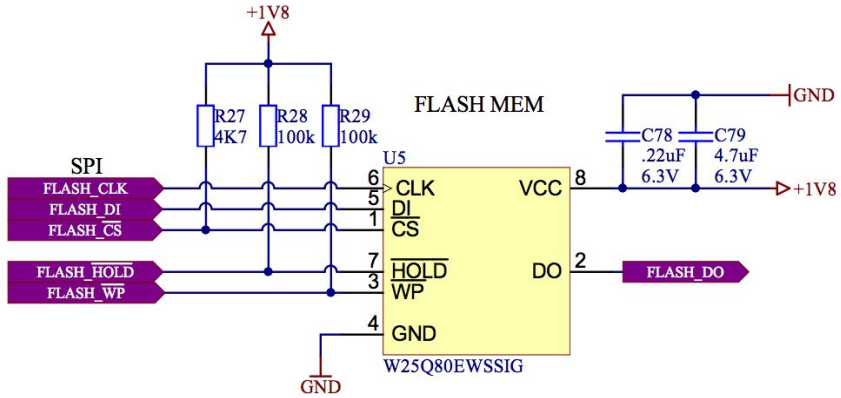


Figure 2. Schematic of the Flash Memory

SRAM: Used to store pedestal calculation results and other calculated values

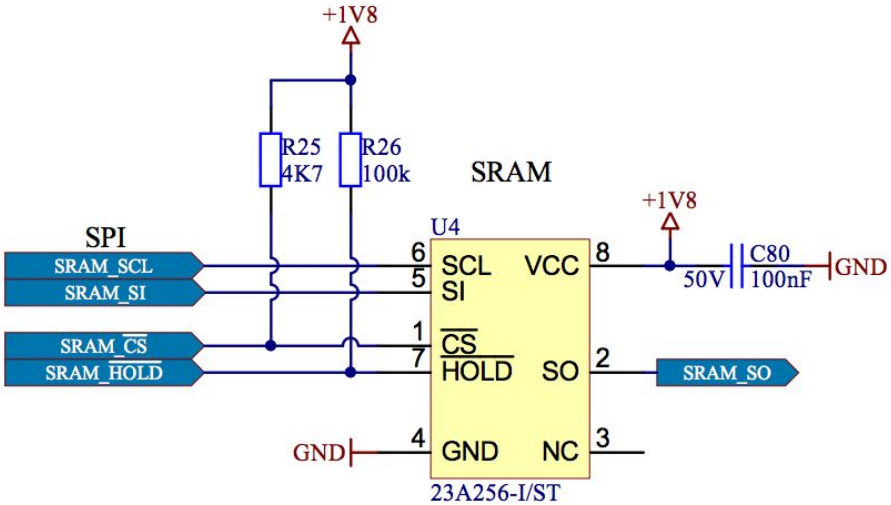
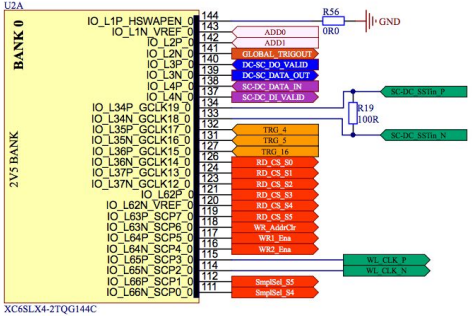
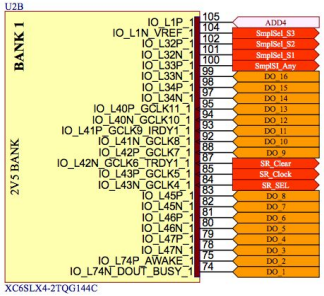


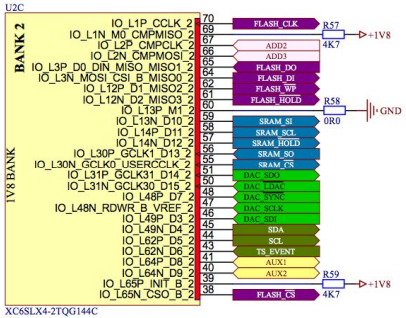
Figure 2. Schematic of the SRAM

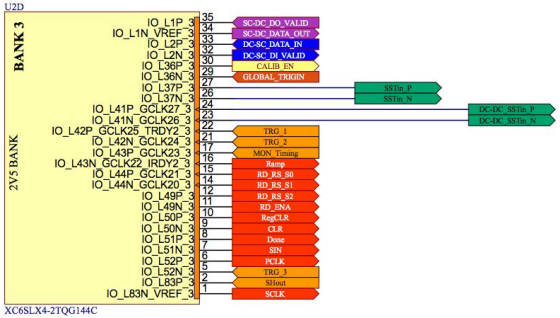
Detailed Schematics (FPGA)



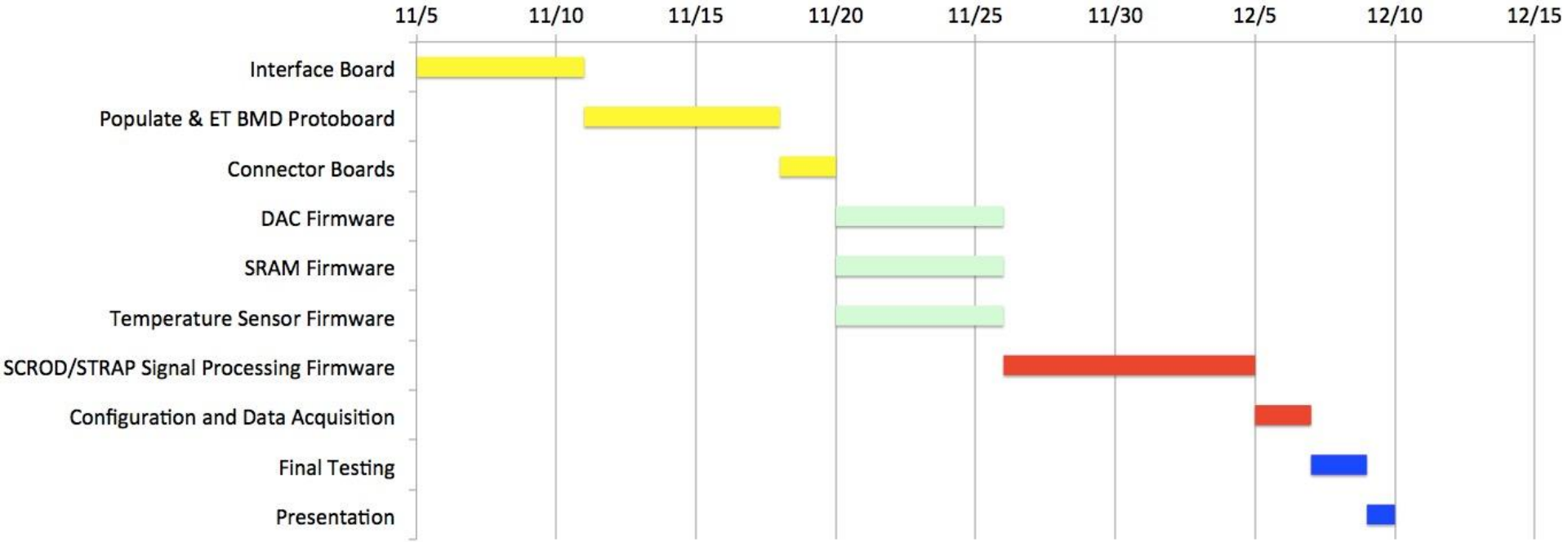


FPGA setup notes:
-FPGA set to master mode (pin 60 to GND 69 set to VCCO3)
-FPGA set serially for JTAG programing
-FPGA set to load image from flash memory





GANTT chart


11/5
11/10
11/15
11/20
11/25
11/30
12/5
12/10
12/15
Interface Board
Populate & ET BMD Protoboard
Connector Boards
DAC Firmware
SRAM Firmware
Temperature Sensor Firmware
SCROD/STRAP Signal Processing Firmware
Configuration and Data Acquisition
Final Testing
Presentation

Overview of Key Components (continued)

- Interface board
  - The purpose of the interface board is to connect SCROD with the daughter cards

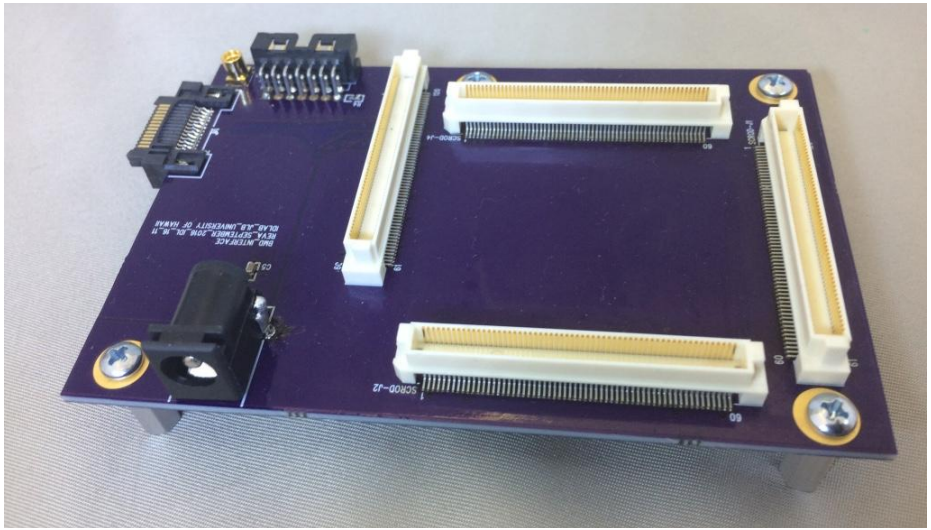


Figure 2. Interface Board

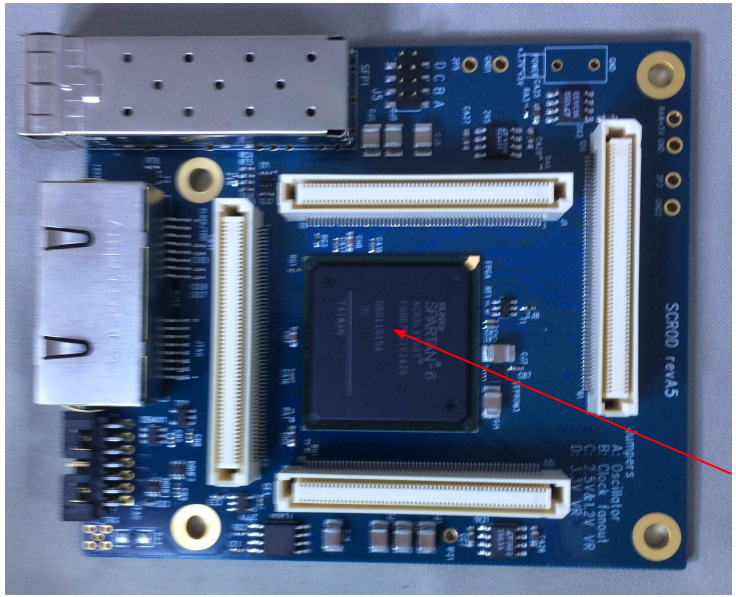


Figure 2. SCROD

- SCROD
  - SCROD card acts as a mother board. The SPARTAN6 FPGA is used to control the daughter cards